VANTIS
BEYOND PERFORMANCE

MACH 5 Power

MACH 5 devices are designed to optimize speed and power for high-performance, low-power designs. In a design file, signals are assigned one of the four power/speed levels. The default level is high-speed/high-power. The device can be powered down on a PAL® block by PAL block basis, and signals with the same speed/power setting are partitioned into PAL blocks set to that power level.

While most MACH 5 designs will safely operate within any available package, there are some designs and system conditions that may generate more heat than a package can reliably dissipate. The heat generated is a function of ambient temperature, device current, supply voltage, device loading, and output frequencies.

Power estimation should be done early in the design process. This can then be used to calculate heat generation and a package can be chosen accordingly. A design can also be modified to reduce power and thus reduce heat generation. There are also other ways to increase heat dissipation.

The formula below is for estimating MACH 5 current consumption:

$$I_{CC} = I_{CC}(\text{Device}) + I_{CC}(\text{DC LOAD}) + I_{CC}(\text{AC LOAD})$$

There are both internal and external (loading) current requirements.

DEVICE CURRENT COMPONENT

Device current in milliamps can be calculated with the following formula:

$$I_{CC}(\text{Device}) = (K0*BLK_{PL0}) + (K1*BLK_{PL1}) + (K2*BLK_{PL2}) + (K3*BLK_{PL3}) + (KAC*MC)*F_{AVE}$$

BLK_{PL0} = Number of PAL blocks in Power Level 0

BLK_{PL1} = Number of PAL blocks in Power Level 1

BLK_{PL2} = Number of PAL blocks in Power Level 2

BLK_{PL3} = Number of PAL blocks in Power Level 3

F_{AVE} = Average Output Frequency of Switching macrocells in MHz

MC = Total Macrocells used in the design

K0–K3 = Static Power Device Constants listed in Table 1

KAC = Dynamic Power Device Constant listed in Table 1

Publication# **20830** Rev: **C**
Amendment/**0** Issue Date: **November 1998**

Table 1. Device Constants

Device	BLK_{TOT}	K0	K1	K2	K3	KAC	$T_{J\ (MAX)}$
M5-128	8	21.6	12.83	8.75	4.38	0.13	150 °C
M5LV-128	8	12.5	6.7	4.35	2.5	0.08	130 °C
M5-192	12	19.3	11.0	7.33	3.75	0.13	150 °C
M5-256	16	20.5	11.8	7.46	3.73	0.13	150 °C
M5LV-256	16	12.0	6.5	4.3	2.5	0.08	130 °C
M5-320 M5LV-320	20	10.5	6.75	4.35	2.85	0.08	130 °C
M5-384 M5LV-384	24	10.5	6.75	4.35	2.85	0.08	130 °C
M5-512 M5LV-512	32	10.5	6.47	4.35	2.56	0.08	130 °C

The BLK_{PL0}, BLK_{PL1}, BLK_{PL2}, BLK_{PL3}, and MC variables can be found in the report (.rpt) file. Below is an excerpt from a report file which shows these variables for a particular design. The average macrocell output frequency must be calculated by the designer.

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POWER SUMMARY:
Number of blocks with power set to LOW is 0
Number of blocks with power set to MED_LOW is 0
Number of blocks with power set to MED_HIGH is 0
Number of blocks with power set to HIGH is 16

DEVICE RESOURCE UTILIZATION:
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Resource	Available	Used	Remaining	%
Clock Pins:	4	0	4	0
I/O Pins:	160	160	0	100
Input Regs:	32	0	32	0
Macrocells:	**256**	**256**	**0**	**100**
Pterms	1168	1048	120	89
1-pt Clusters:	256	256	0	100
3-pt Clusters:	256	256	0	100
Feedbacks	512	216	296	42
Fanouts:	512	368	144	71
Intersegment Lines:	128	0	128	0

Device I_{CC} Is Affected by Temperature and Supply Voltage

I_{CC} is linearly affected by temperature. The given formula for typical conditions (16-bit counters in each PAL block, 25°C and 5-V V_{CC}). Temperature, V_{CC}, and the I_{CC} increase or decrease are shown in Tables 2 and 3. These values are characterized but not tested.

Table 2. Effect of Supply Voltage on I_{CC}

Supply Voltage (V)	M5-128	M5-192	M5-256	M5-320 M5LV-320	M5-384 M5LV-384	M5-512 M5LV-512
4.5 or 3.0 (LV)	–11%	–11%	–11%	–6%	–6%	–6%
4.75	–6%	–6%	–6%	–3%	–3%	–3%
5.25	+7%	+7%	+7%	+1%	+1%	+1%
5.5 or 3.6 (LV)	+13%	+13%	+13%	+3%	+3%	+3%

Table 3. Effect of Ambient Temperature on I_{CC}

Ambient Temperature	M5-128	M5-192	M5-256	M5-320 M5LV-320	M5-384 M5LV-384	M5-512 M5LV-512
T = –40°C	+14%	+14%	+14%	–4%	–4%	–4%
T = 0°C	+1%	+1%	+1%	–1%	–1%	–1%
T = 70°C	–1%	–1%	–1%	+2%	+2%	+2%
T = 85°C	–1%	–1%	–1%	+5%	+5%	+5%

LOAD COMPONENT

The AC load current required by capacitive loading is dependent on voltage, capacitance, and average output frequency.

AC Load Component

No. of I/Os used

$$I_{CC}\ (AC\ Load) = \sum_{n=1} F_n * C_n * (V_{OH} - V_{OL})$$

F_n = *Output frequency of output*

C_n = *Capacitive loading of output*

V_{OH} = *Output Voltage High of the output*

V_{OL} = *Output Voltage Low of the output*

DC Load Component

No. of I/Os used

$$I_{CC}\ (DC\ Load) = \sum_{n=1} V_{OUTn}/R_n$$

V_{OUTn} = *Output frequency of output*

R_n = *Resistive loading of output*

CALCULATING PACKAGE POWER REQUIREMENTS

A package must be able to dissipate enough power to keep the internal silicon junction temperature below the maximum allowable junction temperature ($T_{J(MAX)}$). The following formula is used to calculate the maximum power allowable for a particular package.

$$V_{CC} * I_{CC} \leq (T_{J(MAX)} - T_A)/\Theta_{JA}$$

V_{CC} = *Supply Voltage*

I_{CC} = *Calculated Current*

T_A = *Ambient Temperature*

Θ_{JA} = *Junction-Ambient Thermal Impedance*

The maximum allowable power for a package is dependent on the thermal resistance of that package. Packages with a low thermal resistance are able to dissipate more heat than packages with a high thermal resistances. Air flow can also reduce the thermal impedance. Θ_{JMA} is the junction to ambient thermal impedance with air flow.

THERMAL MANAGEMENT OPTIONS

If an application generates more heat than a package can dissipate, then steps can be taken to reduce heat generation such as:

1. **Power down additional PAL blocks**—Few designs require all signals to run at maximum frequencies. The four power/speed options per PAL block allow optimization for the lowest power at the highest speeds.
2. **Use an external heat sink**—The external heat sink will decrease the thermal impedance of a package and raise the maximum allowable temperature.
3. **Reduce the load on the outputs**—In many applications, heavily loaded outputs significantly increase power requirements. The Bus-Friendly™ inputs and I/Os do not require external resistive loading to float to a known state. Capacitive loading should also be monitored at high frequencies.
4. **Reduce device utilization**—Device current requirements depend on device utilization. Lowering utilization will lower the current required. Multi-device partition facilitates this process.
5. **Choose a package with lower thermal resistances**—Packages with a low thermal resistance are able to dissipate more heat than packages with a high thermal resistances.
6. **Reduce the average output frequency**—The average output frequency affects both the device and load components of power. Reducing the output frequency will reduce the required power.
7. **Reduce the number of outputs**—Reducing outputs reduces the load current required. Multi-device partitioning facilitates this process.
8. **Lower V_{CC}**—Use a 3.3-V device instead of a 5-V device. While I_{CC} is nearly identical, the lower V_{CC} results in lower power.

EXAMPLE POWER ESTIMATION

Counters

The average output frequency of a counter is one-eighth the output frequency of the least significant bit (LSB) of the counter. The most power efficient method for implementing several high speed counters would place the LSBs in a high speed PAL block and the most significant bits (MSBs) in a lower-power PAL block. If all PAL blocks are set to the same power level and the I_{CC} vs. frequency is measured, the following formula is used:

$$I_{CC}(\text{Device}) = BLK_{TOT}*K(x) + KAC*F_{AVE}*MC_{TOT}$$

An example of this is for the M5LV-256 device in high-power mode with a 16-bit counter pattern per PAL block at a clock frequency of 125 MHz. If positive or negative edge clocking is used, then the LSB, will switch at 62.5 MHz, and the average output frequency will be 8 MHz. The equation would be as follows:

$$I_{CC}(\text{Device}) = (16)*(12.0) + (0.08)*(8)*(256) = 356 \text{ mA}$$

If under the same conditions, biphase clocking is used, then a 125 MHz clock produces a 125 MHz LSB, and the average output frequency doubles to 16 MHz:

$$I_{CC}(\text{Device}) = (16)*(12.0) + (0.08)*(16)*(256) = 520 \text{ mA}$$

To determine if this design will run safely in the 208 PQFP package, the following calculation is done:

$$V_{CC}*I_{CC}*\Theta_{JA} + T_A \leq 130\,^{\circ}C$$

$$(3.3)(0.356)(33) + 70 = 108\,^{\circ}C \leq 130\,^{\circ}C$$

This design will safely operate in this package.