VANTIS
BEYOND PERFORMANCE

Latch-Up

LATCH-UP CIRCUIT

Latch-up is caused by an SCR (Silicon Controlled Rectifier) circuit. Fabrication of CMOS integrated circuits with bulk silicon processing creates a parasitic SCR structure. The behavior of this SCR is similar in principle to a true SCR. These structures result from the multiple diffusions needed for the formation of complementary MOS transistors in CMOS processing. The SCR structure consists of a four-layer device formed by diffused PNPN regions. These four layers create parasitic bipolar transistors illustrated in Figure 1.

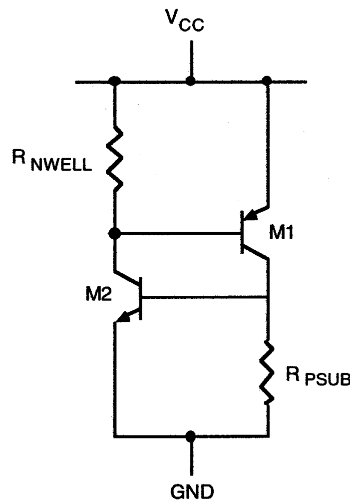

Figure 1. Parasitic Bipolar Transistors 14105C-001

Figure 2 shows a typical CMOS inverter layout with the schematic of the parasitic bipolar SCR structure. Figure 3 is a cross-sectional representation of the CMOS inverter, again with the schematic of the bipolar SCR structure.

Any CMOS diffusion can become part of the parasitic SCR structure, since all of these parts are interconnected through the bulk silicon substrate resistance. Other parasitic resistors shown result from doped regions of the semiconductor. The magnitude to which the resistors resist current flow depends upon geometric size and doping level.

As illustrated in Figure 1, the complementary PNP and NPN transistors are cross-coupled, having common base-collector regions. The vertical PNP device, M1, has its base composed of the N-well diffusion, while the emitter and collector are formed from P-type source-drain and substrate regions, respectively. The lateral bipolar transistor, M2, base is the P substrate with emitter and collector junctions formed from N-type source-drain and N-well diffusions, respectively.

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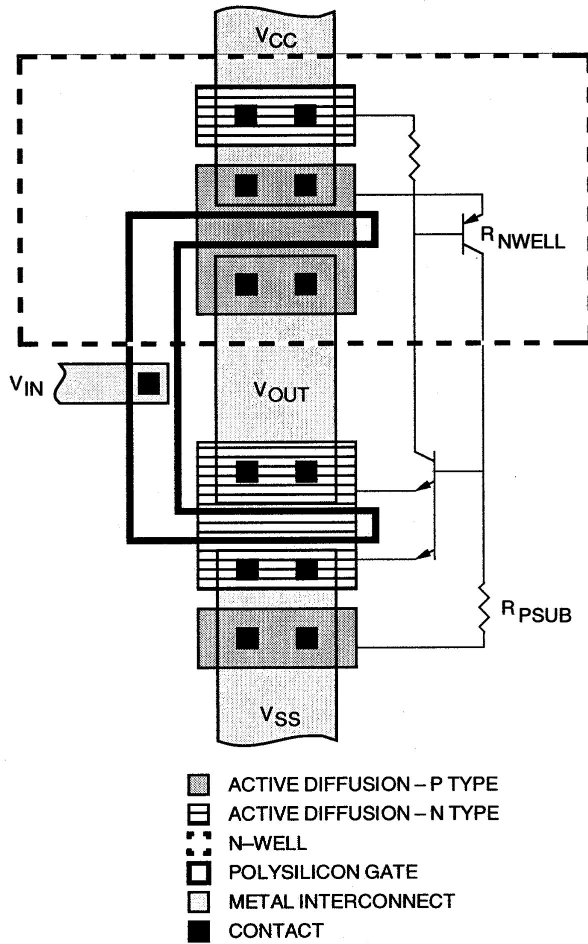

Figure 2. Typical CMOS Inverter Layout

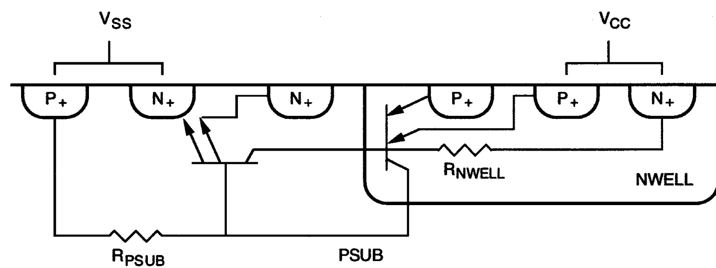

Figure 3. Cross Section of CMOS Inverter

Latch-Up Conditions

Under normal bias conditions, the SCR conducts only leakage current, and the SCR structure is in the blocking state. However, as current flows across any of the parasitic resistors, a voltage drop is developed, turning on the parasitic bipolar base-emitter junction. The forward bias condition of this junction allows collector current to flow in the bipolar transistor. This collector current flows across the base-emitter resistor of the complementary bipolar transistor, creating a voltage sufficient to turn on the transistor.

A regenerative loop is now created between the complementary bipolar transistors such that current conduction becomes self-sustaining. Even after removal of the stimulus that triggered this action, the current conduction can continue. This region of operation is a high-current, low-resistance condition characteristic of a four-layer PNPN structure. This is referred to as latch-up. Once initiated, the excessive latch-up current can permanently damage an integrated circuit by fusing metal lines or destroying junctions.

CAUSES OF LATCH-UP

Latch-up may be initiated in numerous ways. Only the critical causes frequently encountered in a system environment will be discussed. These include power-up, supply overvoltage, and overshoot/undershoot at device pins.

Power-Up

Caution must be exercised when powering up most CMOS ICs to avoid driving device pins before the supply voltage has been applied to the circuit. Placing a device or board in a “hot socket” will create this situation. When subjected to hot-socket insertion, voltage conditions at the device pins are uncertain such that the input diodes may be forward biased. Forward biasing the input diodes with a delayed or uncontrolled application of V_{CC} could cause the device to latch up. Some of Vantis’ CMOS circuits have substantial immunity to hot socket power-up, but since this condition is uncertain and difficult to characterize, test, and guarantee, it should be avoided. Vantis’ MACH®4 and MACH 5 devices have been designed to be hot socketable and will not latch up.

Supply Overvoltage

Supply levels exceeding the absolute maximum rating can cause a CMOS circuit to latch up. Elevated supply voltage may cause internal junctions to break down, producing substrate current capable of triggering latch-up. Latch-up is one of the reasons overvoltage should be avoided; other undesirable effects may result from this.

Overshoot/Undershoot

Generally, the I/O pins experience the noisiest electrical environment. Fast switching signals with a large capacitive load may overshoot, creating a transient forward bias condition at the I/O junction. These junction diodes are illustrated in Figures 4 and 5. Typically, this is where latch-up is most likely to be induced. Proper design of the input and output buffers is essential to minimize the risk of latch-up due to overshoot.

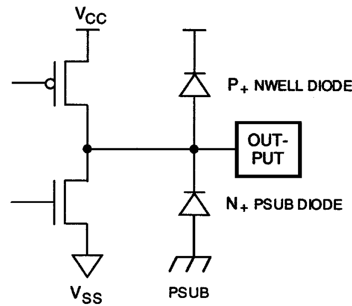

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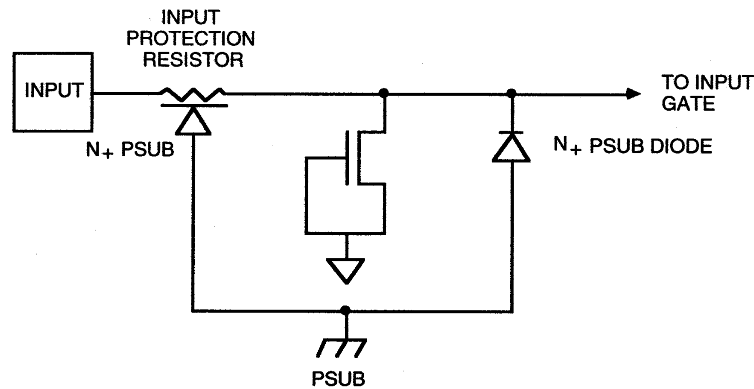
Figure 4. Junction Diode



14105C-005

Figure 5. Junction Diode

TESTING FOR LATCH-UP

Vantis characterizes the latch-up sensitivity of its devices before they are released to the market. Testing is done in such a way as to completely cover every possible latch-up condition, including V_{CC} overvoltage, pin overcurrent, and pin overvoltage.

V_{CC} Overvoltage Test

The V_{CC} overvoltage test is applied to all power (V_{CC}) pins. The test is performed at the highest guaranteed operating temperature of the device. All inputs and I/Os acting as inputs are tied to ground or V_{CC} depending on the device logic, and outputs and I/Os acting as outputs are floating (open).

V_{CC} max is applied to the V_{CC} pin. A positive high voltage pulse is then applied to the V_{CC} pin and returned to V_{CC} max. The occurrence of latch-up is detected if the voltage across the device is less than V_{CC} max, and the current through the device is greater than the normal DC operating current.

Pin Overcurrent Test

The pin overcurrent test is performed on every output, I/O pin, and non-current-limited input pin. Non-current-limited inputs are inputs which present a diode-like (or otherwise "infinite") current characteristic for input voltages in the range (GND – $V_{CC(TYP)}$) < V_{IN} < (2 x $V_{CC(TYP)}$).

The pin overcurrent test is performed at the highest guaranteed operating temperature of the device. Input pins and I/O pins acting as inputs (which are not under test) are tied to ground or V_{CC} depending on the device logic, and outputs and I/Os acting as outputs should be floating (open). V_{CC} max is applied to the V_{CC} pin.

One pin is tested at a time. A three-state output under test should be disabled. A non-three-state output type under test should be a logic High when applying a positive current and a logic Low when applying a negative current. An I/O pin should be placed into the input mode.

A high current pulse is then applied to the pin under test. The magnitude of the pulse is stepped until latch-up is induced. Both positive and negative currents are tested. Latch-up is observed as described previously. The sensitivity of the device is the worst case sensitivity found on any pin of the device.

Pin Overvoltage Test

The pin overvoltage test is performed on current-limited inputs. Current-limited inputs are inputs which present a resistor-like (or otherwise "limited") current characteristic for input voltages in the range (GND – $V_{CC(TYP)}$) < V_{IN} < (2 x $V_{CC(TYP)}$).

The pin overvoltage test is performed at the highest guaranteed operating temperature of the device. Input pins and I/O pins acting as inputs (which are not under test) are tied to ground or V_{CC} depending on the device logic, and outputs and I/Os acting as outputs are floating (open). V_{CC} max is applied to the V_{CC} pin.

One pin is tested at a time. Both positive and negative voltage pulses are applied to the pin under test. Latch-up is observed as described previously. The sensitivity of the device is the worst-case sensitivity found on any pin of the device.