Manual Update Sheet

DATE: June 1, 1998

Document Being Updated: ***TMS320C5x User's Guide*** **Literature Number Being Updated: SPRU056C**

Manual Included in a Kit: Yes

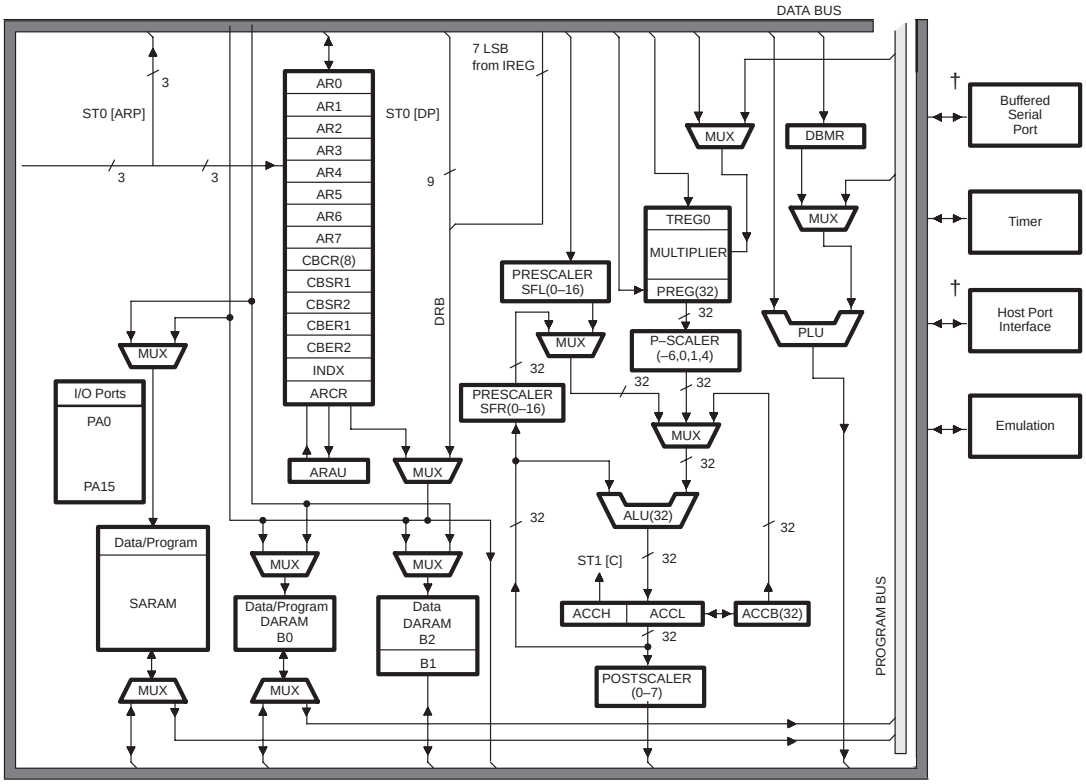
This Manual Update Sheet (SPRZ113A) ships with the *TMS320C5x User's Guide*.

Updates within paragraphs appear in a **bold typeface**.

Page: **Change or Add:**

3–3 In the bottom half of Figure 3–1, the auxiliary register file MUX output now connects with the trailing wire bus found on the data bus.

Figure 3–1. Block Diagram of 'C5x DSP – Central Processing Unit (CPU)



Notes: All registers and data lines are 16-bits wide unless otherwise specified.
† Not available on all devices.

Page: **Change or Add:**

4–11 In Table 4–5, change the reset values for the ARP bit and the OVM bit so both have a reset value of “X.” In other words, there is no reset value for the ARP bit and the OVM bit.

Table 4–5. Status Register 0 (ST0) Bit Summary

Bit	Name	Reset value	Function
15–13	ARP	**X**	Auxiliary register pointer. These bits select the auxiliary register (AR) to be used in indirect addressing. When the ARP is loaded, the previous ARP value is copied to the auxiliary register buffer (ARB) in ST1. The ARP can be modified by memory-reference instructions when you use indirect addressing, and by the MAR or LST #0 instruction. When an LST #1 instruction is executed, the ARP is loaded with the same value as the ARB.
11	OVM	**X**	Overflow mode bit. This bit enables/disables the accumulator overflow saturation mode in the arithmetic logic unit (ALU). The OVM bit can be modified by the LST #0 instruction. OVM = 0 Disabled. An overflowed result is loaded into the accumulator without modification. The OVM bit can be cleared by the CLRC OVM instruction. OVM = 1 Overflow saturation mode. An overflowed result is loaded into the accumulator with either the most positive (00 7FFF FFFFh) or the most negative value (FF 8000 0000h). The OVM bit can be set by the SETC OVM instruction.

4–12 In Table 4–5, change the reset value for the DP bit so it has a reset value of “X.” In other words, there is no reset value for the DP bit.

Table 4–5. Status Register 0 (ST0) Bit Summary (Continued)

Bit	Name	Reset value	Function
8–0	DP	**X**	Data memory page pointer bits. These bits specify the address of the current data memory page. The DP bits are concatenated with the 7 LSBs of an instruction word to form a direct memory address of 16 bits. The DP bits can be modified by the LST #0 or LDP instruction.

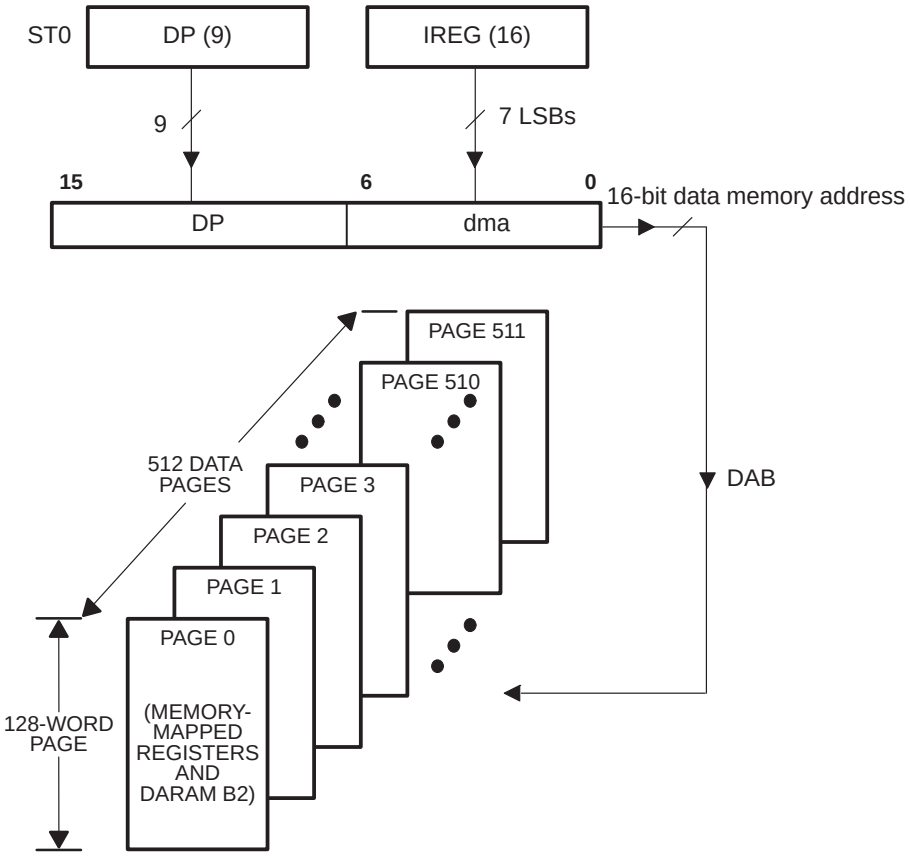
Page:	Change or Add:
4–13	In Table 4–6, change the reset value for the ARB bit and the TC bit so they have no reset value.

Table 4–6. Status Register 1 (ST1) Bit Summary

Bit	Name	Reset value	Function
15–13	ARB	**X**	Auxiliary register buffer. This 3-bit field holds the previous value contained in the auxiliary register pointer (ARP) in ST0. Whenever the ARP is loaded, the previous ARP value is copied to the ARB, except when using the LST #0 instruction. When the ARB is loaded using the LST #1 instruction, the same value is also copied to the ARP. This is useful when restoring context (when not using the automatic context save) in a subroutine that modifies the current ARP.
11	TC	**X**	Test/control flag bit. This 1-bit flag stores the results of the arithmetic logic unit (ALU) or parallel logic unit (PLU) test bit operations. The TC bit is affected by the APL, BIT, BITT, CMPR, CPL, NORM, OPL, and XPL instructions. The status of the TC bit determines if the conditional branch, call, and return instructions execute. The TC bit can be modified by the LST #1 instruction.

Page:	Change or Add:
5–2	In Figure 5–1, change the page 0 length to “128-WORD PAGE.”

Figure 5–1. Direct Addressing



Page: **Change or Add:**

5–22 In Example 5–13, add two new lines at the beginning of the example.

Example 5–13. Circular Addressing

```
mar    *,ar6
ldp    #,0

splk   #200h,CBSR1  ;  Circular buffer start register
splk   #203h,CBER1  ;  Circular buffer end register
splk   #0Eh,CBCR    ;  Enable AR6 pointing to buffer 1

lar    ar6,#200h    ;  Case 1
lacc   *            ;  AR6 = 200h

lar    ar6,#203h    ;  Case 2
lacc   *            ;  AR6 = 203h

lar    ar6,#200h    ;  Case 3
lacc   *+           ;  AR6 = 201h

lar    ar6,#203h    ;  Case 4
lacc   *+           ;  AR6 = 200h

lar    ar6,#200h    ;  Case 5
lacc   *–           ;  AR6 = 1FFh

lar    ar6,#203h    ;  Case 6
lacc   *–           ;  AR6 = 200h

lar    ar6,#202h    ;  Case 7
adrk   2            ;  AR6 = 204h

lar    ar6,#203h    ;  Case 8
adrk   2            ;  AR6 = 200h
```

Page: **Change or Add:**

6–32 Change the second operand for the ADD instruction.

Operands 0 ≤ shift ≤**16** (defaults to 0)

6–44 Change the fourth operand for the AND instruction.

Operands 0 ≤ shift ≤ **16**

6–83 Change the operand for the BSAR instruction.

Operands 1 ≤ shift ≤ **16**

6–85 Change the description for the CALAD instruction.

Description **The current program counter (PC) is incremented by 3 and pushed onto the top of the stack (TOS).**

Then, the one 2-word instruction or two 1-word instructions following the CALAD instruction are fetched from program memory and executed before the call is executed.

Then, the contents of the accumulator low byte (ACCL) are loaded into the PC. Execution continues at this address.

The CALAD instruction is used to perform computed subroutine calls. CALAD is a branch and call instruction (see Table 6–8).

6–87 Change the description for the CALLD instruction.

Description **The current program counter (PC) is incremented by 4 and pushed onto the top of the stack (TOS).**

Then, the one 2-word instruction or two 1-word instructions following the CALLD instruction are fetched from program memory and executed before the call is executed**.**

The program memory address (pma) is loaded into the PC. Execution continues at this address. The current auxiliary register (AR) and auxiliary register pointer (ARP) are modified as specified. The pma can be either a symbolic or numeric address.

CALLD is a branch and call instruction (see Table 6–8).

Page: **Change or Add:**

6–91 Change the description for the CCD instruction.

Description **If the specified conditions are met, the current program counter (PC) is incremented by 4 and pushed onto the top of the stack (TOS).**

Then, the one 2-word instruction or two 1-word instructions following the CCD instruction are fetched from program memory and executed before the call is executed.

Then, the program memory address (pma) is loaded into the PC. Execution continues at this address. The pma can be either a symbolic or numeric address. Not all combinations of the conditions are meaningful. In addition, the NTC, TC, and BIO conditions are mutually exclusive.

If the specified conditions are not met, control is passed to the next instruction.

The CCD functions in the same manner as the CALLD instruction (page 6–87) if all conditions are true. CCD is a branch and call instruction (see Table 6–8).

6–103 Change the opcode for the CRLT instruction to reflect the new values for bits 2, 1, and 0.

Opcode

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	1	1	1	1	0	0	0	0	1	1	**1**	**0**	**0**

6–115 Change the third operand for the LACC instruction.

Operands 0 ≤ shift ≤ **16** (defaults to 0)

6–127 Change the table Cycles for a Single Instruction (short immediate addressing).

Cycles for a Single Instruction (short immediate addressing)

Operand	ROM	DARAM	SARAM	External Memory
	2	2	2	$2+p_{code}$

6–129 Change the table Cycles for a Single Instruction (short immediate addressing).

Cycles for a Single Instruction (short immediate addressing)

Operand	ROM	DARAM	SARAM	External Memory
	2	2	2	$2+p_{code}$

6–188 Change the fourth operand for the OR instruction.

Operands 0 ≤ shift ≤ **16**

6–261 Change the second operand for the SUB instruction.

Operands 0 ≤ shift ≤ **16** (defaults to 0)

6–278 Change the data memory address in Example 1 from 1905h to 1005h.

6–282 Change the fourth operand for the XOR instruction.

Operands 0 ≤ shift ≤ **16**

Page: **Change or Add:**

8–6 In Figure 8–6, change the word Off-chip to Reserved on the Program memory map for the range from 0040h to 8000h.

8–11 In Table 8–6, change the values in the Off-Chip column for the first and fifth rows.

Table 8–6. 'C57S Program Memory Configuration

Bit values			ROM	SARAM	DARAM B0	
CNF	RAM	MP/$\overline{MC}$	(2K-words)	(6K-words)	(512-words)	Off-Chip
0	0	0	0000–07FF	Off-chip	Off-chip	**8000**–FFFF
1	0	0	0000–07FF	Off-chip	FE00–FFFF	**8000**–FDFF

8–32 Change the last sentence in the fourth bullet.

- 32K words of global data memory are enabled initially in data spaces 8000h to FFFFh. After the code transfer is complete, the global memory is disabled before control is transferred to the destination address **in program memory**.

9–10 In Table 9–4, change the sentences after Soft=0 and Soft=1. Also, add a sentence to the TSS register.

Table 9–4. Timer Control Register (TCR) Bit Summary

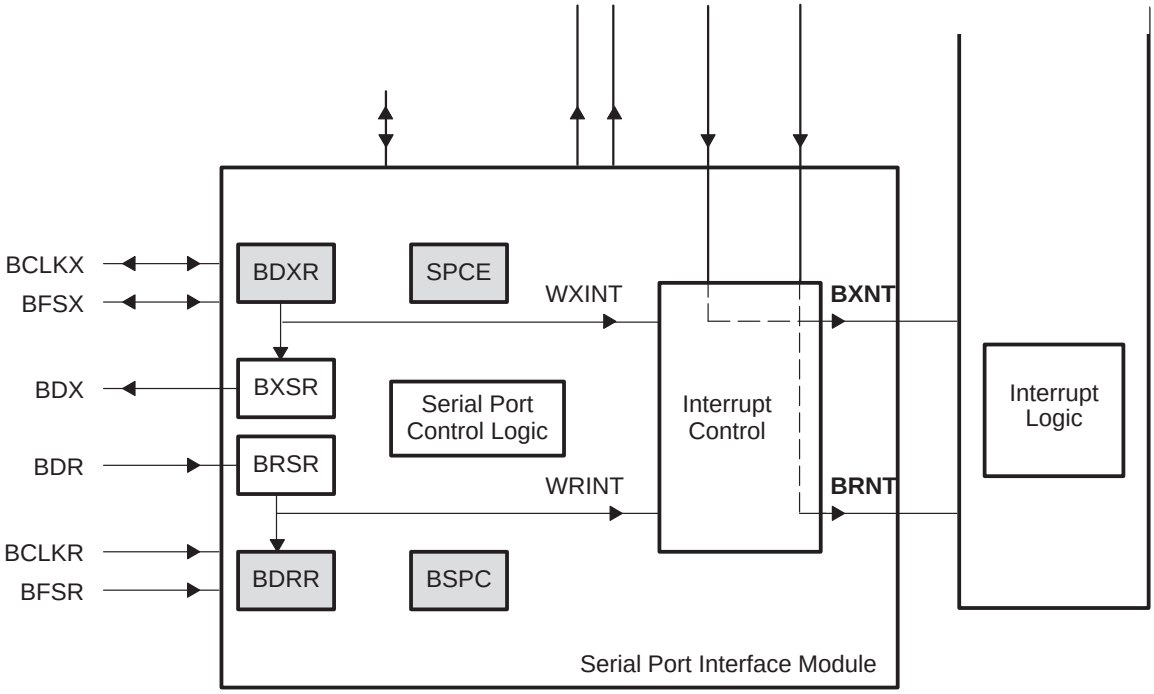
Bit	Name	Reset value	Function
11	Soft	0	This bit is used in conjunction with the Free bit to determine the state of the timer when a halt is encountered. When the Free bit is cleared, the Soft bit selects the emulation mode. Soft = 0 The timer stops immediately. Soft = 1 The timer stops **after decrementing to zero**.
4	TSS	0	Timer stop status bit. This bit stops or starts the on-chip timer. At reset, the TSS bit is cleared and the timer immediately starts timing. **Note that due to timer logic implementation, two successive writes of one to the TSS bit are required to properly stop the timer.**

9–11 Delete the last sentence in the Notes section and replace it with the sentence indicated.

The current value in the timer can be read by reading the TIM; the PSC can be read by reading the TCR. Because it takes two instructions to read both registers, there may be a change between the two reads as the counter decrements. Therefore, when making precise timing measurements, it may be more accurate to stop the timer to read these two values. **Due to timer logic implementation, two instructions are also required to properly stop the timer; therefore, two successive writes of one to the TSS bit should be made when the timer must be stopped.**

Page:	Change or Add:
9–62	Change the XINT and RINT labels found in the lower right portion of Figure 9–35.

Figure 9–35. ABU Block Diagram



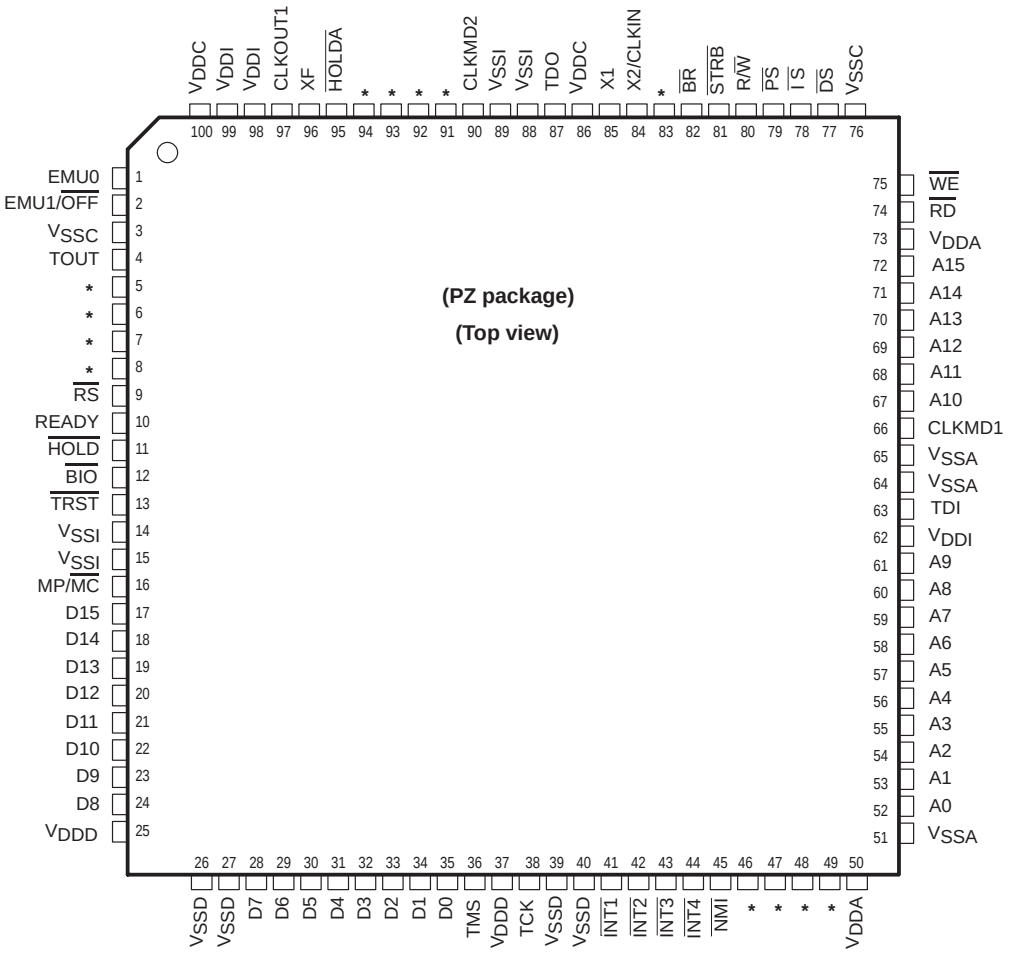
Page:	Change or Add:
9–63	Change the last sentence in the first paragraph.

The internal ’C5X memory used for autobuffering consists of a 2K-word block of single-access memory that can be configured as data, program, or both (as with other single-access memory blocks). This memory can also be used by the CPU as general purpose storage, however, this is the only memory block in which autobuffering can occur. Since the BSP is implemented on several different TMS320 devices, the actual base address of the ABU memory may not be the same in all cases. **The 2K-word block of BSP memory is located at 800h–FFFh in data memory or at 8000h–87FFh in program memory as specified by the RAM and OVLY control bits**.

Page: **Change or Add:**

A–4 In Figure A–2, change the signal name on pin 80 to R/$\overline{W}$.

Figure A-2. Pin/Signal Assignments for the ’C51, ’C52, ’C53S, and ’LC56 in 100-Pin TQFP

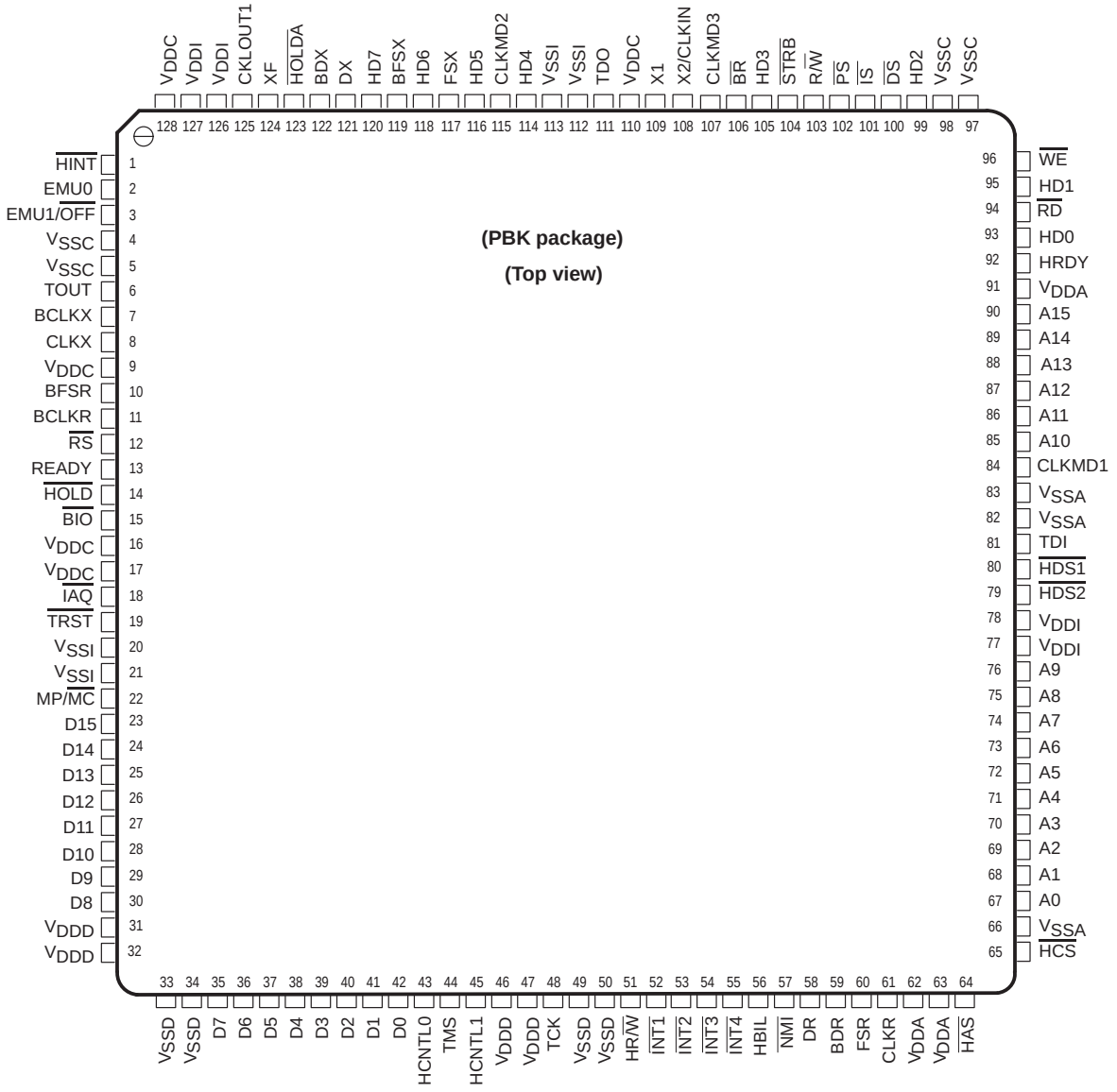


Note: * These pins are reserved for specific devices (see Table A–6 on page A-12).

Page: **Change or Add:**

A–6 In Figure A–3, change the signal name on pin 108 to X2/CLKIN.

Figure A–3. Pin/Signal Assignments for the ’LC57 in 128-Pin TQFP



Page: **Change or Add:**

A–7 In Table A–3, change the signal name on pin 108 to X2/CLKIN and reorder the signal names.

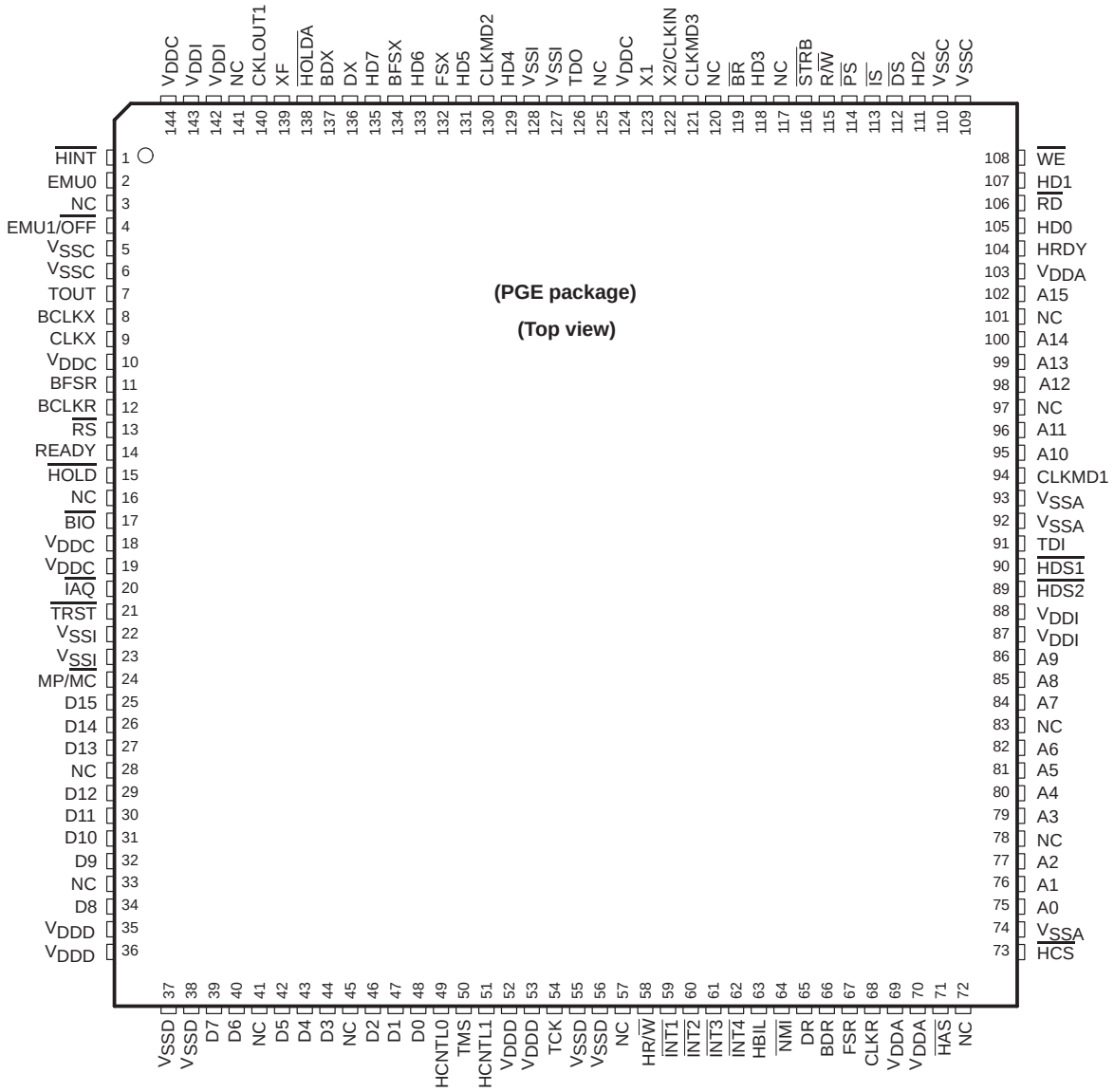
Table A–3. Signal/Pin Assignments for the 'LC57 in 128-Pin TQFP

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
A0	67	CLKMD3	107	FSX	117	$\overline{IS}$	101	V_{DDD}	47
A1	68	CLKOUT1	125	$\overline{HAS}$	64	MP/$\overline{MC}$	22	V_{DDI}	77
A2	69	CLKR	61	HBIL	56	$\overline{NMI}$	57	V_{DDI}	78
A3	70	CLKX	8	HCNTL0	43	$\overline{PS}$	102	V_{DDI}	126
A4	71	D0	42	HCNTL1	45	$\overline{RD}$	94	V_{DDI}	127
A5	72	D1	41	$\overline{HCS}$	65	READY	13	V_{SSA}	66
A6	73	D2	40	HD0	93	$\overline{RS}$	12	V_{SSA}	82
A7	74	D3	39	HD1	95	R/$\overline{W}$	103	V_{SSA}	83
A8	75	D4	38	HD2	99	$\overline{STRB}$	104	V_{SSC}	4
A9	76	D5	37	HD3	105	TCK	48	V_{SSC}	5
A10	85	D6	36	HD4	114	TDI	81	V_{SSC}	97
A11	86	D7	35	HD5	116	TDO	111	V_{SSC}	98
A12	87	D8	30	HD6	118	TMS	44	V_{SSD}	33
A13	88	D9	29	HD7	120	TOUT	6	V_{SSD}	34
A14	89	D10	28	$\overline{HDS1}$	80	$\overline{TRST}$	19	V_{SSD}	49
A15	90	D11	27	$\overline{HDS2}$	79	V_{DDC}	9	V_{SSD}	50
BCLKR	11	D12	26	$\overline{HINT}$	1	V_{DDA}	91	V_{SSI}	20
BCLKX	7	D13	25	$\overline{HOLD}$	14	V_{DDA}	63	V_{SSI}	21
BDR	59	D14	24	$\overline{HOLDA}$	123	V_{DDA}	62	V_{SSI}	112
BDX	122	D15	23	HRDY	92	V_{DDC}	16	V_{SSI}	113
BFSR	10	DR	58	HR/$\overline{W}$	51	V_{DDC}	17	$\overline{WE}$	96
BFSX	119	$\overline{DS}$	100	$\overline{IAQ}$	18	V_{DDC}	110	X1	109
$\overline{BIO}$	15	DX	121	$\overline{INT1}$	52	V_{DDC}	128	X2/CLKIN	108
$\overline{BR}$	106	EMU0	2	$\overline{INT2}$	53	V_{DDD}	31	XF	124
CLKMD1	84	EMU1/$\overline{OFF}$	3	$\overline{INT3}$	54	V_{DDD}	32		
CLKMD2	115	FSR	60	$\overline{INT4}$	55	V_{DDD}	46		

Page: **Change or Add:**

A–10 In Figure A–5, correct the signal names for pins 1–16, 28–45, 57–71, and 78–141; change the signal name on pin 122 to X2/CLKIN.

Figure A–5. Pin/Signal Assignments for the ’C57S in 144-Pin TQFP



Note: NC These pins are not connected (reserved).

Page: **Change or Add:**

A–11 In Table A–5, correct the signal names for pins 1–16, 28–45, 57–71, and 78–141; change the signal name on pin 122 to X2/CLKIN; reorder the signal names.

Table A–5. Signal/Pin Assignments for the ’C57S in 144-Pin TQFP

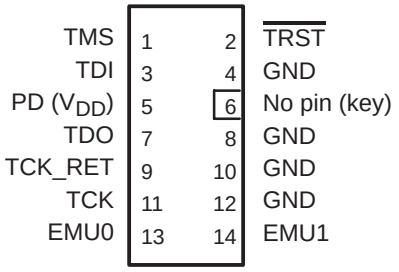
Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
A0	75	CLKX	9	HD0	105	TCK	54	V_{SSD}	37
A1	76	D0	48	HD1	107	TDI	91	V_{SSD}	38
A2	77	D1	47	HD2	111	TDO	126	V_{SSD}	55
A3	79	D2	46	HD3	118	TMS	50	V_{SSD}	56
A4	80	D3	44	HD4	129	TOUT	7	V_{SSI}	22
A5	81	D4	43	HD5	131	$\overline{\text{TRST}}$	21	V_{SSI}	23
A6	82	D5	42	HD6	133	V_{DDA}	69	V_{SSI}	127
A7	84	D6	40	HD7	135	V_{DDA}	70	V_{SSI}	128
A8	85	D7	39	$\overline{\text{HDS1}}$	90	V_{DDA}	103	$\overline{\text{WE}}$	108
A9	86	D8	34	$\overline{\text{HDS2}}$	89	V_{DDC}	10	X1	123
A10	95	D9	32	$\overline{\text{HINT}}$	1	V_{DDC}	18	X2/CLKIN	122
A11	96	D10	31	$\overline{\text{HOLD}}$	15	V_{DDC}	19	XF	139
A12	98	D11	30	$\overline{\text{HOLDA}}$	138	V_{DDC}	124	†	3
A13	99	D12	29	HRDY	104	V_{DDC}	144	†	16
A14	100	D13	27	HR/$\overline{\text{W}}$	58	V_{DDD}	35	†	28
A15	102	D14	26	$\overline{\text{IAQ}}$	20	V_{DDD}	36	†	33
BCLKR	12	D15	25	$\overline{\text{INT1}}$	59	V_{DDD}	52	†	41
BCLKX	8	DR	65	$\overline{\text{INT2}}$	60	V_{DDD}	53	†	45
BDR	66	$\overline{\text{DS}}$	112	$\overline{\text{INT3}}$	61	V_{DDI}	87	†	57
BDX	137	DX	136	$\overline{\text{INT4}}$	62	V_{DDI}	88	†	72
BFSR	11	EMU0	2	$\overline{\text{IS}}$	113	V_{DDI}	142	†	78
BFSX	134	EMU1/$\overline{\text{OFF}}$	4	MP/$\overline{\text{MC}}$	24	V_{DDI}	143	†	83
$\overline{\text{BIO}}$	17	FSR	67	$\overline{\text{NMI}}$	64	V_{SSA}	74	†	97
$\overline{\text{BR}}$	119	FSX	132	$\overline{\text{PS}}$	114	V_{SSA}	92	†	101
CLKMD1	94	$\overline{\text{HAS}}$	71	$\overline{\text{RD}}$	106	V_{SSA}	93	†	117
CLKMD2	130	HBIL	63	READY	14	V_{SSC}	5	†	120
CLKMD3	121	HCNTL0	49	$\overline{\text{RS}}$	13	V_{SSC}	6	†	125
CLKOUT1	140	HCNTL1	51	R/$\overline{\text{W}}$	115	V_{SSC}	109	†	141
CLKR	68	$\overline{\text{HCS}}$	73	$\overline{\text{STRB}}$	116	V_{SSC}	110		

† These pins are not connected (reserved).

Page: **Change or Add:**

D–2 In Figure D–1, change the PD pin 5 from +5V to V_{DD}.

Figure D–1. Header Signals and Header Dimensions



Header Dimensions:
Pin-to-pin spacing: 0.100 in. (X,Y)
Pin width: 0.025 in. square post
Pin length: 0.235 in., nominal

In Table D–1, change the voltage for pin 5 (the PD pin) from +5V to V_{DD}.

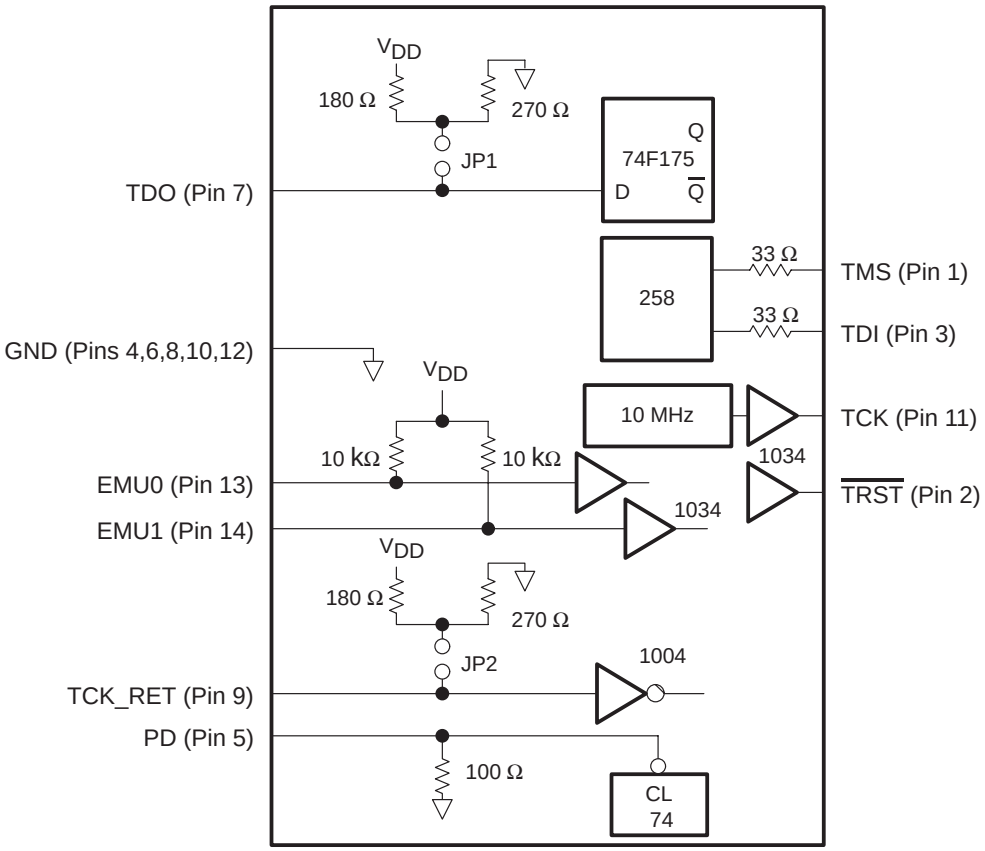
Table D–1. XDS510 Header Signal Description

Pin	Signal	State	Target State	Description
5	PD	I	O	Presence detect. Indicates that the emulation cable is connected and that the target is powered up. PD should be tied to **V_{DD}** in the target system.

Page: **Change or Add:**

D–5 In Figure D–2, change the voltages from +5V to V_{DD}.

Figure D–2. Emulator Cable Pod Interface

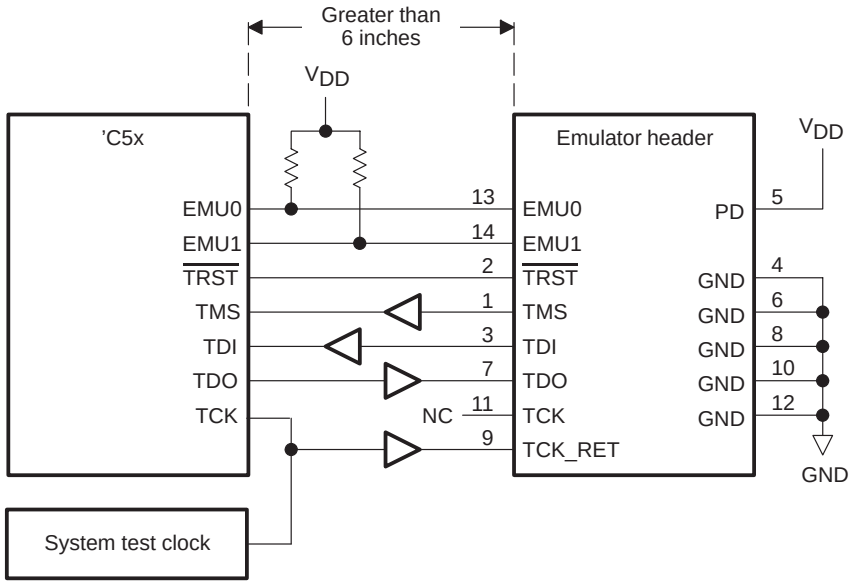


NOTE:
All devices are 74AS, unless otherwise specified.

Page: **Change or Add:**

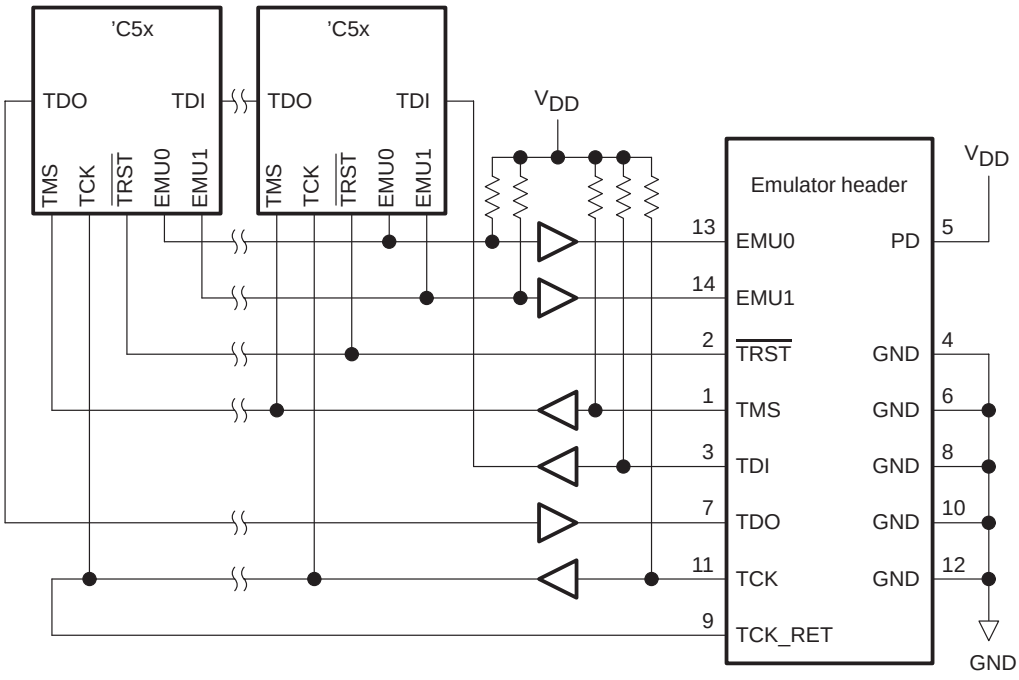
D–7 In Figure D–4, change the voltages from +5V to V_{DD}.

Figure D–4. Target-System Generated Test Clock



D–8 In Figure D–5, change the voltages from +5V to V_{DD}.

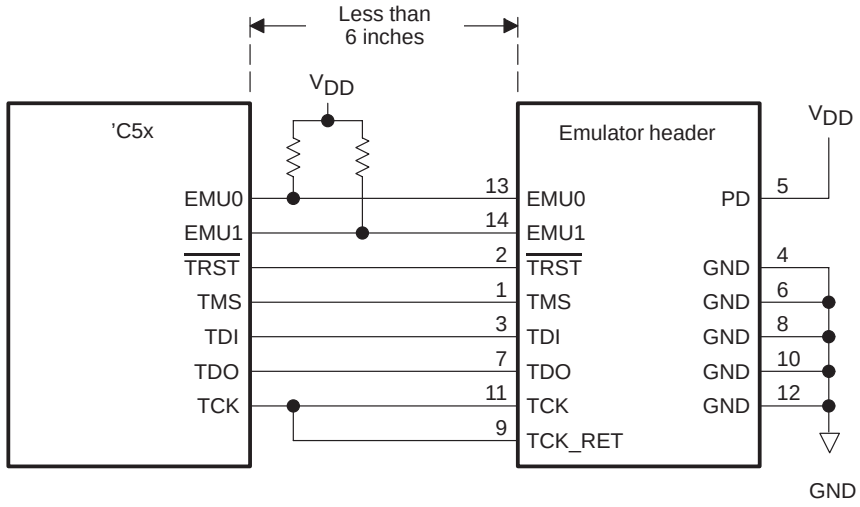
Figure D–5. Multiprocessor Connections



Page: **Change or Add:**

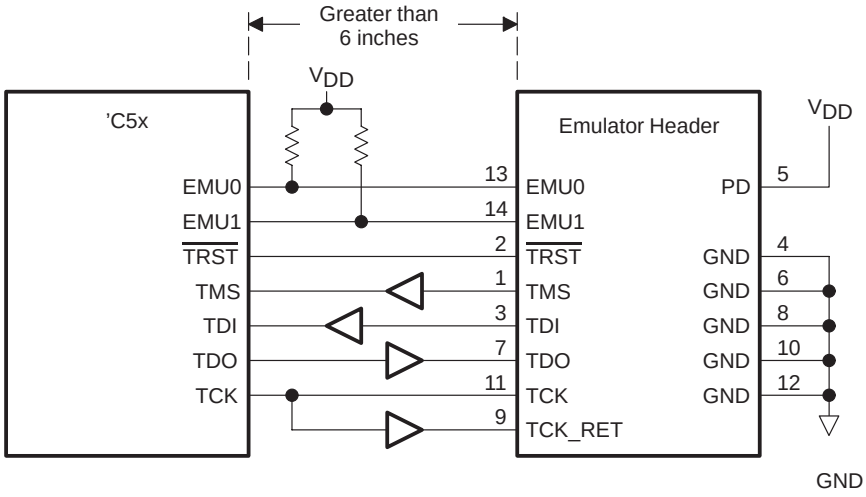
D–9 In Figure D–6, change the voltages from +5V to V_{DD}.

Figure D–6. Emulator Connections Without Signal Buffering



D–10 In Figure D–7, change the voltages from +5V to V_{DD}.

Figure D–7. Buffered Signals



IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.