Dead-Time Generation on the TMS320C24x

Application Report
SPRA371

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain application using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Overview

A Dead-Band generator protects the power semiconductors during the commutation. The dead time is programmable between 0µs and 102µs. This time range is sufficient for all kinds of power semi-conductors (MOSFET, IGBT, BIPOLAR, and THYRISTOR) in a wide range of kW (kiloWatt) or HP (Horse Powers).
TMS320C24x Dead-Band separates the transition edges of two signals: output and complemented output, by a time interval. This time interval is programmable. The Dead-Band can only be used with Full Compare Output.
Full compare has two outputs per channel, a “true” phase and a “false” phase . These exits allow the device to directly drive the upper and the lower halves of an H-bridge. To accommodate any combinations of transistor types and polarities in the H-bridge, the state of the outputs in the ACTIVE versus INACTIVE time slots are programmable. Therefore, it does not necessarily follow that, in the dual output compare channels, the true and false phase outputs are electrically complementary. Furthermore, it is also not true that when one output is ACTIVE, the other is INACTIVE.

The key point to remember is:

- Both “true” and “false” phase outputs use the same definition for ACTIVE vs. INACTIVE time slots. The electrical state of the output pins will be determined by the value programmed in the appropriate ACTION register (ACTR) for the ACTIVE state.

In fact, the only distinguished feature between the true and false outputs is the generation of the dead band time. Dead-Band generation is accomplished by digitally counting a programmable number of cycles between the generate edges on the true and false outputs due to the a compare trigger event. The delay generated starts when the compare event happens.

The rules for Dead-Band generation are:

- When a compare event happens to enter the ACTIVE time slot of the PWM cycle, the FALSE output changes from the INACTIVE state to the ACTIVE

state immediately. The TRUE output waits for the dead-band time before changing from its INACTIVE to ACTIVE state.

- When a compare or period occurs to enter the INACTIVE time slot of the PWM cycle, the TRUE side output changes from the ACTIVE state to the INACTIVE state immediately, while the FALSE side output changes after the dead-band time.
- If the time slot definition is reset to INACTIVE on an underflow event (symmetric only), both outputs go to the INACTIVE state immediately, no dead-band is generated.

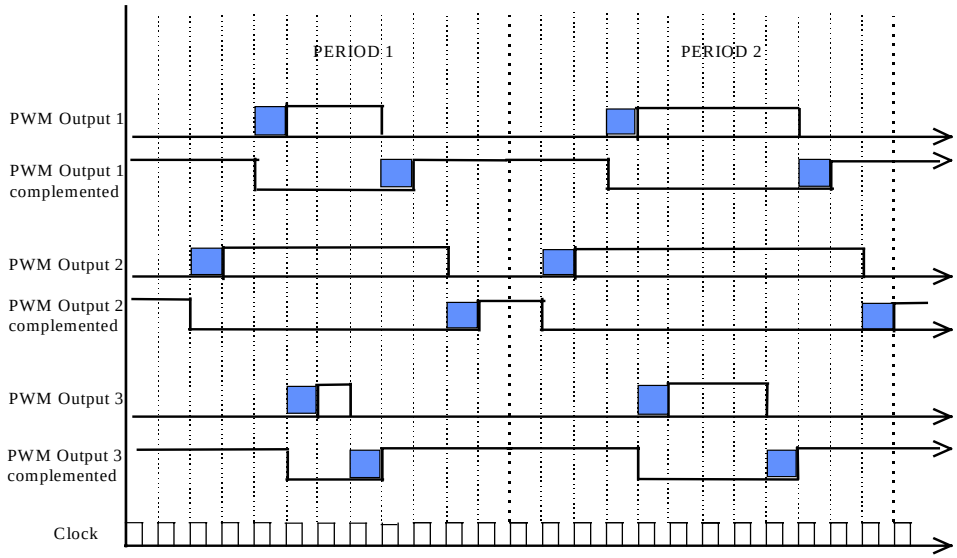
Index

1. Possibilities of Dead-Band Generator

The Dead-Band Generator associated with the General Purpose Timer One can be used:

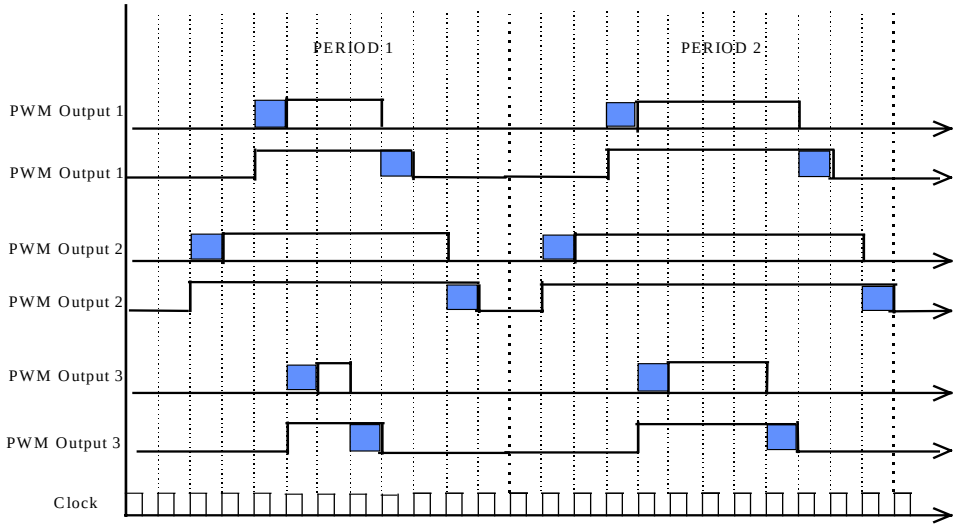
- To generate three symmetrical PWM plus three complemented PWM with Dead-Time on the Full Compare output:

In this example, all Dead-Band values are the same for all PWM.

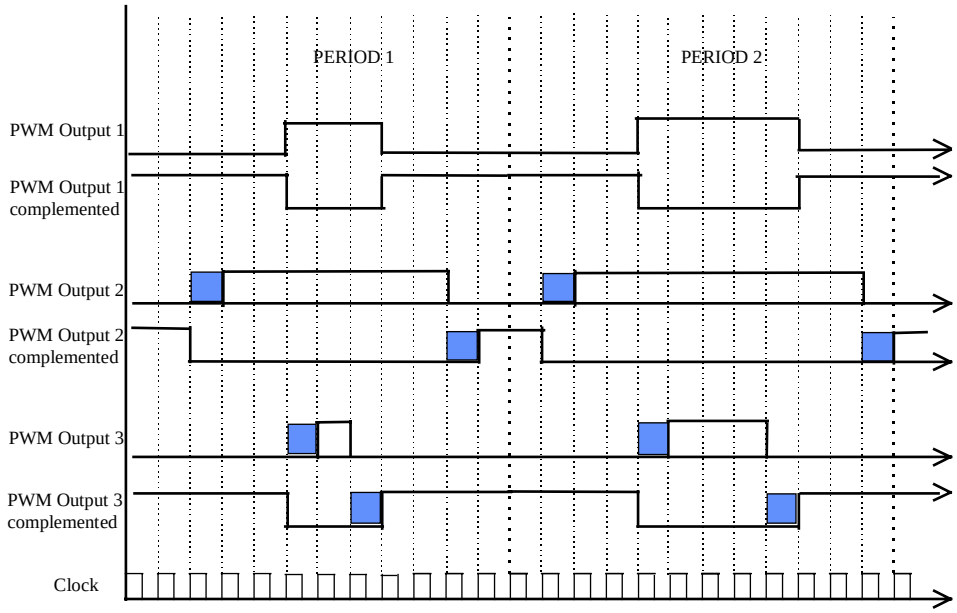


- To generate three symmetrical PWM plus three PWM with Dead-time on the Full Compare output:

In this example, all Dead-Band values are the same for all PWM.



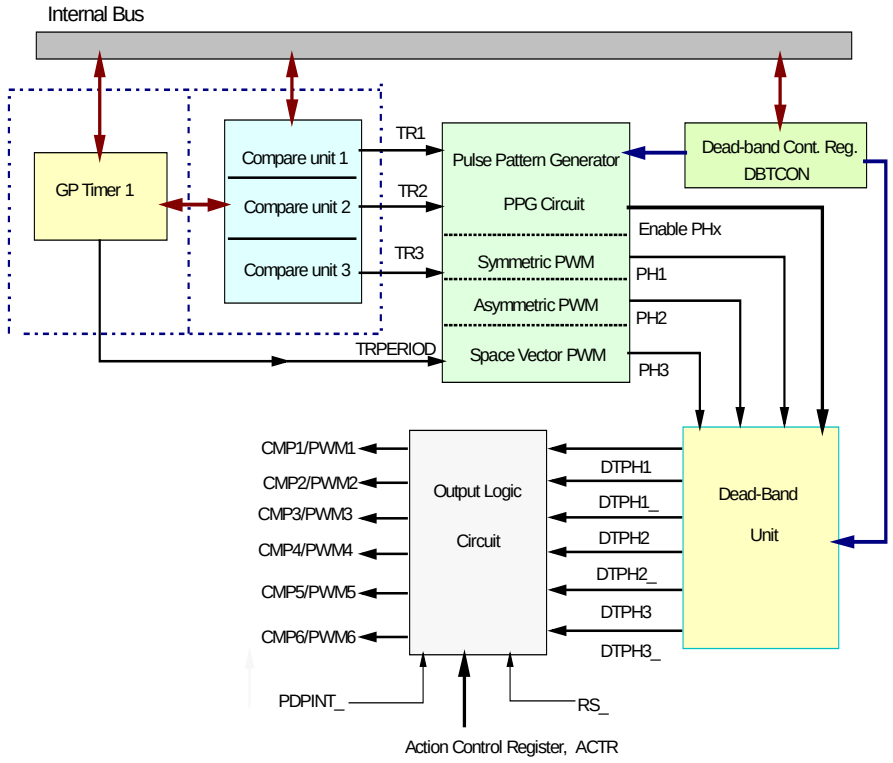
- To generate three symmetrical PWM plus three complemented PWM with Dead-time on the Full Compare output, Dead-band is enable on Phase Two and Phase Three but is disable on Phase One:



2. Description: Event Manager Programming

2.1 Connection of Dead-Band Units in the Event Manager

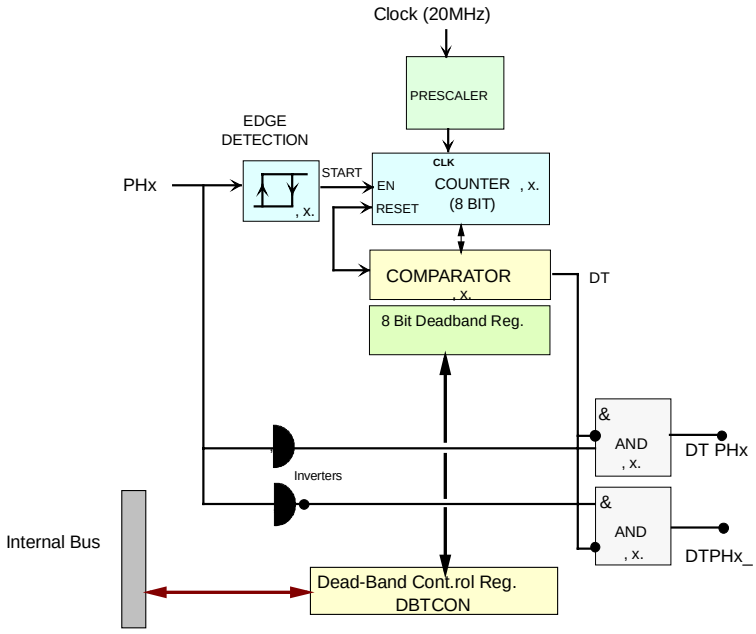
The PWM circuit associated with full compare units make it possible for the generation of 6 PWM output channels that have programmable Dead-Band and programmable output polarity.



Three pairs PWM (Full Compare) are exclusively based on the Time Base One.

- **Complemented PWMs with Dead-Band**, signals will be opposite of each other with a time interval which separate transition edges.
- All PWM combinations, each output pin of pairs PWM can be programmed by user software using Output Logic Circuit.

2.2 Dead-Band Unit Composition



2.3 Preparation Phase to Configure the Full Compare Units with Dead-Band

Two main modules have to be proposed to generate three pairs PWM with Dead-band:

- Full Compare Units programming:
  - to write ACTR : Action Control Register which controls the action on each of 6 compare output pins.
  - to write CMPR1 : Compare register 1
  - to write CMPR2 : Compare register 2
  - to write CMPR3 : Compare register 3
  - to write DBTCON : Dead-Band Timer Control Register
  - to write COMCON : Compare Control Register

Timer Base generation with General Purpose Timer 1:
CF Application not "TMS320C24x General Purpose Timer 1 in symmetrical mode"

- to write TPR1 : Timer Period register.
- to write TCNT1 : Counter register initialization.
- to write TCON1 with bit 6=0b (timer disable)
  : Control register to program Count Mode Selection, Clock Pre-scaler, Clock Source, compare reload condition, enable compare operation.
- to write TCON1 with bit 6=1b to start the timer.
  : Control register to enable the Timer 1

2.4 Example

Generation of three pairs PWM, each pair has an output and a complemented output with a 50ns Dead-Band, PWM are symmetrical.

- Free run, no emulation mode.
- Timer count mode in Continuous Up/Down-Count Mode : symmetrical PWM
- No timer input pre-scaler and internal clock.
- Reload the Full Compare shadow compare register when counter = 0.
- PWM output Active High for uneven output and Active Low for even output.
- dead-band 50ns for each phase
- Period 5 * 2 * 50ns.

Register programming:
CF Application note "TMS320C24x PWM Full Compare in symmetric mode" for compare gneration.

```
ACTR          =  0666h
                 Bit 1&0      :10b  ,Active High for output 1
                 Bit 3&2      :10b  ,Active Low for output 2
                                    (output 1 complemented)
                 Bit 5&4      :10b  ,Active High for output 3
                 Bit 7&6      :10b  ,Active Low for output 4
                                    (output 3 complemented)
                 Bit 9&8      :10b  ,Active High for output 5
                 Bit 11&10    :10b  ,Active Low for output 6
                                    (output 5 complemented)
```

```
DBTCON        =  02e0h
                 Bit 3&4      ;00b  ,Dead-Band Pre-scaler is x/1
                 Bit 5        :1b   ,Enable Dead-Band Phase 1
                 Bit 6        :1b   ,Enable Dead-Band Phase 2
                 Bit 7        :1b   ,Enable Dead-Band Phase 3
                 Bit 8-15     :01h  ,Dead-Band value is 2 DSP
                                     Clock.
CMPR1         =  3h
CMPR2         =  2h
CMPR3         =  4h

COMCON(1)      = 0307h
                 Bit 0        :1b   ,PWM mode for PWM2 and PWM1
                 Bit 1        :1b   ,PWM mode for PWM4 and PWM3
                 Bit 2        :1b   ,PWM mode for PWM6 and PWM5
                 Bit 9        :1b   ,Full Compare output are
                                     enabled.
                 Bit 11&10    :00b  ,Reload Compare register at
                                     TCNT1=0.
COMCON(2) =8307h
                 Bit 15       :1b   ,Enable Compare operations
```

CF Application note "TMS320C24x General Purpose Timer 1 symmetric mode" for time base generation

```
TPR1          =  5h
TCMPR1        =  3h
TCNT1         =  0h
TCON1 (first) =  a802h
                 Bit 1        : 1b  , Enable timer compare
                                     operation.
                 Bit 3&2      : 00b , Compare Register reload
                                     when counter is zero.
                 Bit 5&4      : 00b , Internal Clock source
                                     select.
                 Bit 6        : 0b  , Timer 1 Disabled and pre-
                                     scaler reset.
                 Bit 13,12&11 : 101b   , Continuous-Up/Down
                                     Count Mode.
                 Bit 15&14    : 10b , GP timer not affected by
                                     emulation suspend.
TCON1 (second) = a842h
                 Bit 6        : 1b  , Timer 1 is enabled.
```

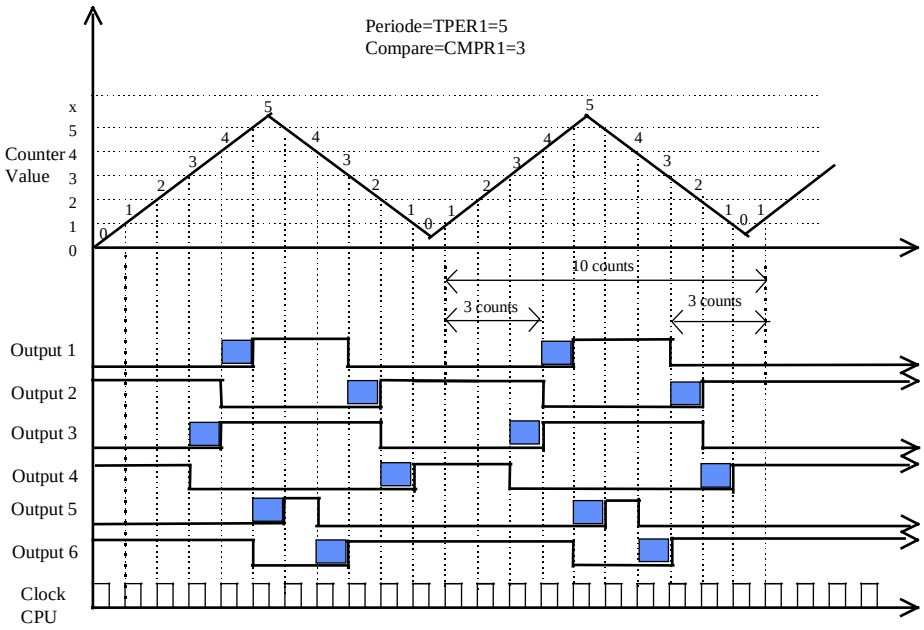
Initialization Assembly code:

```
        ;Note : registers are memory mapped.

  GPTCON .set   7400h     ;General Timer Controls
  TCNT1  .set   7401h     ;T1 Counter Register
  TPR1   .set   7403h     ;T1 Period Register
  TCON1  .set   7404h     ;T1 Control Register
  COMCON .set   740dh     ;Compare Control Register
  ACTR   .set   740eh     ;Full Compare Action Register
  DBTCON .set   7410h     ;Dead-Band Timer control register
  CMPR1  .set   7411h     ;Full Compare unit Compare register 1
  CMPR2  .set   7412h     ;Full Compare unit Compare register 1
  CMPR3  .set   7413h     ;Full Compare unit Compare register 1

         LDP    #232
         SPLK   #666h,ACTR
         SPLK   #1e0h,DBTCON
         SPLK   #3h,CMPR1
         SPLK   #2h,CMPR2
         SPLK   #4h,CMPR3
         SPLK   #307h,COMCON
         SPLK   #8307h,COMCON
         SPLK   #5h,TPR1
         SPLK   #0h,TCNT1
         SPLK   #0a802h,TCON1
         SPLK   #0a842h,TCON1
```

Result of this example



2.5 Boundary Conditions for Dead-Band Generator

The Dead-Band module is totally secure. In case the Dead-time value is equal or greater the active width or is more than periode boundary, the two phases stay complemented all the time.

Example with a 150ns Dead-Time