TMS320C24x PWM Simple Compare in Symmetric Mode

Application Report
SPRA370

TEXAS INSTRUMENTS

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Overview

Three simple Compare Units can generate up to 3 PWM. The Time base for Simple Compare Unit is provided by the General Purpose Timer 1 or General Purpose Timer 2. The Simple Compare Module can be used in parallel with the Full Compare module and generate 3 additional phases with an independent time base. There is no possibility to generate complemented output with Simple Compare Output.

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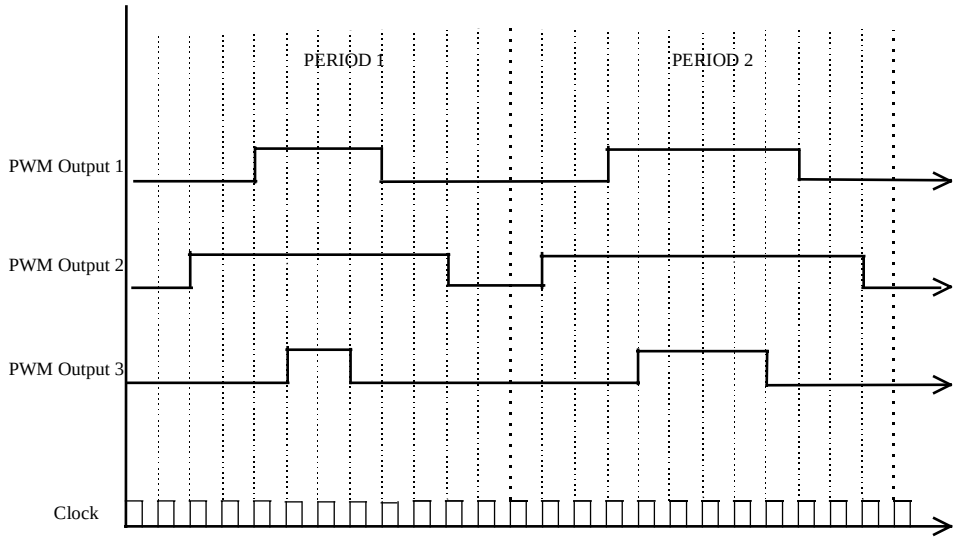
1. Possibilities of PWM Simple Compare in Symmetric Mode

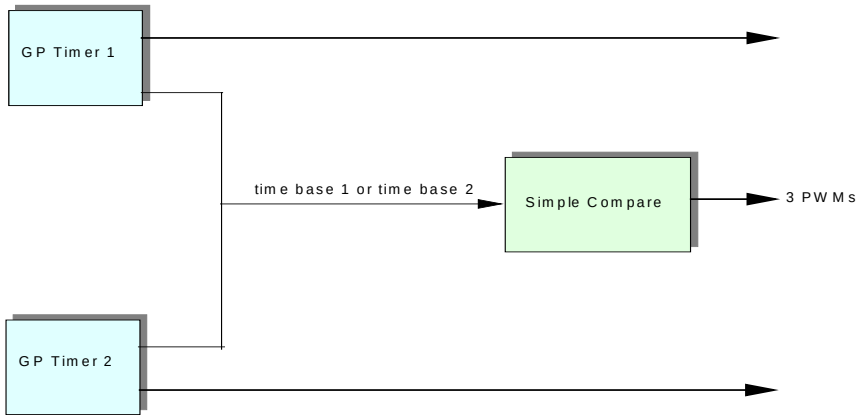
Simple Compare in symmetric mode can be used:

- To generate **three symmetrical PWMs** on the Simple Compare output

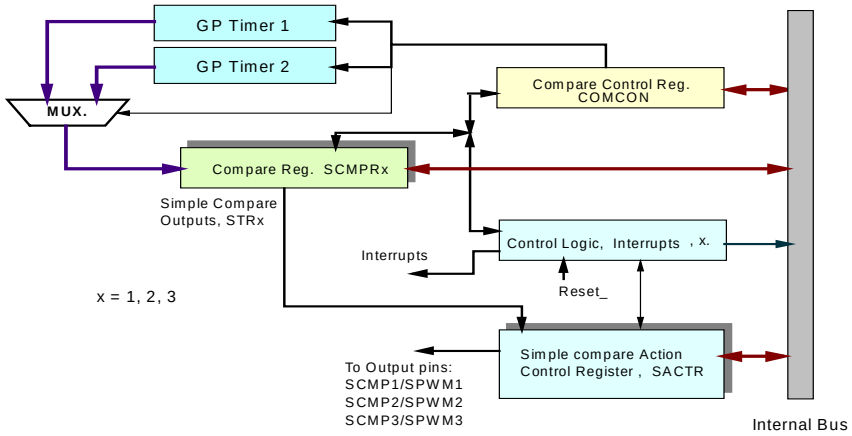


2. Description: Event Manager Programmation

Simple Compare Units connected to time base generation architecture



2.1 Simple Compare Unit Composition



2.2 Preparation Phase to Configure the Three Simple Compare Units

Two main modules have to be programmed to generate three simple compare:

- Simple Compare Units programmation:
  - to write SACTR : Action Control Register which controls the action on each of 6 compare output pins.
  - to write SCMPR1 : Compare register 1
  - to write SCMPR2 : Compare register 2
  - to write SCMPR3 : Compare register 3
  - to write COMCON : Compare Control Register

- Timer Base generation with General Purpose Timer 1: *CF Application note "TMS320C24x General Purpose Timer 1 in symmetrical mode"*
  - to write TPR1 : Timer Period register.
  - to write TCNT1 : Control register initialisation.
  - to write TCON1 with bit 6=0b (timer disable) : Control register to program Count Mode Selection, Clock Pre-scaler, Clock Source, compare reload condition, enable compare operation.
  - to write TCON1 with bit 6=1b to start the timer. : Control register to enable the Timer 1

2.3 Example

Generation of three symmetrical PWM.

- Free run, no emulation mode.
- Timer count mode Continuous Up/Down-Count Mode : symmetrical PWM.
- No timer input pre-scaler and internal clock.
- Reload the Simple Compare shadow compare register when counter equal 0.
- PWM output Active High for uneven output and Active Low for even output.

- Period 5 * 2 * 50ns.

Register programming:

```
SACTR          =  2ah
                  Bit 1&0   :10b  ,Active High for output 1
                  Bit 3&2   :10b  ,Active High for output 3
```

```
                  Bit 5&4   :10b  ,Active High for output 5
SCMPR1         =  3h
SCMPR2         =  2h
SCMPR3         =  4h

COMCON(1)      =  0100h
                  Bit 4&3   :00b  ,Simple Compare action (SACTR)
                  Bit 6&5   :00b  ,Simple Compare registers
                                  reload condition : TCNT1=0
                  Bit 7     :0b   ,Simple Compare time base
                                  selects : GPTimer1
                  Bit 8     :1b   ,Simple Compare output are
                                  enabled.
COMCON(2)      =  8100h
                  Bit 15    :1b   ,Enable Compare operations
```

CF Application note "TMS320C24x General Purpose Timer 1 in symmetrical mode" for time base generation

```
TPR1           =  5h
TCMPR1         =  3h
TCNT1          =  0h
TCON1 (first)  =  a802h
                  Bit 1         : 1b   , Enable timer compare
                                         operation.
                  Bit 3&2       : 00b  , Compare Register reload
                                         when counter is zero.
                  Bit 5&4       : 00b  , Internal Clock source
                                         select.
                  Bit 6         : 0b   , Timer 1 Disabled and pre-
                                         scaler reset.
                  Bit 13,12&11: 101b   , Continuous-Up/Down Count
                                         Mode.
                  Bit 15&14     : 10b  , GP timer not affected by
                                         emulation suspend.
TCON1 (second) = a842h
                  Bit 6         : 1b   , Timer 1 is enabled.
```

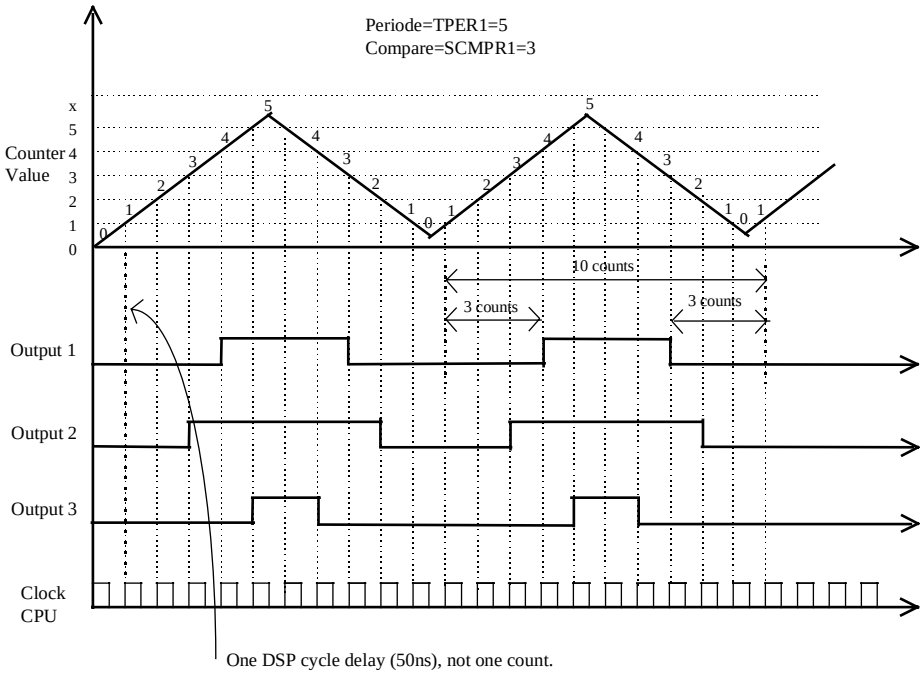
Initialisation Assembly code:

```
GPTCON .set   7400h     ;General Timer Controls
TCNT1  .set   7401h     ;T1 Counter Register
TPR1   .set   7403h     ;T1 Period Register
TCON1  .set   7404h     ;T1 Control Register
COMCON .set   740dh     ;Compare Control Register
SACTR  .set   740fh     ;Full Compare Action Register
SCMPR1 .set   7414h     ;Full Compare unit Compare register 1
SCMPR2 .set   7415h     ;Full Compare unit Compare register 1
```

```
SCMPR3 .set   7416h     ;Full Compare unit Compare register 1

        LDP    #232
        SPLK   #2ah,SACTR
        SPLK   #3h,SCMPR1
        SPLK   #2h,SCMPR2
        SPLK   #4h,SCMPR3
        SPLK   #100h,COMCON
        SPLK   #8100h,COMCON
        SPLK   #5h,TPR1
        SPLK   #0h,TCNT1
        SPLK   #0a802h,TCON1
        SPLK   #0a842h,TCON1
```

Result of this example



Note: the first period of a continuous up/down count is 1 DSP cycle longer and is not totally symmetrical (see diagram above).

2.4 Modification of the active width during running

When new compare values in the Full Compare registers are written, new values are loaded in a shadow register and are active at the end of the period, when TCNT1=0 (for this configuration).

Example:
SCMPR1 switch from 3 to 4 during the second period
SCMPR2 switch from 2 to 3 during the second period
SCMPR3 stays at the same value

Results will be: