Practical Considerations in High Performance MOSFET, IGBT, and MCT Gate Drive Circuits

by Bill Andreycak

TOPIC 6

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Introduction:

The switchmode power supply industry trend towards higher conversion frequencies is motivated by the desire to achieve higher power densities. As switching frequencies push towards and beyond 1 MHz, MOSFET transition periods can become a significant portion of the total switching period. Losses associated with voltage and current overlap during switching transitions not only degrade power supply efficiency, but warrant consideration from both a thermal and packaging standpoint. Although brief, each of the MOSFET switching transitions can be further reduced if driven from a high speed, high current totem-pole driver.

Inadequate gate drive is generally the result of underestimating the effective load of a power MOSFET upon its driver.

General Applications of Power MOSFETs

Effective Gate Capacitance: MOSFET input capacitance (C_{ISS}) is frequently misused as the load represented by a power MOSFET to the gate driver IC. In reality, the effective input capacitance of a MOSFET (C_{EFF}) is much higher, and must be derived from the manufacturers' published total gate charge (Q_G) information. Even the specified maximum values of the gate charge parameter do not accurately reflect the driver's instantaneous loads during a given switching transition. Fortunately, FET manufacturers provide a curve for the gate-to-source voltage (V_{GS}) versus total gate charge in their data sheets. This will be segmented into four time intervals of interest per switching transition. Each of these will be analyzed to determine the effective gate capacitance and driver requirements for optimal performance in a clamped inductive load (Buck derived) application.

Total Gate Charge (Q_G): First, a typical high power MOSFET "Gate Charge versus Gate-to-Source Voltage" curve will be examined. An IRFP460 device has been selected and this curve is applicable to most other MOSFET devices by adjusting the gate charge numbers accordingly. Both turn-on and turn-off transitions are shown with the respective drain currents and drain-to-source voltages.

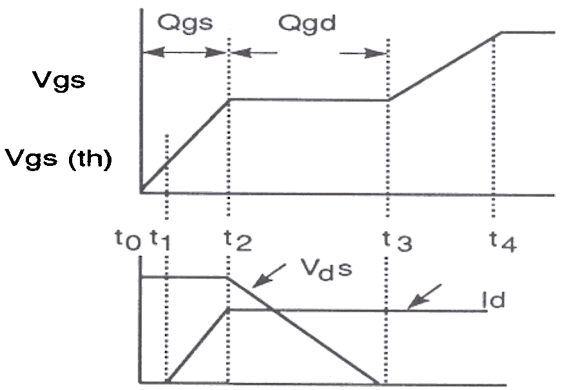

Fig 1. - Turn-On Waveforms
Gate voltage vs. time

Interval t_0-t_1: The time required to bring the gate voltage from zero to its threshold $V_{GS(th)}$ can be expressed as a delay time. Both the voltage across the switching device and current through it are unaffected during this interval.

Interval t_1-t_2: This period starts at time t_1 when The gate voltage has reached $V_{GS(th)}$ and drain current begins to flow. Current continues to rise

until essentially reaching its final value at time t_2. While this occurred, the gate to source voltage had also been increasing. The drain-to-source voltage remains unchanged at $V_{DS(off)}$. Power in the MOSFET is wasted by the simultaneous overlap of voltage and current.

Interval t_2-t_3: Beginning at time t_2 the drain-to-source voltage starts to fall which introduces the "Miller" capacitance effects (C_{GD}) from the drain to the MOSFET gate. The result is the noticeable plateau in the gate voltage waveform from time t_2 until t_3 while a charge equal to Q_{GD} is admitted. It is here that most drive circuits are taxed to their limits. The interval concludes at time t_3 when the drain voltage approaches its minimum.

Interval t_3-t_4: During this final interval of interest the gate voltage rises from the plateau of the prior region up to its final drive voltage. This increasing gate voltage decreases $R_{DS(on)}$, the MOSFET drain-to-source resistance. Bringing the gate voltage above 10 - 12V, however, has little effect on further reducing $R_{DS(on)}$.

SUMMARY OF TURN-ON WAVEFORMS AND DRIVER LIMITATIONS

Intrvl	$V_{GS(t)}$	$I_{D(t)}$	$V_{DS(t)}$	Driver Limitation
t_0-t_1	0-threshold	0	$V_{DS(off)}$	Slew rate (dv/dt)
t_1-t_2	thrs-plateau	rising	$V_{DS(off)}$	Slew rate (dv/dt)
t_2-t_3	V(plateau)	$I_{ON(dc)}$	falling	Peak current I(max)
t_3-t_4	rising	$I_{ON(dc)}$	I_{ON}*$R_{DS(t)}$	Peak I, dv/dt

The intervals during turn-off are basically the same as those described for turn-on, however the sequence and corresponding waveforms are reversed:

Interval t_4-t_3: The beginning of the turn-off cycle can be described as a delay from the final drive voltage ($V_{GS(on)}$) to the plateau region. Both the drain voltage and current waveforms remain unchanged while the effective resistance ($R_{DS(on)}$) increases as the gate voltage decreases.

Interval t_3-t_2: Once the plateau is reached at time t_3, the gate voltage remains constant until time t_2. Gate charge due to the Miller effect is being removed, an amount equal to Q_{GD}. The drain voltage rises to its off state amplitude, $V_{DS(off)}$, while the drain current continues to flow and equals I(on). This lossy transition ends at time t_2.

Interval t_2-t_1: Once the Miller charge is completely removed, the gate voltage is reduced from the plateau to the threshold voltage causing the drain current to fall from I_{ON} to zero. Transition power loss ends at time t_1 when the gate threshold is crossed.

Interval t_1-t_0: This brief period is of little interest in the turn-off sequence since the device is off at time t_1.

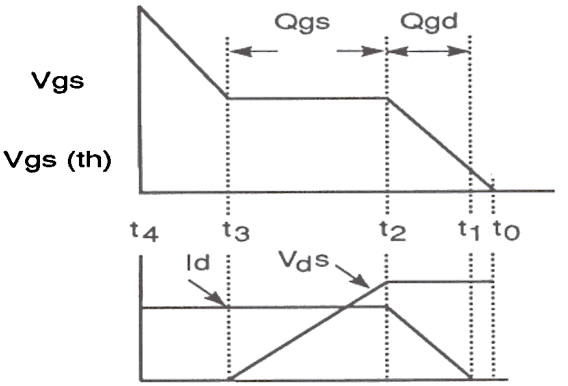

Fig 2. Turn Off Waveforms

SUMMARY OF TURN-OFF WAVEFORMS AND DRIVER LIMITATIONS

Intrvl	$V_{GS(t)}$	$I_{D(t)}$	$V_{DS(t)}$	Driver Limitation
t_4-t_3	falling	$I_{ON(dc)}$	I_{ON}*$R_{DS(t)}$	Peak I and dv/dt
t_3-t_2	V(plateau)	$I_{ON(dc)}$	falling	Peak Current I(max)
t_2-t_1	Vplat-thrsh	falling	$V_{DS(off)}$	Slew rate (dv/dt)
t_1-t_0	thrsh-0	0	$V_{DS(off)}$	Slew rate (dv/dt)

FET Transition Power Loss: During each of the FET turn-on and turn-off sequences power is lost due to the simultaneous overlap of drain-source voltage and drain current. Since FET voltage and current are both externally controlled by the application, the driver IC can reduce power loss by making the transition times as brief as possible. Minimizing switching losses simply requires a competent driver IC, one able to provide high peak currents with high voltage slew rates.

A review of the prior transition waveforms indicates that power is lost between times t_1 to t_3. While t_2 serves as the pivot point for which waveform is rising or falling, the equations show that t_2 is irrelevant in the power loss equation. For the purpose of brevity, the waveform of interest can be approximated as a triangle while the other waveform is constant. The t_1 to t_3 interval can then be defined as the net transition time, $t_{TRANSITION}$, with a conversion period of t_{PERIOD}.

During the two intervals from t_1 to t_3:

$$P_{LOSS} = \frac{I_{ON} V_{ds(off)} (t_2 - t_1)}{2\ t_{PERIOD}}$$

$$= \frac{V_{ds(off)} I_{ON} (t_3 - t_2)}{2\ t_{PERIOD}}$$

Combining the two equations with $t_{TRANSITION} = t_3 - t_1$ results in a net loss of :

$$P_{LOSS} = \frac{I_{ON} V_{ds(off)} (t_2 - t_1)}{2\ t_{PERIOD}}$$

Since these losses are incurred twice per cycle, first at turn-on and then again at turn-off, the net result is a doubling of the power loss.

$$P_{LOSS} = \frac{V_{ds(off)} I_{ON} t_{(trans)}}{t_{PERIOD}}$$

This relationship displays the need for fast transitions at any switching frequency, and is of significant concern at one megaHertz. Minimization of the FET transition power loss can be achieved with high current drivers.

Gate Charge: Each transition interval has an associated gate charge which can be derived from the FET manufacturers data sheets. Since there are three basic shapes to the V_{GS} curve, the interval from t_0 to t_1 can be lumped together with t_1 to t_2. For most large FET geometries, the amount of charge in the t_0-t_1 span is negligible anyway. This simplification allows an easy calculation of the effective gate capacitance for each interval along with quantifying the peak current required to traverse in a given amount of time.

Charge can be represented as the product of capacitance multiplied by voltage, or current multiplied by time. The effective gate capacitance is determined by dividing the required gate charge (Q_G) by the gate voltage during a given interval. Likewise, the current necessary to force a transition within a specified time is obtained by dividing the gate charge by the desired time.

$$\text{Effective } C_{GS} = \Delta Q_G / \Delta V_{GS}$$

$$\text{Required } I_G = \Delta Q_G / t_{TRANSITION}$$

A "large" industry standard FET, the IRFP460 device, will be used for an example of the actual gate charge requirements over several intervals. First, the effective capacitance over the typical gate drive voltage of 0 - 10V will be determined. Typical gate to source voltage verses gate charge is shown in the figure below.

As V_{GS} is varied from 0 to 10 Volts:

$$\text{Effective } C = \Delta Q_G / \Delta V_{GS} = 120nC / 10V = 12nF$$

Notice that the effective load of 12 nanoFarads is approximately three times greater than the FET input capacitance, C_{ISS}, specified as 4.1nF.

The average, or effective capacitance can also be somewhat misleading if used as the driver's load. This can best be demonstrated by the plateau in the gate voltage waveform where the voltage is virtually constant yet charge is induced. This indicates that the gate capacitance during this period is extremely high.

Gate charge, which dictates the driver requirements and obtainable transition times will be determined over the three regions of interest.

From t_0 to t_2:

$$\Delta Q_{GS} = 20nC\ ;\quad \Delta V_{GS} = 6V$$

Here, the effective capacitance can be calculated as 20nC/6V or 3.3nF, slightly lower than C_{ISS}. During this period the driver IC is generally slew rate limited, unable to provide a high enough dv/dt to become peak current limited. The exact process used by the manufacturer and the resulting transistor speeds can be approaching their maximums.

During the plateau region from t_2 to t_3:

$$\Delta Q_{GD} = 0;\quad \Delta V_{GS} \text{ is 0 (approx)}$$

The effective capacitance is difficult to calculate given these conditions, but is quite substantial. Of more importance is the peak driver current which governs the duration of the "Miller" plateau region

and fall time of the drain voltage. Since charge also equals current multiplied by time ($Q=I\cdot t$), the necessary gate current can be determined based on a desired drain fall time. Likewise, the achievable drain voltage fall time can be determined based upon peak driver current.

$$I_{G(max)} = \Delta Q_{GD(plateau)} / t_{(Vds\ fall)}$$

$$t_{(Vds\ fall)} = \Delta Q_{GD(plateau)} / I_{(max)\ driver}$$

The final area of interest is from t_3 to t_4 where ΔQg equals 40nC and the gate voltage rises by about 4 Volts. Here the interval capacitance of 10nF approaches that of the average value of 12nF for the entire turn-on or turn-off interval.

In many applications using large FETs, the peak driver current dominates as the limiting factor in obtaining rapid MOSFET transition speeds.

Gate Drive Power Considerations: Perhaps the most popular misconception in the power supply industry is that a FET gates require NO power from the auxiliary supply - that both turn-on and turn-off are miraculously power free. Another fallacy is that the driver consumes all the measured supply current, Icc, and none of it is used to transition the gates. Obviously, both of these statements are false.

In reality, the power required by the gate itself can be quite substantial in high frequency applications. Calculation of this begins by listing the specified total gate charge for the FET device, Q_G. The gate power utilized in charging and discharging a capacitor at frequency "F" is:

$$P_{CAP} = C\cdot V^2\cdot F$$

Substituting the gate charge for capacitance multiplied by voltage ($Q=C\cdot V$) in this equation results in :

$$P_{GATE} = Q_G\cdot V\cdot F$$

Typical gate power required versus FET size and switching frequency is tabulated in Table 1. The corresponding driver input current at a nominal 12 Volt bias is shown in Table 2.

Table 1 - GATE POWER (mW) vs. SWITCHING FREQUENCY AND FET SIZE

	SWITCHING FREQUENCY(KHZ)							
	50	100	150	200	250	500	750	1MHZ
Size 1	10	18	28	36	46	90	136	180
Size 2	16	30	46	60	76	153	226	300
Size 3	28	54	82	108	136	275	406	504
Size 4	48	96	144	192	240	480	720	960
Size 5	100	200	300	400	550	1.0W	1.5W	2W
Size 6	144	288	432	576	720	1.4W	2W	>2W

Table 2 - DC SUPPLY CURRENT (mA) vs. SWITCHING FREQUENCY AND FET SIZE

	SWITCHING FREQUENCY (KHZ)							
	50	100	150	200	250	500	750	1MHZ
Size 1	1	1	2	4	5	6	10	12
Size 2	1	2	4	5	6	10	16	20
Size 3	2	4	6	8	10	16	26	36
Size 4	4	8	10	12	16	32	48	64
Size 5	8	14	20	26	32	66	100	130
Size 6	10	20	28	38	48	96	144	190

Driver Considerations

As previously demonstrated, the ideal MOSFET gate drive IC is a unique blend of both high speed switching and high peak current capability. Initially, the high speed is required to bring the gate voltage from zero to the plateau, but the current is low. Once the plateau is intersected, the driver voltage is fairly constant, and the IC must switch modes. Instantly, the driver current snaps to its maximum as charge is injected to overcome the FET's Miller effects. Finally, a combination of both high slew rate and high current is needed to complete the gate drive cycle.

At turn-off this sequence is reversed, first demanding both high slew rate and high current simultaneously. This is followed by the plateau region which is limited only by the maximum driver current. Finally, there is high speed discharge of the gate to zero Volts. Optimization of a driver for this type of application can be difficult. In general, the MOSFET driver IC output stage is designed to switch as fast as the manufacturer's process will allow.

Cross Conduction: There are numerous tradeoffs involved in the design of these drivers beyond the obvious choices of number of outputs and peak current capability. Cross-conduction is defined as the conduction of current through both of the totem pole transistors simultaneously from Vin to ground. It is an unproductive loss in the output stage which results in unnecessary heating of the driver and wasted power. Cross conduction is the result of turning one transistor ON before the opposing one is fully off, a compromise often necessary to minimize the input to output propagation delays.

An interesting observation is that cross-conduction is less of a concern with large capacitive loads (FETs) than with unloaded or lightly loaded driver outputs. Any capacitive load will reduce the slew of the output stage, slowing down its dv/dt. This causes a portion of the cross conduction current to flow from the load, rather than from the input supply through the driver's opposite output transistor. The power loss associated with a driver's inherent cross-conduction is unchanged with large capacitive loads, however it is not caused by a "shoot-through" of supply current.

Driver Performance: There are a variety of applications for MOSFET drivers - each with its own unique set of speed and peak current requirements. Most general purpose drivers feature 1.5 amp peak totem-pole outputs which deliver rise and fall times of approximately 40nsec into 1 nF. Propagation delays are in the vicinity of 40 to 50 nsec, making these devices quite adaptable to numerous power supply and motor control applications. These specifications can be used for a comparison to those of a new series of higher speed and higher current devices: the UC1708, UC1710 and the UC1711 power MOSFET drivers. Each member in this group of 3rd generation driver ICs features significant performance improvements over their predecessors with one parameter optimized for a specific set of applications.

Propagation delays: The trend towards higher power densities has thrust switching frequencies well beyond 1MHz in many low to medium power systems. With a one microsecond or less total conversion period, the FET switching transitions should be in the order of low tens of nanoseconds to yield high efficiency. Also, the propagation delays from the driver input to output should be around ten nanoseconds for quick response.

Table 3 - MOSFET DRIVER IC
FEATURE AND PERFORMANCE OVERVIEW

	UC1708	UC1710	UC1711
Number of outputs	2	1	2
Peak output current (per output)	3A	6A	1.5A
Noninverting input-output logic	✓	✓	
Inverting input-output logic	✓	✓	
Maximum supply voltage Vcc	35V	20V	40V
Typical supply current Icc (1)	16mA	30mA	17mA
Remote Enable	✓		
Shutdown Input	✓	✓(2)	
Separate signal, power grounds	✓(3)	✓(3)	
Separate Vin and Vc pins		✓(3)	
8 pin DIL package	✓	✓	✓
16 pin DIL package	✓	✓	✓
5 pin TO-220 package		✓	

Note 1. Typical Vc plus Vcc current measured at 200KHZ, 50% duty cycle and no load
Note 2. Using the device's other input
Note 3. Package dependent

Thermal Considerations: The driver output stage can be modeled as a resistance to the respective auxiliary supply rail driving an ideal FET capacitor. All of the energy used to charge and discharge the MOSFET gate capacitor is converted into heat by the driver. This gate power loss adds to the driver's own power loss - resulting in a net driver power dissipation equal to its input voltage, Vcc, multiplied by the sum of the gate and driver currents, I_G + Icc. This can be calculated or determined empirically by measuring the driver DC input voltage and current.

Proper IC package selection and/or device heat sinking is the only method available to insure a safe operating junction temperature, T_J. All IC's are specified and graded into junction temperature ranges, and priced accordingly. It should be noted that using a device outside its tested and rated temperature range can result in poor performance, parameters out of specifications, and quite possibly—no operation at all.

Junction Temperature: The junction temperature of the driver IC is obtained by first calculating the device thermal rise above the ambient temperature. This is obtained by multiplying the average input power ($V_{IN} \cdot I_{IN}$) by the device free air thermal impedance, Θ_{JA}. This term is then added to the ambient temperature to yield the resulting junction temperature, T_J.

If the driver is thermally attached to a heat sink or "cold plate", then the thermal impedance from the device junction to it's package case, Θ_{JC}, is used to determine the thermal rise. Likewise, this thermal rise is added to the heat sink temperature to determine the junction temperature. In either case, the maximum junction temperature, $T_{J(max)}$, should be determined and checked against the device absolute maximum specification.

Average supply currents of the driver ICs vary primarily with the switching frequency. A rough approximation of 25mA will be used as the driver supply current, regardless of the specific device utilized and switching frequency. A typical supply voltage of 12V will be used which results in a power dissipation of 300mW, excluding any contribution by the gate charging/discharging power.

The calculated gate power of Table 1 has been added to the estimated 300mW driver power to formulate Table 4 - the total driver power dissipation. This is of particular interest in selecting a driver package (8 pin, TO-220, etc) and heat sink determination for a specific maximum junction temperature, or rise. Typical junction temperature rises vs. frequency and FET size for a IC package, and recommendations are shown in Table 5.

Table 4 - AVERAGE POWER DISSIPATION (mW) vs. FREQUENCY AND SIZE

	SWITCHING FREQUENCY (KHZ)							
	50	100	150	200	250	500	750	1MHZ
Size 1	310	318	328	336	346	390	436	480
Size 2	316	330	346	360	376	452	526	600
Size 3	328	354	382	408	436	570	706	840
Size 4	348	396	444	492	540	780	1.0W	1.3W
Size 5	400	500	600	700	800	900	1.7W	2.4W
Size 6	444	588	732	876	1.0W	1.7W	2.5W	3.1W

Table 5 -PACKAGES AND TEMPERATURE RISE

For P(diss) < or = 400mW:

<320mW = 8 pin DIL, < 40°C rise
<360mw = 8 pin DIL, < 45°C rise
<400mW = 8 pin DIL, < 50°C rise

For P(diss) > 400mW a heat sink is required:

<600mW = 8 pin DIL, <40°C rise with heat sink
<750mW = 8 pin DIL, <50°C rise with heat sink
>750mW = TO-220 Package

High Power MOSFET Applications

Many high power applications require the use of "monster" MOSFETs or several large FETs in parallel for each switch. Generally, these are low to medium frequency applications (less than 200kHz) where obtaining a low $R_{DS(on)}$ is of primary concern to minimize the DC switch loss. It is not uncommon to find two, three and even four large devices used in parallel, although some of these combinations are unlikely from a cost versus performance standpoint.

Table 6 displays the individual FET device characteristics and several popular parallel arrangements. Listed in descending order is room temperature $R_{DS(on)}$ and the total gate charge required. This will ultimately be used to determine the gate drive current in Table 7 and total power dissipation in Table 8 applications.

Table 6 - PARALLELED MOSFET CHARACTERISTICS

CONFIGURATION	RDS(ON)	Qg(nC)
1 x Size 4	0.85	63
1 x Size 5	0.40	130
1 x Size 6	0.27	190
2 x Size 4 (1)	0.425	126
3 x Size 4 (1)	0.283	189
4 x Size 4 (1)	0.213	252
2 x Size 5	0.200	260
2 x Size 6	0.135	380
3 x Size 5 (1)	0.133	390
4 x Size 5 (1)	0.100	520
3 x Size 6 (2)	0.090	570
4 x Size 6 (2)	0.068	760

Notes: 1. Consider another selection
2. Consider a "Monster" FET

Table 7 - AVERAGE SUPPLY CURRENT vs. FREQUENCY AND SELECTION

	SWITCHING FREQUENCY (KHZ)					
Configuration	25	50	75	100	150	200
1 × Size 5	31	39	45	51	65	77
2 × Size 6	35	45	53	63	83	101
3 × Size 6	39	53	69	73	91	139
4 × Size 6	45	63	82	101	139	177

Table 8 POWER DISSIPATION (mW) vs. FREQUENCY AND APPLICATION

	SWITCHING FREQUENCY (KHZ)					
Configuration	25	50	75	100	150	200
2 X SIZE 5	372	468	540	612	780	924
2 X SIZE 6	420	540	636	756	1.0W	12W
3 X SIZE 6	468	636	828	876	1.1W	1.7W
4 X SIZE 6	540	756	984	1.2W	1.7W	21W

"Homebrew" Totem-poles vs. Integrated Circuit Drivers

The prior lack of "off-the-shelf" high current or high speed drivers prompted many to design their own gate drive circuits. Traditionally, an NPN-PNP emitter follower arrangement as shown in Figure 3 was used in lower frequency applications. This noninverting configuration interfaces easily with most PWM controllers and performs adequately in many converters. Peak gate drive current does suffer from dependency on driver transistor gain, and transition times are lengthened by the "slow" PNP transistor.

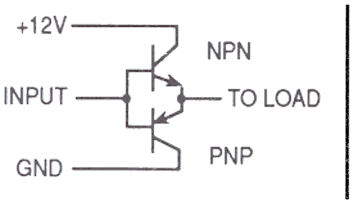

Fig 3. - Bipolar Gate Driver

The major drawback to this bipolar drive technique, however, is the potential turn-off of the drive transistors whenever the gate voltage overshoots the supply voltage rails. Any parasitic layout or wiring inductance in series with the MOSFET or IGBT gate will significantly degrade performance for two reasons. First, the inductance limits the gate drive current rate of rise to less than optimal. Second, and most consequential, is that the inductance forms a resonant L/C tank with the gate capacitance. This causes the gate voltage to overshoot during turn-on and rise above the auxiliary supply voltage which introduces two other problems. A Zener clamp must be physically located directly at the FET gate to prevent exceeding the maximum gate-to-source voltage. Also, any overshoot beyond the supply rails will reverse bias the drive transistors as either emitter rings towards the respective base voltage. This immediately turns OFF which ever drive transistor was ON and puts the drive stage into a high impedance state.

The overshoot will ring and eventually decay to an amplitude at which the drive transistor will begin to turn back on. There is a finite time involved with this process, however, depending on the transistors' speed, base drive and resonant tank period. Before the drive transistor is turned back on, the gate voltage continues to resonate closer towards its opposite state. For example, if the FET was ON, then the gate voltage continues to decrease. And if the drive transistor takes too long to turn on, it's possible for the MOSFET gate voltage to cross its "ON" gate threshold, thus turning the device OFF. Since most MOSFETS have shorter delays than the bipolar drivers, it's relatively easy to unintentionally construct a poor gate drive circuit with a discrete design. Both a zener clamp diode and a Schottky diode around each drive transistor to the rails is necessary with NPN/PNP drivers.

For higher speed applications, a P and N channel FET pair can be used as shown in Figure 4. The circuit is configured with the P channel MOS as the upper side switch to simplify the auxiliary bias. Otherwise, a gate drive potential of 10V above the auxiliary bias would required. Unfortunately, this configuration also has a few drawbacks. First, it leads to an inverting logic flow from the driver input to its output, complicating matters especially during power-up and power-down sequences. Without a clever undervoltage lockout circuit the main power switch will tend to be ON as the

auxiliary supply voltage is raised or lowered while the PWM is OFF.

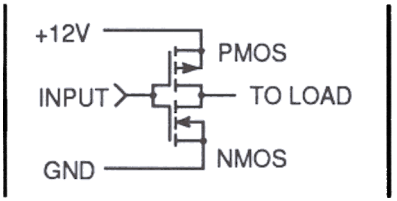

Fig 4. - FET Gate Driver

Cross conduction of both FETs may be unavoidable with this configuration due to the difference between the gate threshold voltages of each device. Depending on the supply voltage, both P and N channel devices can cross conduct while their input drive waveform is above $V_{GS(th)}$ of the "N" device and below that of the "P" device. One technique to minimize the peak cross conduction current is to add some resistance between the FETs. While this does minimize the "shoot-through" current, it also limits the peak current available to the load. This somewhat defeats the purpose of using the MOSFETs in the first place to deliver high currents. The resistor serves an additional purpose of damping the gate drive oscillations during the transitions, minimizing the overshoot. In a practical application, two resistors can be used in the place of one with the center tap connecting to the FET gate load as shown in Figure 5.

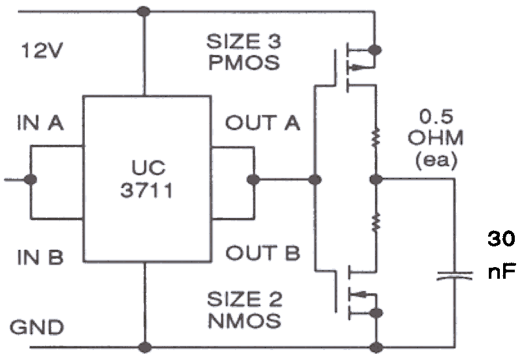

Fig 5. - FET Driver with Limiting Resistors

The performance of the circuit in Figure 5 was evaluated and compared to that of the UC1710 driver into a 30nF load, approximately equivalent to three IRFP460 devices in parallel. The discrete drive circuit utilized an IRFP930 "P" type and an IRF520 "N" channel device connected in series with two one-half ohm resistors to limit the shoot-through current. These FETs were driven from the UC1711 dual driver which can deliver 3A peak gate drive currents for rapid transitions. The performance of this circuit was compared to that of the UC1710 driver IC which has 6A capability. The test results as shown in Figure 6 indicate very similar performance into a 30nF load from either technique. Obviously, the "homebrew" approach utilizes a total of three devices in comparison to a single driver to obtain essentially the same high speed performance. Additionally, the cost of the P channel FET alone may warrant consideration, not to mention the difference in PC board real estate. As a final note, the discrete FET approach required significantly more supply current than the sole driver IC, primarily due to the higher cross conduction.

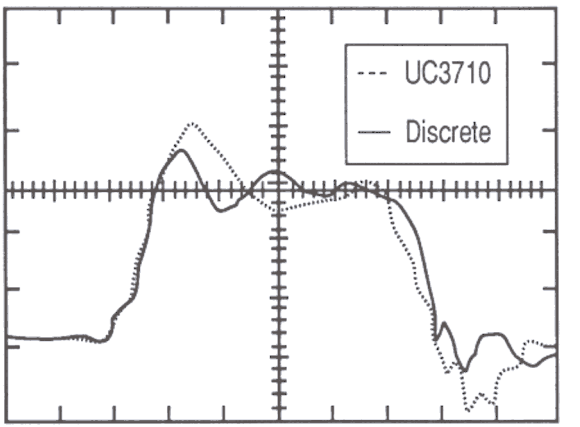

Fig 6. - Driver Performance into 30nF Load

Power Devices

IGBTs and MCTs: While existing generations of power MOSFETs continue to be enhanced for lower $R_{DS(on)}$ and faster recovery internal diodes, alternative new devices have also been introduced. Among the most popular, and viable for high voltage, high power applications are IGBTs (Insulated Gate Bipolar Transistors) and MCTs (MOS Controlled Thyristors). Although frequently drawn as an NPN structure, the IGBT actually resembles a PNP bipolar transistor with an internal MOS device to control the base drive. Indicative by its description, the MCT is essentially an SCR structure also utilizing a MOS drive stage. Both devices offer significant cost advantages over MOSFETs for a given power capability.

MOSFET, IGBT and MCT Gate Drives: There are numerous reasons for driving the MOSFET gate to a negative potential during the device's off state. Degradation of the gate turn-on threshold over time and especially following high levels of irradiation are amongst the most common. However, with IGBTs, the important concern is the ability to keep the device off following turn-off with a high drain current flowing. On larger IGBT's with ratings up to 300 Amps, inductive effects caused by the device's package alone can "kick" the effective gate-to-emitter voltage positive by several Volts at the die - even with the gate shorted to the emitter at the package terminals. Actually, this is the result of the high current flowing in the emitter lead (package) inductance which can less than 1nH. The corresponding voltage drop changes polarity at turn off, thus pulling the emitter below the gate, or ground. If high enough, a fast turn off will be followed by a parasitic turn-on of the switch, and potential destruction of the semiconductor. Applying the correct amplitude of negative gate voltage can insure proper operation under these high current turn-off conditions. Also, the negative bias protects against turn-on from high dv/dt related changes that could couple into the gate through the "Miller" capacitance.

Unlike power MOSFET switches, IGBT trans-conductance continues to increase with gate voltage. While most MOSFET devices peak with about 10 to

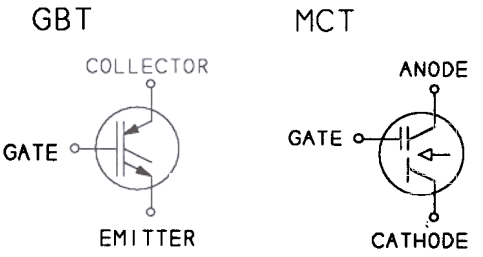

Fig 7. - IGBT and MCT Diagrams

12 Volts at the gate, IGBT performance steadily improves up to the suggested 16 Volt maximum gate voltage. Typically, most IGBT manufacturers recommend a negative drive voltage between -5 and -15V. Generally, it is most convenient to derive a negative voltage equal in amplitude to the positive supply rail, and ±15V is common.

The gate charge required by an IGBT (for a given voltage and current rating) is noticeably less than that of a MOSFET. Part of this is due to the better utilization of silicon which allows the IGBT die to be considerably smaller than its FET counterpart. Additionally, the IGBT (being a bipolar transistor) does not suffer from the severe "Miller" effects of the MOS devices, easing the drive requirements in a given application. However, because of their advantages, most available IGBTs have fairly high gate charge demands - simply because of their greater power handling capability.

In contrast, MCTs (MOS Controlled Thyristors) exhibit the highest silicon utilization level among power switching devices. While relatively new to the market, these devices are quickly gaining acceptance in very high power (above several kilowatts) applications because of their high voltage (1000V) and high current (to 1000A) capability. Recently introduced parts boast maximum ratings to one megawatt, ideal for large industrial motor drives and high power distribution—even at the substation level. These devices are essentially MOS controlled SCRs and are intended for low frequency switchmode conversion. They will most likely

replace high power discrete transistors, Darlingtons and SCRs because of their higher efficiency and lower cost.

Gate Charge And Effective Capacitance with Negative Bias: While several MOSFET and IGBT manufacturers recommend negative gate voltages in the device's off state, few publish any curves or information about gate charge characteristics when the gate is below zero Volts. This complicates the gate drive circuit design as each IGBT, MOSFET or MCT switch must be evaluated by the user over the ranges of operating conditions. A test fixture as shown in Figure 8 can be used to provide empirical generalizations for devices of interest. A switched constant current source/sink has been configured using a simple dual op-amp to drive a "constant" 1mA at the device under test (DUT). Gate voltage versus time can be monitored which provides the exact gate charge requirements for a given device. Any application specific requirements can also be accommodated by modifying the test circuit with external circuitry.

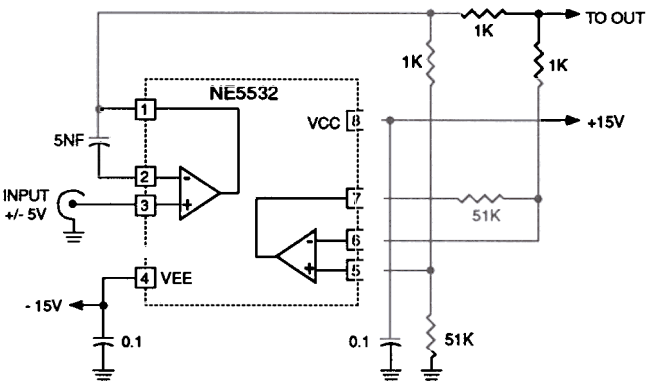

Fig 8. - Gate Charge Test Circuit

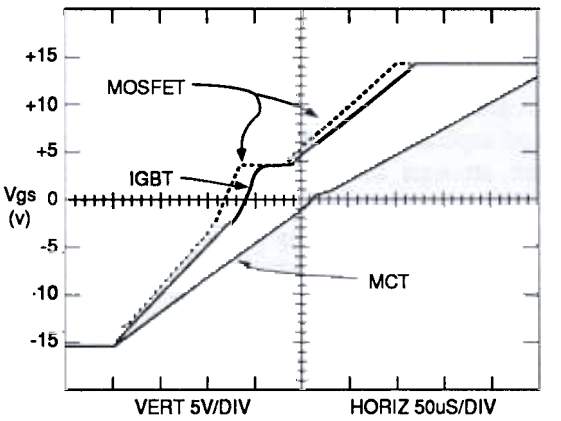

Fig 9. - Gate Charge Comparison Low to High Transition

Negative Gate Charge - Empirical Data: Several MOSFET, IGBT and MCT gate charge measurements were taken to establish the general characteristics with negative gate bias. The gate charge and effective capacitance during this third quadrant operation was calculated and compared to of the first quadrant specifications from the manufacturers data sheets. Figure 9 demonstrates the general relationships of gate charges for comparison.

Both the IGBT and MCT have similar negative bias gate charge requirements as with an applied positive bias. The MOSFET, however, exhibits a slightly reduced gate charge in its negative bias region, somewhere between 70 and 75 percent of its positive bias charge. The MOSFET's more significant "Miller" effect in the first quadrant is responsible for this since the higher effective capacitance during the plateau region does not occur with negative bias.

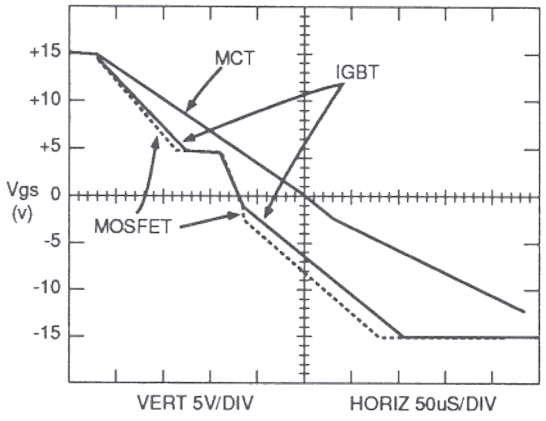

Fig 10. - Gate Drive Comparison
High to Low Transition

Total Gate Power - Negative Drive Voltage Applications: All of the previously presented gate power equations still apply, however they must be modified to include the additional charge requirements of the negative supply voltage. For the sake of simplicity, a multiplication factor can be used for recalculation of the exact figures. When identical amplitudes of positive and negative supply voltages are used, for example ±15V, then the gate power utilized can be simply multiplied by a factor of two. This completes the process for the IGBTs and MCTs. The total MOSFET gate charge, on the other hand, should only be multiplied by a factor of 1.7 to 1.75 to accommodate the reduced negative bias demands. Additionally, if a negative supply voltage different than the positive rail voltage is used, for example +15V and -5V, then the scaling factor must be adjusted accordingly. In this case, the new total gate power would be 1 + (−5/−15) or 1.33 times the initial 0-15V gate power for IGBTs and MCTs. The negative drive voltage scaling factor (−5/−15) would be multiplied by the 70 to 75% index if a MOSFET were used instead of an IGBT or MCT. This would result in a 1.23 to 1.25 times net increase over the initial (0-15V) gate power demand.

Summary

The universal need for improved switching efficiency in the power management industry is being addressed by the recent introductions of many higher performance MOSFET, IGBT and MCT semiconductors. Moreover, industry demand for increased power density continually elevates conversion frequencies. Each of these efforts has placed considerably more demands on the gate drive circuitry, especially the integrated circuit gate drivers. The intent of this paper has been to provide the designer with a comprehensive, quantitative understanding of gate drive characteristics, suitable for a variety of applications.

Additional Information

UNITRODE Application Note U-118, "New Driver IC's Optimize High Speed Power MOSFET Switching Characteristics", UNITRODE LINEAR IC DATABOOK, IC 600

UNITRODE Application Note U-126, "A New Generation of High Performance MOSFET Drivers Features High Current, High Speed Outputs"

UNITRODE Application Note U-127, "Unique Chip Pair Simplifies Isolated High Side Switch Drive"

INTERNATIONAL RECTIFIER Application Notes AN-937, AN-947 and Data Sheets, I.R. HEXFET Power MOSFET Designers Manual HDB-4

INTERNATIONAL RECTIFIER AN-983, "IGBT Characteristics and Applications"; IGBT Designer's Manual

High Performance MOSFET Driver Reference

UC1711: The UC1711 device features typical propagation delays of three and ten nanoseconds at no load, depending on the transition. Coupled with dual 1.5A peak totem-pole outputs, this device is optimized for high frequency FET drive applications. Its all NPN Schottky transistor construction is not only fast, but radiation tolerant as well.

UC1710 "Miller Killer": High peak gate drive currents are desirable in paralleled FET applications, typical of a high power switching section or power factor correction stage. Dubbed as "the Miller Killer", the UC1710 boasts a guaranteed 6A peak output current. This hefty driver current minimizes the FET parasitic "Miller" effects which would otherwise result in poor transition performance. Higher currents are possible with this driver, but the limiting factor soon becomes the parasitic series inductance of the FET package (15 nH) and the layout interconnection of 20 nH/inch. An RF type arrangement of the PC board layout is an absolute MUST to realize this device's full potential.

UC1710 Block Diagram: The UC1710 has "no-load" rise and fall times of 20 nanoseconds (or less) which do not change significantly with any loads under 3nF. It is also specified into a load capacitance of 30nF, representative of three paralleled "size 6" FET devices. Propagation delays are brief with typical values specified at 35 nanoseconds from either input to a 10% output voltage change.

UC1708: The UC1708 is a unique blend of the high speed attributes of the UC1711 along with the higher peak current capability of the UC1710. This dual noninverting driver accepts positive TTL/CMOS logic from control circuits and provides 3A peak output from each totem pole.

Propagation delays are under 25nsec with rise and fall times typically 35nsec into 2.2nF. The output stage design is a "no float" version incorporating a self biasing technique to hold the outputs low during undervoltage lockout, even with V_{IN} removed.

In the 16 pin DIL package, the device features a remote ENABLE and SHUTDOWN function in addition to separate signal and power grounds. The ENABLE function places the device in a low current standby mode and the SHUTDOWN circuitry is high speed logic directly to the outputs.

Transition Performance: Using the performance table, the driver output slew rates and average current delivered can be calculated. The figures can be compared to lower power op-amps or comparators to gain a perspective on the relative speed of these high performance drivers. The UC1708 delivers output slew rates (dv/dt) in the order of 300 to 480 V/µsec, at average load currents of under one amp, depending on the load. The high speed UC1711 exhibits similar characteristics under loaded conditions, but can achieve a no load slew rate of over 1700 V/µsec-nearly 2 V/nsec. For higher power applications, the UC1710 "Miller Killer" will produce an average current of 4.5A *at* slew rates of 150 Vµsec. With lighter loads it will deliver an average current of 1.5A at a slew rate of approximately 500 V/µsec. In most applications, the UC1710 will easily outperform "homebrew" discrete MOSFET transistor totem-pole drive techniques.

Each device in this new generation of MOSFET drivers is significantly more responsive than the earlier counterparts for a given application - higher speed (UC1711), higher peak current (UC1710) or a combination of both (UC1708).

UC1708 / 1710 / 1711 Performance Comparison

PARAMETER	LOAD	UC1708	UC1710	UC1711
Propagation Delay	0	25	30	10
t_{PLH}	1.0 nF	25		15
input to 10% output	2.2 nF	25	30	20
	30 nF		30	
Rise time	0	25	20	12
t_{TLH}	1.0 nF	30		25
10% to 90% rise	2.2 nF	40	25	40
	30 nF		85	
Propagation Delay	0	25	30	
t_{PHL}	1.0 nF	25		5
input to 90% output	2.2 nF	25	30	5
	30 nF		30	
Fall Time	0	25	15	7
t_{THL}	1.0 nF	30		25
90% to 10% fall	2.2 nF	40	20	40
	30 nF		85	

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