

Fixed-Frequency, Resonant-Switched Pulse Width Modulation with Phase-Shifted Control

by Bob Mammano

TOPIC 5

Fixed-Frequency, Resonant-Switched Pulse Width Modulation with Phase-Shifted Control

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Abstract

Modulating the energy in a bridge power stage with phase control can achieve high efficiency at high frequencies by combining square-wave conduction with resonant switching. With this approach, zero-voltage lossless switching can be obtained without the higher conduction losses typical with resonant topologies. An added benefit is constant frequency operation which significantly eases filter designs. As with so many other new topologies, the introduction of integrated circuit controllers are a vital part of industry acceptance and utilization, and this paper will describe one such new IC developed for this application.

Introduction

Designers have long known that attempts to reduce PWM power supply size by increasing the switching frequency quickly ran into unacceptable switching losses in the power devices, and that while resonant techniques made switching more efficient, these approaches added new losses caused by the higher peak currents of the sinusoidal waveshape. An additional troublesome characteristic of resonant mode topologies is the fact that control is accomplished by varying the switching frequency, a situation which complicates the design of the input and output filters and causes the system designer concern over noise sensitivity.

A resonant-switched, phase-shifted PWM control algorithm addresses all these issues. First, pulse-width modulation infers square waveshapes for both current and voltage which transfers more power for a given current level than sine waves and keeps the I^2R losses low. Secondly, resonant switching means that the high square-wave

switching losses at each transition are alleviated by using resonant techniques to switch the current at zero voltage. Finally, by controlling the phase relationship between two square-waves, a full range of control may be achieved with constant switching frequency. This technique is most easily implemented with a full bridge power topology and several examples have been described in past seminars.

Square-Wave Resonant Switching

The principle for controlling a phase-shifted PWM bridge starts by developing two complimentary square-wave drives with a method of varying the phase relationship between them. These waveforms are illustrated in Figure 1. Each drive will have two outputs which alternate with a 50% duty cycle to alternately drive the upper and lower switches in one-half of the bridge power stage. With the load connected between the centers of the two half-bridges, it should be clear that power is only received when diagonal switches within the bridge are conducting simultaneously. If the two half-bridges are switching with zero phase difference, there is no power delivered to the load; and, as the phase changes, the period of diagonal conduction changes, modulating the width of the output power pulse. The drive signals to the output stage are triggered from a master clock so that they run at constant frequency, and the phase relationship between the two complimentary half bridges is defined with conventional PWM techniques.

Each of the half-bridge drivers has been described as alternating with a 50% duty cycle but for resonant switching, there must be a dead-time, or short period at each transition when both

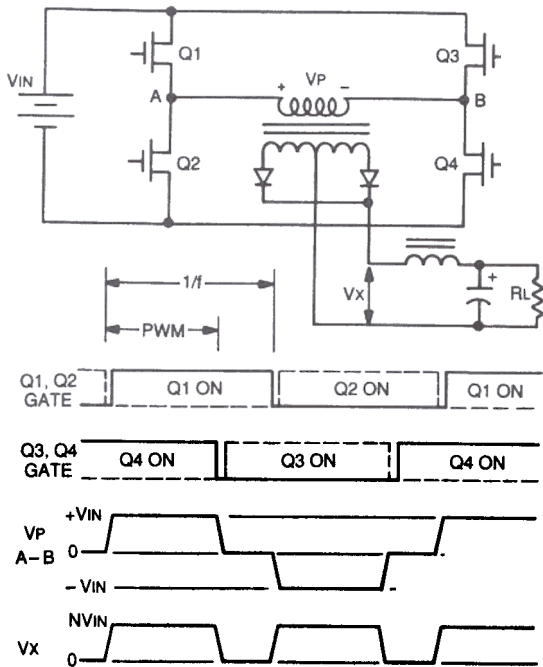


Fig 1. - Phase-Shifted PWM Bridge Power Stage and Waveforms

half-bridge switches are held off. During this time, the load inductance resonates with the parasitic capacitance of the power switches to swing the voltage from one rail to the other while both the half-bridge switches are off. Figure 2 shows this action during the time between Q4 turning off and Q3 turning on. The load current, as seen in the primary of the power transformer, diverts first from Q4 to the capacitors, C3 and C4, and then to the FET diode, D3, at which time Q3 can be turned on. With proper timing, both switches turn on and off with zero voltage across them, resulting in close to lossless switching. The challenge for the control circuit is to provide that proper timing, a task made more difficult because the value of the effective load inductance is different for the two sides of the bridge, and the fact that this dead-band must also be user-definable for different applications.

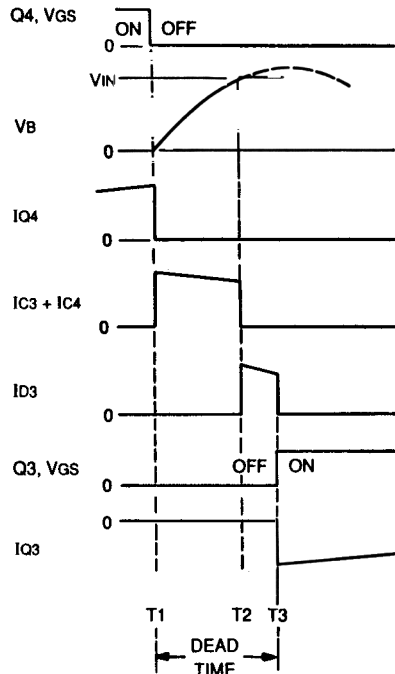
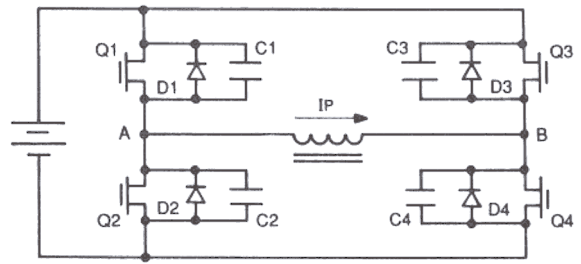


Fig 2. - Lossless Switching During Deadtime Between Q4 and Q3 Conduction

Phase-Shifted PWM Control

A new integrated circuit designed to implement phase-shifted PWM control—the UC1875—has been developed by Unitrode IC Corporation and is shown in block diagram form in Figure 3. This IC is different from all prior control chips in that it contains four separate outputs for driving the four bridge switches. These switch drivers must be activated as complimentary pairs with a method of varying the phase relationship between them. To understand this operation, look first to the upper portion of Figure 3. Here a constant frequency oscillator toggles a flip/flop whose two outputs

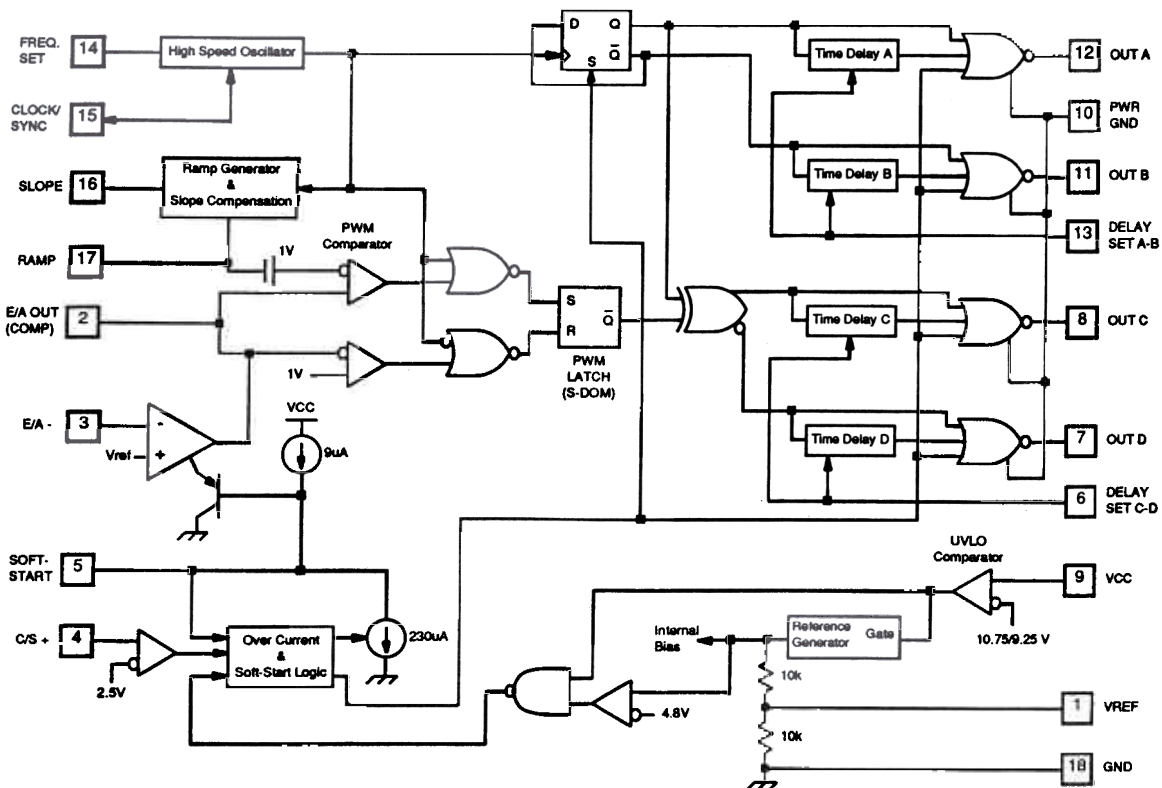


Fig 3. - UC1875 Phase-Shifted PWM Controller Simplified Block Diagram

form the alternating drive for one half-bridge. A dead-time between each transition is accomplished by a time delay for the turn-on signal which is bypassed for turn-off.

An identical pair of outputs provides the alternating drives for the other half-bridge but this pair is switched from the action of an Exclusive-Or circuit which is effectively triggered from the trailing edge of the PWM comparator. Since the upper flip/flop is synchronized with the leading edge of the PWM signal, the duration of the modulator's output pulse defines the relative phase relationship between the switching of the two half-bridges.

There are at least two performance characteristics important to the modulation circuitry: Operation must be correct and accurate at frequencies into the megaHertz range as a major goal is the capability for efficient high frequency performance; and the range for phase shift control must be as broad as

possible—desirably from zero to 180 degrees which is equivalent to pulse width modulation from zero to 100%. In order to better describe how the UC1875 meets these goals, the circuit blocks will be described individually.

The UC1875 Controller

Output Stage: Figure 4 shows a single output circuit in somewhat greater detail. Transistors Q3, Q4, Q5, and Q6 form a high-speed totem-pole driver which will source or sink more than one amp with a total delay of approximately 30 nanoseconds. To insure a low output level prior to turn-on, transistors Q7, Q8, and Q9 form a self-biased driver to hold Q6 on prior to the supply reaching its turn-on threshold. This circuit is operable even when the supply to the chip is zero. Q6 is also turned on and the output held low with the sensing of a current fault from the fault logic section of the chip.

The delay which provides the dead-time is

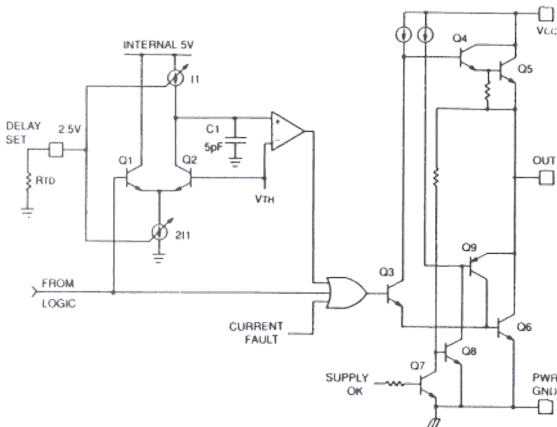


Fig 4. - One of Four Identical Output Stages in the UC1875

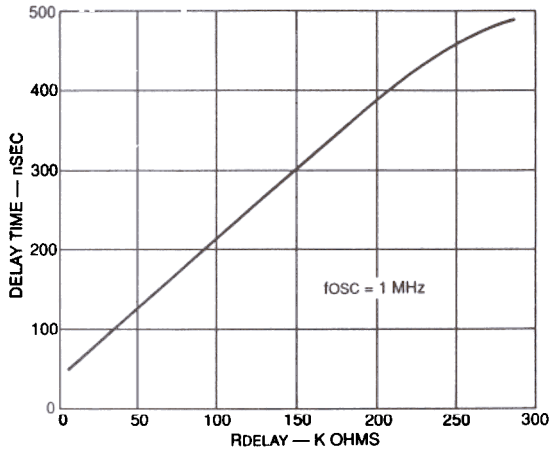


Fig 5. - Programming the Output Stage Turn-On Delay to Set the Deadband

The delay which provides the dead-time is accomplished with C_1 which must charge to V_{th} before the output can go high. The charging time is defined by the current source, I_1 , which is programmed by an external resistor, R_{TD} . Since the voltage level at the DELAY SET pin is internally regulated at 2.5V, predictability is assured and the range of dead-time control is from 50 to more than 400 nanoseconds as shown in Figure 5.

Oscillator: This circuit, as shown in Figure 6, is an all-NPN oscillator which will operate effectively at frequencies well above 2 MHz. The waveform at

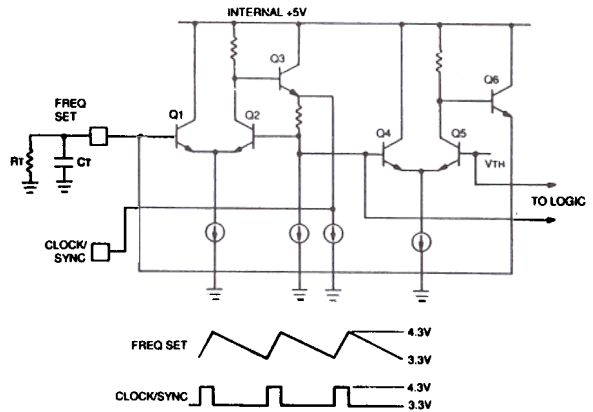


Fig 6. - The Timing Oscillator can be either Free-Running or Externally Synchronized

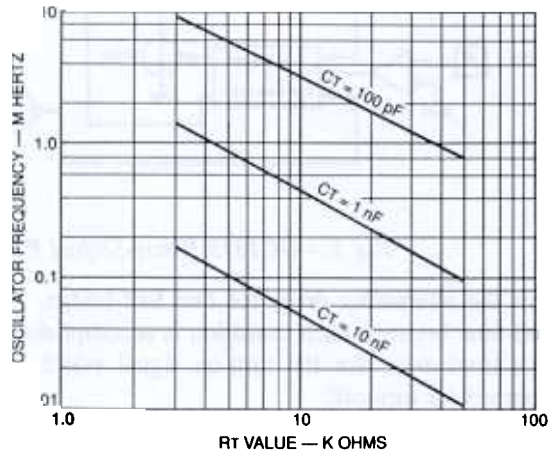


Fig 7. - Selecting R_T and C_T to Establish the Clock Frequency

the FREQ SET pin is an inverted ramp which allows the operating frequency to be accurately set with a parallel R_T - C_T to ground. The Oscillator timing relationships are shown in Figure 7. It should be noted that there is a separate ramp generator for use with the Pulse Width Modulator--this circuit is just for frequency control.

The clock output delivers a pulse which is nominally 50 nanoseconds wide but this pin is bi-directional—it can deliver a sync pulse to as many as four other circuits or it can accept a synchronizing signal from an external master clock.

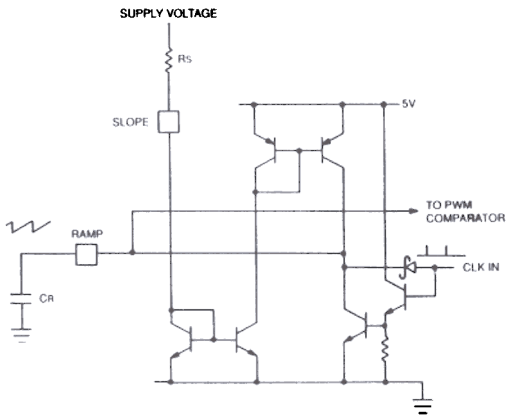


Fig 8. - The Ramp Generator Allows Either Voltage or Current Mode Operation

Ramp Generator: Figure 8 shows the Ramp Generator circuit which is merely a double current mirror, reset with each clock pulse. It can be used in several ways, however. With the resistor R_s tied to a stable voltage source, the waveform on CR will be a constant-slope ramp which will provide conventional voltage-mode control into the PWM comparator. With R_s connected to the power supply input voltage, a variable-slope ramp will give voltage feed-forward. Eliminating CR and tying the Slope pin to ground will provide a direct input into the PWM comparator for current-mode control. And finally, connecting CR in series with a small current-sensing resistor will allow a ramp to be added to a current waveform to accomplish current-mode with built-in slope compensation.

Error Amplifier: High frequency operation means more than just the performance of the oscillator. In addition to minimizing the circuit delays throughout the signal path, the Error Amplifier must have a wide bandwidth to allow using this high switching frequency to provide fast response to the external demands placed on the resultant power supply. The UC1875 accommodates this with a minimum bandwidth of 7 MHz and the frequency and step response as shown in Figures 9 and 10.

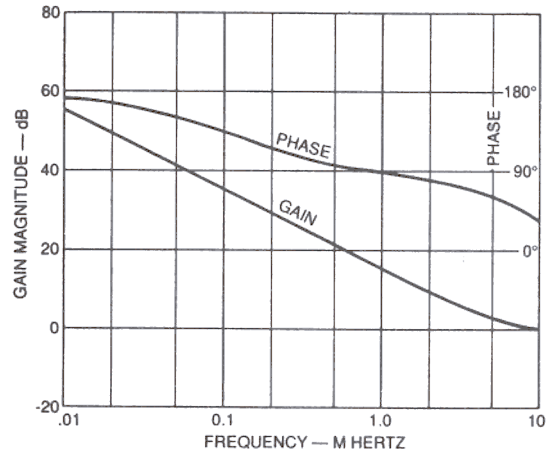


Fig 9. - Error Amplifier Gain / Phase Response

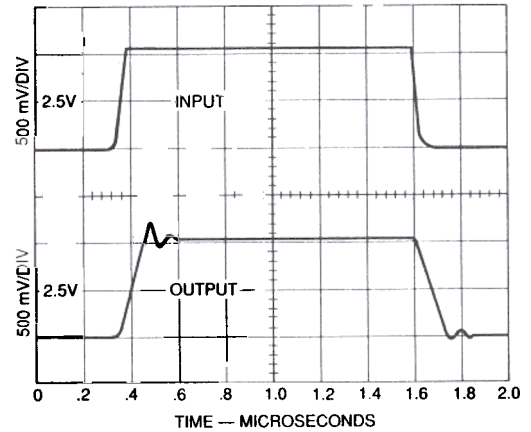


Fig 10. - Error Amplifier Step Response at Unity Gain

Phase Modulation: An important element in defining the method for phase control is to be able to extend the duty-cycle to as close to 100% as possible. Wide output pulses mean lower peak currents and even 100% at the modulator will be reduced by the dead-time used for resonant switching. Another implication of phase control is that a command for zero power cannot stop the switching action. Instead, the phase difference between the two half-bridges must go to zero to eliminate any power transfer to the load. So the challenge is to design a modulator which will control from zero to 100%, recognizing that there

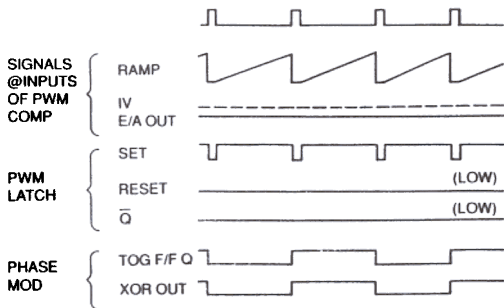


Fig 11A. - Phase Modulation -- Error Amplifier Output <1.0V

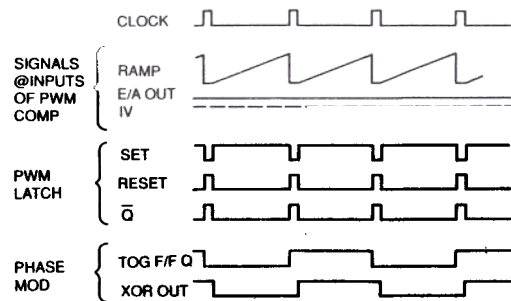


Fig 11B. - Phase Modulation -- Error Amplifier Output Between 1.0V and the Ramp Valley

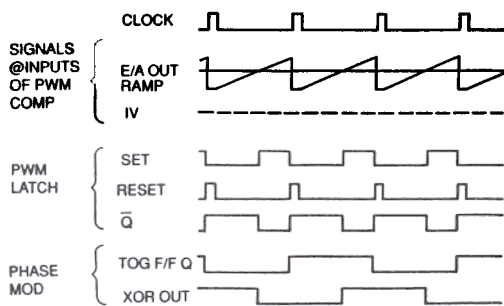


Fig 11C. - Phase Modulation -- Error Amplifier Output at Mid-Range

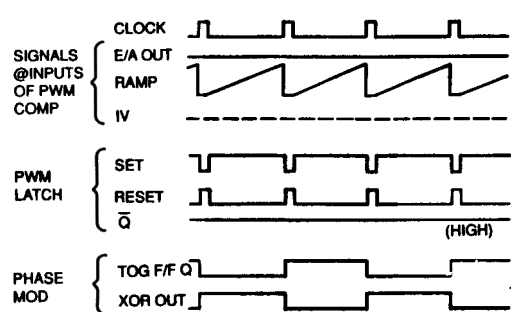


Fig 11D. - Phase Modulation -- Error Amplifier Output Greater than Ramp Peak

must be some overhead time to reset the clock, ramp, and latches. The solution implemented in the UC1875 can be seen in the block diagram of Figure 3. Control to 100% is accomplished with the PWM Comparator because the use of the Exclusive-Or circuit to drive the second output pair allows the clock pulse width to be placed at the beginning of the control range, rather than at the end as in all other conventional PWM circuits. Control to zero is now not possible with the PWM Comparator as its action will cease when its pulse width shrinks to the width of the clock pulse; however, as the Error Amplifier output drops below one Volt in an effort to further reduce the phase, the second comparator will hold the PWM Latch in reset forcing the output phase to zero.

The action of this control is best illustrated in the timing waveforms shown in Figure 11. These drawings show the phase modulation by comparing

the output from the Toggle Flip/flop with that of the Exclusive-Or. It should be noted that the dead-time delays will subtract from the on-time of all these modulator waveforms. The four graphs show the phase modulation resulting from four different levels of Error Amplifier command.

Fault programming: An additional function of any control circuitry is internal programming for housekeeping and fault protection. Figure 12 shows this operation as it is implemented within the UC1875. This device offers two forms of power shutdown: Complete turn-off of all four output power stages, and zero phase difference between the two half-bridges which remain switching. Complete turn-off is ordered for an over-current fault or a low supply voltage as a typical bridge power circuit is very unforgiving of abnormal conditions. When the SOFT START pin is low, however, switching is allowed to proceed while the

phase shift is advanced from zero to its nominal value with the time constant of the soft-start capacitor. The logic in the fault programming insures that a continuous fault will institute a low frequency "hiccup" retry cycle by forcing the soft-start capacitor to charge through its full cycle between each restart attempt.

Conclusion

This discussion has attempted to provide a thorough understanding of a control circuit which implements a new and significantly different power control algorithm. By integrating into a single IC all the circuitry necessary to perform these functions, resonant-switched, phase-shifted PWM power topology is now much more practical and cost effective, and power systems with significantly enhanced cost-effective power density should soon be a reality.

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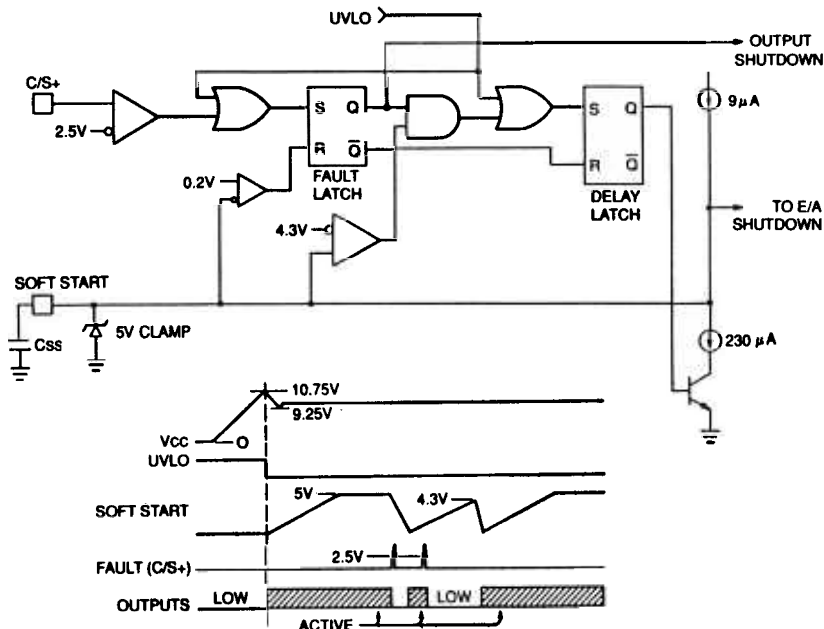


Fig 12D. - Fault Shut-Down Ensures Full Soft-Start Recycle Before Restarting

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