

Resonant Mode Converter Topologies – Additional Topics

by Robert Mammamo

TOPIC 6

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Bob Mammano

Introduction

In the 1988/89 series of Unitrode Power Supply Design Seminars, a basic tutorial on resonant mode power supply topologies was presented to describe the many circuit configurations possible and attempt to show how these topology choices might affect system performance. At that point in time, the emphasis was rightly given to the discontinuous, or quasi-resonant, approach as these were, and perhaps still are, the most widely applied techniques for raising switching frequencies without suffering excessive losses in the switching devices. With a quasi-resonant topology, the switching device conducts into a resonant circuit and switches off when either the current or voltage reaches zero. It then remains off until the demands of the load require another switch cycle. While these discontinuous approaches do reduce switching losses at frequencies into the megahertz range, the penalties they extract are higher conduction losses and wide ranges in switching frequency.

In seeking to reduce these drawbacks, there are at least two other circuit topologies which have been proposed in the industry and appear promising enough to be worthy of at least an introduction in this session. The first approach is a true continuous resonant circuit operating on the high side of the resonant curve, and the second uses resonant switching in a full-bridge, phase modulated circuit. Examples of these techniques are presented in the material which follows.

A Superresonant Series-parallel Half-bridge Converter

This information has been extracted from work described by R.L. Steigerwald of General Electric and references [1] and [2] listed below should be consulted for additional details.

A superresonant circuit is one that operates at frequencies above resonance and the important waveforms for a half-bridge topology are shown in Figure 1. Note that the current in the resonant inductor is continuous and lags the square-wave voltage drive. From the drain current waveform it can be seen that when one switch turns on, the current is flowing in the reverse direction through the body diode associated with that FET. This means that there is essentially zero voltage across the switch at turn on, and therefore minimal switching loss. The current smoothly transitions from the

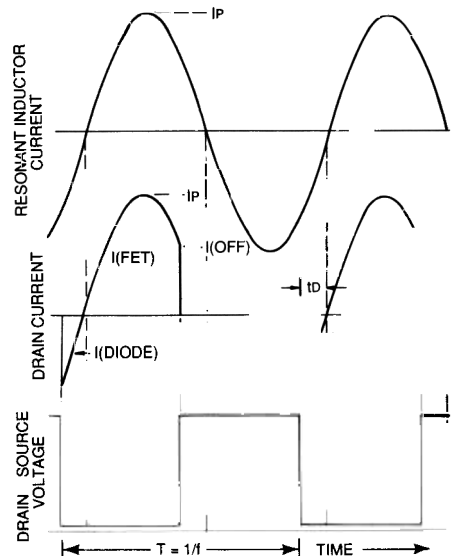


Fig. 1 -- Superresonant Converter Waveforms

diode to the FET and on through its resonant curve. Because the current is lagging, the switch turns off before the current reaches zero, potentially a high dissipation condition; however, by merely placing a small capacitor across the switch, the current transfers to charge the capacitor, which is then discharged through the load during the next half cycle. The internal FET diode which was conducting at turn on is allowed to recover while the FET is conducting in the forward direction - a fairly benign environment for this component, even at relatively high switching frequencies.

The control circuit for this topology commands an alternating 50% duty cycle for each switch, less a small dead time to allow the snubber capacitors to charge. Regulation is accomplished by varying the frequency such that it decreases - moves closer to the resonant point - with increasing load. The output filter is then designed to handle maximum load at a finite minimum frequency.

Although it hasn't been verified yet, it appears that the UC1861 could readily be used as a control circuit for this topology at frequencies up to one megahertz. With reference to the block diagram shown in Figure 2, the Error Amplifier can be used to decrease the VFO

frequency with increasing load, finite limits of minimum and maximum frequency may be programmed, the One-Shot can be used to set the dead-band time, and the two outputs can be transformer coupled to drive the two FET switches.

A half-bridge topology for a resonant converter is usually configured as either a series or parallel loaded circuit as shown in the first two illustrations of Figure 3. A series loaded circuit tends to act as a current source and, as a result, can lose voltage regulation if the load falls below some minimum. A parallel resonant circuit has a low output impedance and can therefore readily handle large load variations but the circulating current in the switches and resonating components is relatively independent of load and, as a result, the efficiency can drop significantly at light loads.

The series parallel configuration (C) of Figure 3 can be designed to deliver the best features of both the above circuits while minimizing their deficiencies. The balance between series and parallel operation is determined by the C_p to C_s relationship. Some compromise is necessary. A reasonable choice is to make $C_p = C_s$. Under this condition, series operation predominates at high loads. Decreasing the

load decreases the circulating current, maintaining efficiency down to some median load. Below this value the circuit takes on parallel characteristics and while the circulating current no longer decreases, control is maintained down to no load.

So in comparison to a quasi-resonant topology,

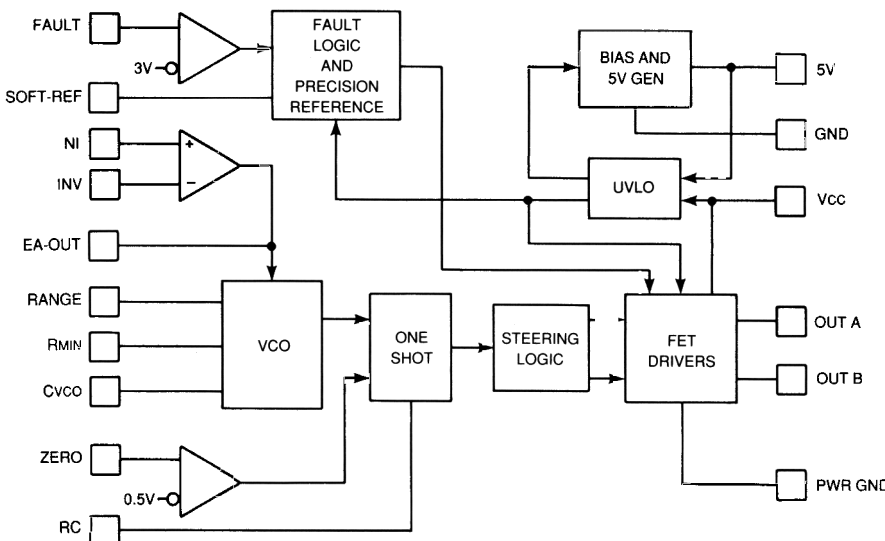


Fig. 2 -- Superresonant Control Using the UC1861

the series-parallel, superresonant, half-bridge converter appears to offer:

- Lossless switching
- No need for fast diodes or lossy snubbers
- Less frequency variation to regulate
- Lower conduction losses
- Less efficiency loss at light loads

A Fixed-frequency, Full-bridge, Resonant-switching, Phase-shifted PWM Converter

This mouthful of adjectives, which for simplicity's sake is often shortened to "Phase-Shifted PWM", describes a conventional bridge topology which has been modified in two ways - the modulation is done by phase shifting two over-

lapping constant-frequency square waves, and resonant switching is used to minimize switching losses. It is not a full resonant circuit in that both the voltage and current waveforms are square - except at the transitions where resonance is used to extend the rise and fall times, achieving what is often called "soft" switching. In addition to relatively lossless switching, an obvious benefit of this approach is a constant switching frequency.

Parentage of this topology has been difficult to determine. The phase shifted PWM technique may have stemmed from work done by Bruce Carsten in testing magnetic cores, while the resonant switched bridge was used many years ago in commutating high-power thyristor switches. Material for this description was largely derived from work done at IBM by M.M. Walters and W.M. Polivka, but the Reference section lists several other useful sources.

The basic phase-shifted bridge circuit is shown in Figure 4 and while the schematic is the same, the meth-

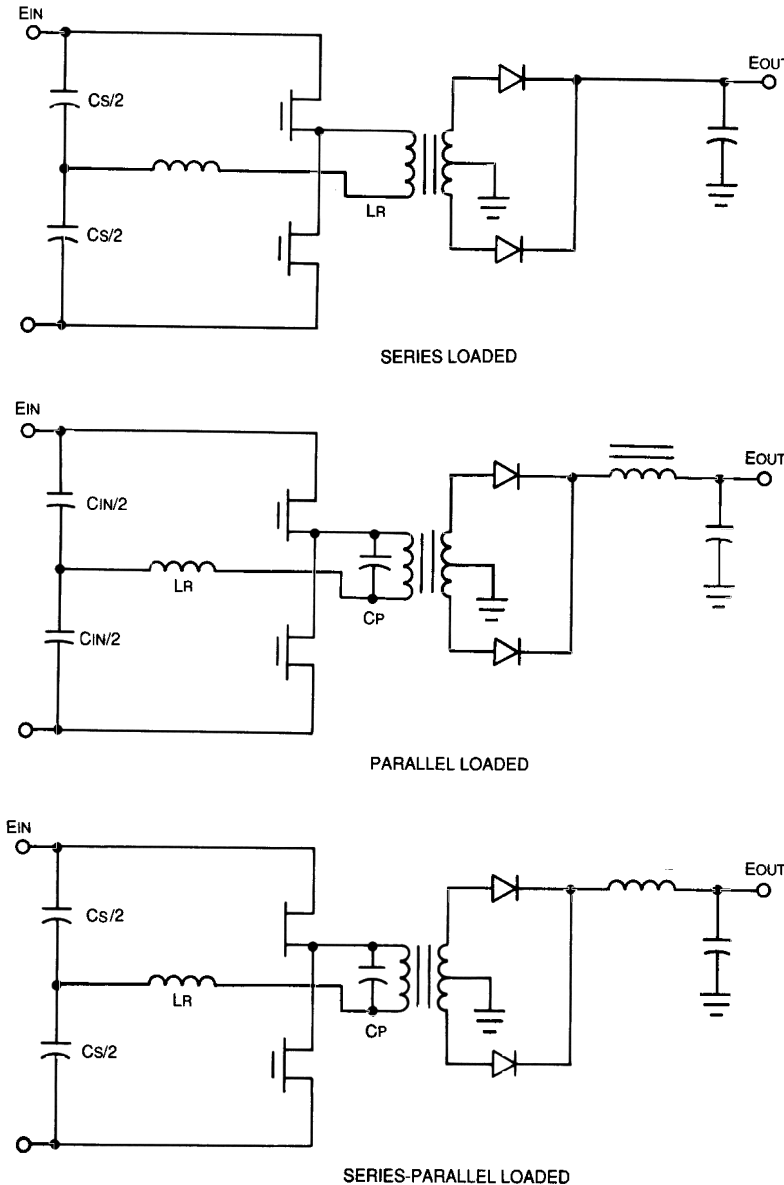


Fig. 3 -- Series, Parallel, and Series-Parallel Loading

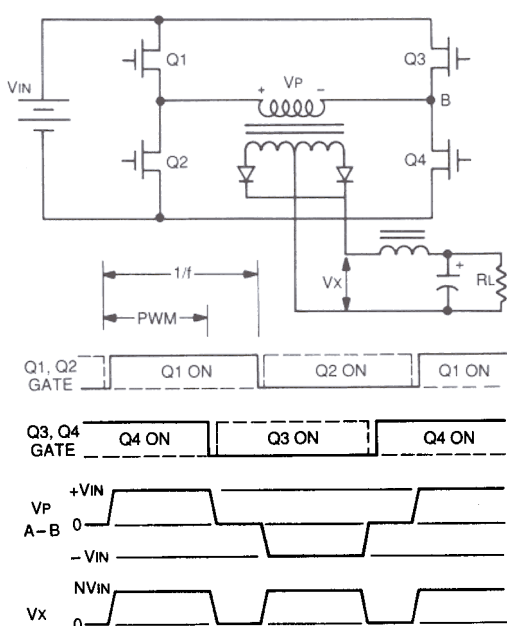


Fig. 4 -- Phase-Shifted Bridge Circuit

od of driving the switches is quite different from a conventional PWM bridge. Instead of varying the on-time of diagonally conducting switches, all four switches are always driven with a constant frequency, 50 percent duty cycle while the phase relationship between diagonal switch pairs is controlled to pulse-width modulate the period of overlapping conduction. From the waveforms of Figure 4, it can be seen that one switch on each side of the bridge is always conducting. Current is delivered to the load when diagonal switches are on, and freewheels in the primary when opposite switches conduct. The fact that the freewheeling current circulates in the primary side - rather than in the output rectifiers - is an important part of the mechanism for low-loss switching.

This mechanism is illustrated in Figure 5, but first it must be noted that the duty cycle for each switch is not actually 50%, but slightly less to allow a small but important dead time during which the resonant action takes place. For this explanation, it is assumed that initially switches Q_1 and Q_4 are on and delivering current to the load by means of primary current, I_p , flowing as shown. At time T_1 , Q_4 is

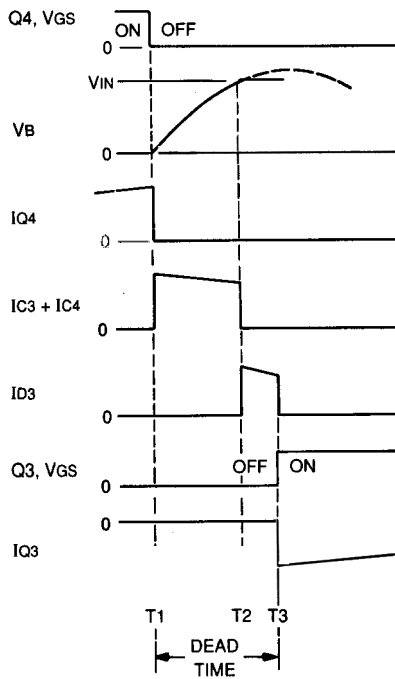
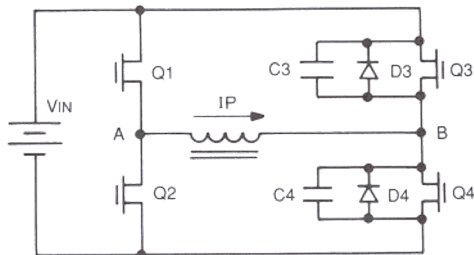


Fig. 5 -- Phase-Shifted Bridge Waveforms

turned off but I_p continues to flow due to the reflected action of the output inductor. Since Q_4 is off, I_p must now go into the parasitic capacitances of Q_4 and Q_3 , increasing the charge on C_4 and reducing it on C_3 . While this is happening, the node voltage at V_B resonates up until it forward-biases the body diode of Q_3 at time T_2 . Now the voltage is clamped with D_3 conducting until Q_3 is turned on - with close to zero voltage across it - at time T_3 . From this time, the current can continue to circulate through Q_1 and Q_3 , but with no voltage across the primary winding.

The next sequence in the operation is that Q_1 turns off and during the dead time on the left side of the bridge, node voltage V_A resonates down until it forward biases the diode of Q_2 , at which time Q_2 can turn on losslessly. While the mechanism is similar to that described above, there is one important difference: With the reversal in voltage across the primary winding, the current quickly reverses from positive freewheel current to negative load current with the controlling inductance being the leakage and magnetizing inductance of the power transformer. Insuring that this transition will always be concluded within the dead time - to insure that Q_2 turns on with zero voltage - may require a gap in the power transformer core to increase the resonating inductance.

Developing a drive for this phase-shifted topology takes a little extra effort as there is currently no integrated circuit controller with the required architecture; however, a possible block diagram is shown in Figure 6. In this circuit, the upper flip-flop is triggered by the clock to provide alternating drives to one side of the power bridge. The lower flip-flop is

triggered by the trailing edge of the PWM generator so that it generates the alternating drive for the other side of the bridge, but with a phase delay equal to the width of the PWM signal. There is some additional gating to insure that both flip-flops keep switching with zero phase difference when the PWM signal goes to zero. The time delays in the outputs delay only the turn on commands, providing a deadband which can be set for the particular application. Since the bridge sees only the differences between drive commands, any additional delays common to all outputs should cancel out allowing full control from zero to maximum duty cycle. The outputs from this controller must interface with gate-drive transformers which will be necessary to provide the level shifting to the upper power switches. Gate drive transformers have the added advantage of forcing one gate negative when the other is driven positive, preventing parasitic turn-on from the Miller capacitance.

Recognizing the added complexity of a full-bridge topology, this phase-shifted PWM approach has several advantages:

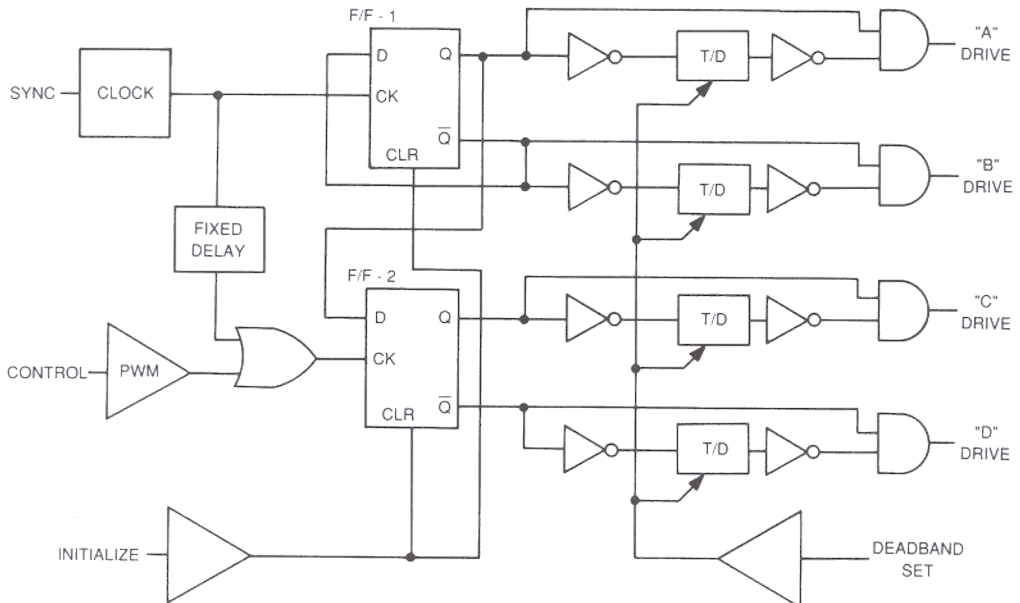


Fig. 6 -- Possible IC Controller for Phase-Shifted PWM Converter

- Lossless switching at high frequencies (Power switches turn on and off at zero voltage)
- Minimum conduction losses with PWM power transfer
- Fixed frequency operation
- Trapezoidal waveshapes for low RFI and EMI

Using this technology, IBM has reported a 220 Watt, 5 Volt output, 200 Khz converter with 80% efficiency; GE has built a 250 Watt, multiple output, 500 kHz converter at 90% efficiency; and MIT also reports 90% efficiency for a 1 kW, 40 Volt output, 500 kHz model.

References

For the Superresonant Half-Bridge:

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- [2] R.A. Fisher, R.L. Stiegerwald, and C.F. Saj, "A Frequency/PWM Controlled Converter with Two Independently Regulated Outputs", *HFPC Proceedings*, pp. 459 - 471, May 1989.

For the Phase-Shifted PWM:

- [3] M.M. Walters and W.M. Polivka, "A High-Density Modular Power Processor for Distributed Military Power Systems", *APEC Proceedings*, pp. 403 - 412, March 1989.
- [4] L.H. Mweene, C.A. Wright and M.F. Schlecht, "A 1kW, 500kHz Front-End Converter for a Distributed Power Supply System", *APEC Proceedings*, pp. 423 - 432, March 1989.

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- [6] B. Carsten, "Fast, Accurate Measurements of Core Loss at High Frequencies", *PC&IM Magazine*, March 1986.

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