High Power Factor Preregulator for Off-Line Power Supplies

by Lloyd Dixon

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Lloyd H. Dixon, Jr.

Introduction

Off-line switching power supplies usually employ a rectifier bridge or doubler with a simple capacitor input filter to draw power from the ac line. The "bulk" filter capacitor charges to nearly the peak ac line voltage, supporting an unregulated dc bus powering the downstream switching converters. This bulk capacitor must be *large*. It alone supplies total power during most of each half-cycle while instantaneous line voltage is below the dc bus, (or for longer time, depending on hold-up requirements).

Unfortunately, with a capacitor input filter, the line current waveform is non-sinusoidal—a narrow pulse with very high peak current. Input power factor is only 0.5 − 0.65 and the high harmonic content causes line noise. The rms line current may be twice the equivalent rms sine wave. A 120V, 15A line may not be able to supply even 1 kW of input power without tripping the line circuit breaker. With lower wattage systems, perhaps twice as many high power factor supplies could operate from the same line. For these reasons, high power factor is becoming a requirement in many power supply specifications.

The high power factor switching preregulators described in this paper are interposed between the input rectifier bridge and the bulk filter capacitor. Switching at a frequency *much* higher than the line, the preregulator is programmed to draw a half-sinusoid input current, in phase with the line voltage. The current is controlled by the deviation of the dc bus voltage from the desired value. The result is:

1. Improved input power factor: .95 to .999

2. Reduced harmonics (< 3%, if necessary)
3. Tapless/switchless operation over the full 90V − 270V line voltage range.
4. Crudely regulated bulk capacitor voltage. The resulting narrow dc bus voltage range permits the downstream converters to be designed for lower cost and greater reliability and efficiency.
5. Smaller bulk capacitor size and cost.
6. Reduced rms charging current resulting in improved capacitor reliability.

Basic Preregulator Operation

Throughout this paper, a preregulator switching frequency, f_s = 100 kHz, and a line frequency, f_L = 60 Hz are assumed.

Referring to Fig. 1, to achieve an input power factor approaching 1.0, the preregulator is programmed to draw input current which varies in direct instantaneous proportion to the input voltage half sine wave. Thus the voltage and current waveforms on the input side of the rectifier bridge are in-phase sine waves. This is of course what a simple resistive load does, and an active preregulator circuit performing this function is often called a "resistor emulator".

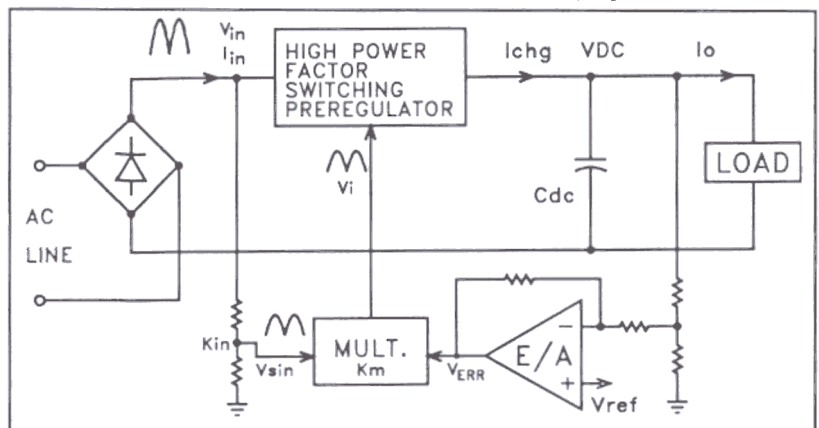The input current programming signal may be obtained by multiplying a half-sinusoid

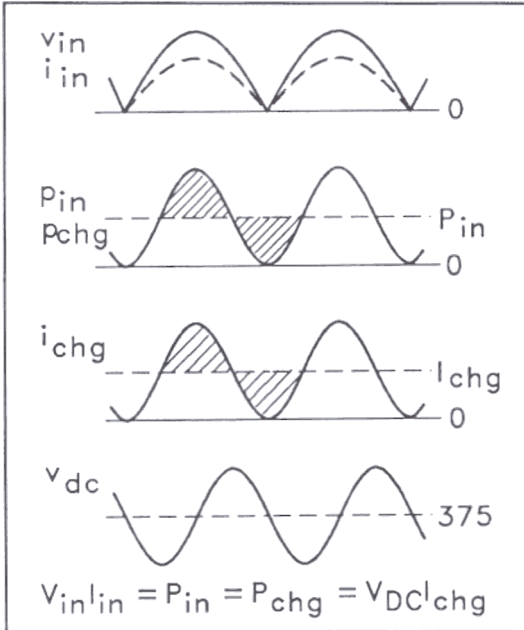Fig. 1 - High Power Factor Preregulator

Fig. 2 - Preregulator Waveforms

(usually derived from the rectified line voltage waveform) by a control voltage, V_{ERR}, which must be constant during each half-cycle. Thus V_{ERR} controls the rms input current, governing the power drawn from the line during each half cycle. V_{ERR} represents the deviation of V_{DC} from its desired value, amplified and inverted at the error amplifier output. When V_{DC} is low, V_{ERR} is large, calling for increased input power to make up the energy deficit in the bulk filter capacitor, C_{DC}, across the dc bus.

Power transfer: Although the preregulator input current waveform is a half-sinusoid, its output current i_{chg}, which charges C_{DC}, is a sine squared function (see Fig. 2). Considerable operational insight can be gained by thinking in terms of the preregulator *power input* and *power output*, rather than input/output voltages and currents—see Fig. 2. Assuming the preregulator operates with high efficiency and at a switching frequency very much greater than the line (100 kHz vs. 50-60 Hz), the amount of energy stored or dissipated within the preregulator can be considered negligible at the line frequency. (Inductive energy stored in the preregulator is usually more than the energy transferred during one *switching* frequency cycle, but totally negligible compared to energy transfer

during one *line* half-cycle.) Thus on a time scale relevant to the line frequency, the instantaneous power output to C_{DC} equals the power input, and the cumulative energy delivered to C_{DC} during each line half-cycle equals the energy drawn from the line.

With high power factor (1.0), the line voltage and current waveforms are in-phase sine waves, by definition. Thus, during each half-cycle, the instantaneous input power, p_{in}, (and p_{chg}, the power output to C_{DC}) is a $\sin^2$ function:

$$p_{chg} = p_{in} = 2\,V_{in}I_{in}\sin^2\omega_L t \qquad (1)$$

where V_{in} and I_{in} are rms values and
$\omega_L = 2\pi$ times line frequency.

Since $2\sin^2 x = 1 - \cos 2x$, then

$$p_{chg} = p_{in} = V_{in}I_{in}(1 - \cos 2\omega_L t) \qquad (2)$$

C_{DC} is usually large enough to hold the dc bus voltage V_{DC} fairly constant. Thus the charging current is nearly proportional to the instantaneous power, and:

$$i_{chg} \approx p_{chg}/V_{DC}$$
$$\approx V_{in}I_{in}(1 - \cos 2\omega_L t)/V_{DC} \qquad (3)$$
$$I_{CHG} = V_{in}I_{in}/V_{DC} \qquad (4)$$

(4) is the average of (3)

As shown in Fig. 2, the ac component of i_{chg} produces a small ripple voltage, v_{dc}, at $2f_L$ (with 90° phase lag) on the dc bus, depending on capacitor size. i_{chg} is not perfectly sinusoidal because the ripple component of V_{DC} makes Eq. 3 an approximation, but the error is negligible in practice.

For a minimal C_{DC} value (providing ½ cycle hold-up), the ripple voltage on a 400 V dc bus will be approximately 10 to 20 Vp-p at full load. If C_{DC} is too small, the dc bus ripple voltage will be larger, but more importantly, bus voltage regulation against line and load changes will be very poor and hold-up capability will be inadequate.

Note that in the entire preceding discussion, the specific power circuit topology was not mentioned. Indeed, the input/output voltage, current and power waveforms and magnitudes are fundamental to the preregulator's task of maintaining good input power factor, charging C_{DC} and regulating the dc bus voltage, totally independent of the specific power circuit used.

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Power Circuit Topology

Three basic power circuit topologies—Buck, Flyback, and Boost—that might be used in the high power factor switching preregulator are shown in Fig. 3. Each circuit has its advantages and disadvantages which are summarized in Fig. 4.

Boost topology: This is the most popular HPFP configuration. Boost circuits require that the output voltage, V_{DC}, must always be greater than instantaneous line voltage, v_{in}. A boost circuit designed for a V_{DC} level exceeding the maximum peak line voltage can operate over the full line voltage range, from zero to the max. peak value. V_{DC} of 380–400V allows operation over a span of 90V to 270V rms line without range switching. However, because V_{DC} must exceed v_{in}, the boost topology is not compatible with a standard 300 V_{DC} bus from a 220V line. Unfortunately, a 400V bus requires higher voltage ratings for the devices used in the downstream converters.

In the boost configuration, the input current is not switched and di/dt is low because of the inductor location. This minimizes line noise and EMI. In addition, line spikes are absorbed by the inductor, increasing circuit reliability.

With continuous mode operation, the input location of the inductor also makes it easy to use current mode control to program the input current half sine. (Current mode control actually controls inductor current.)

The circuit location of the transistor switch makes it easy to drive the gate/base, since the source/emitter is referenced to the control circuit and C$_{DC}$ common. The maximum voltage applied to the transistor equals the output voltage, V_{DC}.

Probably the greatest disadvantage of the boost topology is its *inability to limit current*, because there is no series switch between input and output. Overload or startup overcurrent conditions cannot be controlled or limited. While it can be argued that the downstream switching power converters will provide the necessary current limiting to protect the preregulator, failure of the bulk capacitor or converter transistors is not covered.

Furthermore, the boost topology can not function with V_{DC} less than the instantaneous line voltage. This occurs every time the supply
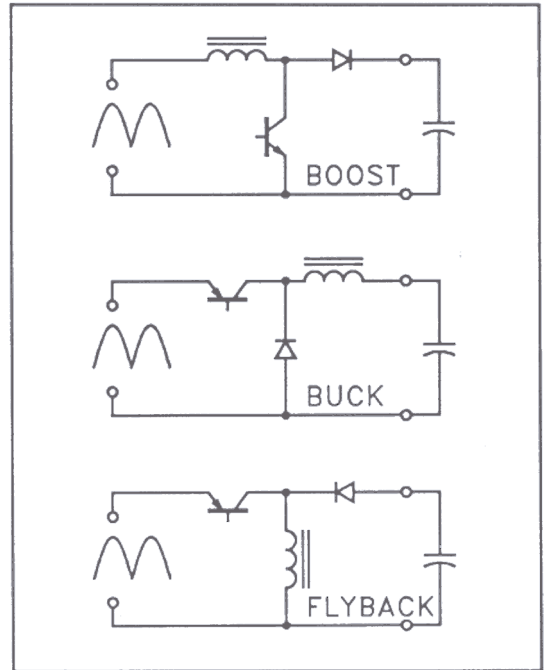

Fig. 3 - Basic Preregulator Topologies

is turned on, and after line voltage interruptions of sufficient duration. Soft start is useless because the boost circuit does not function under these conditions. The transistor switch will remain *off*, but input current will rise to a peak value several times greater than normal maximum levels, saturating the input inductor and causing failure unless *additional* current limiting circuits are provided. This will be discussed fully later in this paper.

Slope compensation is required with continuous mode operation to avoid instability at duty ratios > 0.5, occurring whenever instantaneous v_{in} is less than $V_{DC}/2$. Slope compensation is difficult to accomplish with the boost topology because the inductor current downslope (which determines the compensation required) varies considerably with v_{in}. This problem can be avoided by reducing the bandwidth of the inner current control loop so that the *average* inductor current is directly controlled, rather than the *peak* current intercept. There is plenty of room to reduce the current loop bandwidth without affecting circuit performance because the switching frequency is so much higher than the line frequency.

BOOST – Constant Frequency, Continuous Mode

ADVANTAGES:
1. Input current is not chopped – little EMI
2. Inductor current *is* input current – current mode control is ideal to program input current waveform.
3. Switch voltage ratings = V_o
4. Inductor at input absorbs line voltage spikes
5. Easy to drive switch - source/emitter at zero ref.

DISADVANTAGES:
1. No control when $V_{in} > V_o$ – start-up, line overvoltage
2. Cannot limit overcurrent – load fault, start-up.
3. V_o higher than max. peak V_{in} requires higher voltages in downstream converter.
4. Slope compensation required – changes with V_{in}

BUCK

Unsuitable for high power factor preregulator except as supplement to Boost preregulator for current limiting.

FLYBACK – Constant Frequency, Continuous Mode.

ADVANTAGES:
1. V_o can be greater or less than peak V_{in}
   a. 300V bus – eases voltage requirements of downstream converter.
   b. Can control start-up current inrush and load fault.
2. Easy to provide isolation in preregulator rather than in downstream converter transformers.

DISADVANTAGES:
1. High switch voltage ratings: $V_o + V_{in}$
2. Chopped input current – hard to filter – EMI
3. Difficult to program input current half sine with current mode control
4. Slope compensation required

Discontinuous Flyback – PRO'S & CON'S
1. Automatic current half-sine by programming and fixing the "on" time during each line half-cycle.
2. No slope compensation required.
3. Peak current nearly twice continuous mode flyback

Fig. 4 - Preregulator Topology Advantages/Disadvantages

The discontinuous inductor current mode is impractical for the boost topology in the high power factor preregulator because at peak V_{in} the inductor current downslope is very shallow, so ripple current is small. But in a high power factor preregulator at peak V_{in}, line current is at its peak. With high peak current but low ripple, inductor current must be continuous.

Buck Topology: In the buck configuration, V_{in} must be greater than V_o. This makes it unsuitable for high power factor preregulator use because it cannot function on the skirts of the input half sine when v_{in} is less than V_{DC}. However, the buck topology can be very useful to provide current limit support to a boost pre-regulator.

Flyback Topology: The flyback (buck-boost) configuration overcomes two of the boost topology disadvantages: The flyback circuit can control and limit start-up inrush current and load overcurrent. Also, the output voltage may be *greater or less* than the instantaneous input voltage, making it possible to provide a 300V bus from a 220V rms line.

In the basic flyback circuit, output voltage must be opposite in polarity from the input voltage. This may be inconvenient. But the circuit location of the inductor provides a unique possibility for the flyback: the inductor could have primary and secondary windings. This can provide polarity independence and also input-output isolation in the preregulator, relieving

the downstream converters of this isolation requirement. The converter transformers can be simplified and leakage inductance reduced because creepage and insulation are eliminated. Isolated feedback can also be eliminated in the downstream converters, making it easy and inexpensive to achieve good regulation.

However, the chopped input waveform of the flyback circuit results in more noise and EMI than the comparable boost topology, requiring more input filtering.

The location of the transistor switch makes it difficult to drive the gate/base—a small drive transformer is normally used.

The transistor voltage rating must be greater than max peak $v_{in} + V_{DC}$, much higher than with the boost configuration.

Finally, it is more difficult to program the required input current half-sine wave with the flyback preregulator and current mode control. This is because current mode control actually controls *peak inductor* current, which is almost the same as the *average inductor* current with continuous mode operation (with any topology). The inductor current *is* the input current in the boost topology, but not in flyback circuits. The relationship between flyback input current and inductor current changes considerably with v_{in}, which complicates input current programming. Also, slope compensation is required with continuous mode operation.

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Both of the above problems can be overcome by using *average input* current mode control, sacrificing some current loop bandwidth, as discussed earlier with the boost circuit.

Discontinuous mode flyback: Input current can be easily programmed in the constant frequency, discontinuous operating mode if the "on" time, or duty ratio, is made proportional to the control voltage, V_{ERR}. Peak and average currents at 100 kHz will then be proportional to the instantaneous line voltage waveform, automatically providing high power factor during each half cycle. No slope compensation is required with discontinuous operation.

The main disadvantage of the discontinuous mode is that the triangular shaped input waveform has nearly twice the peak current of the comparable continuous mode waveform. This increases noise problems and transistor current rating requirements.

The Control Loop

The basic control circuit as shown in Fig. 1 is independent of the specific power circuit topology used. It involves an inner current control loop and an outer voltage control loop. The current in the inner loop is programmed according to the output voltage error sensed and amplified by the outer loop. Thus the control circuit operates exactly like any current mode control system—with two exceptions:

1. The current control loop programs the *input* current, not the output current.
2. The programmed current is proportional to the control voltage, V_{ERR}, *multiplied by a half sine derived from the rectified line voltage.*

These two control system elements assure that the input current is a half sine wave in phase with the rectified input voltage, i.e., the input power factor approaches 1.0.

However, there are several significant and limiting problems with this basic control system approach. To set the stage for this, consider the following:

The load power demand on the switching preregulator does not change with input rms line voltage, for two reasons:

1. The preregulator maintains a fairly constant output bus voltage V_{DC}.
2. The downstream switching converters draw constant power regardless of V_{DC} variation.

Since the switching preregulator operates with high efficiency, the *input power drawn from the line does not change with rms line voltage*, but only with downstream load changes.

Therefore, when rms line voltage varies:

a. *rms* line current must be *inversely proportional* to the *rms* line voltage to maintain constant power input.

But *within each half-cycle*:

b. *Instantaneous* current must be *directly proportional* to *instantaneous* line voltage in order to have a good power factor.

Poor open loop line regulation: Criteria (a) and (b) above conflict with each other in the basic control circuit. If control voltage V_{ERR} is fixed (open control loop), instantaneous current programmed by the multiplier is directly proportional to instantaneous line voltage, thus satisfying (b) and providing good power factor. However, in contradiction to (a), rms line current will also vary *directly* with rms line voltage. Thus, although power input should not change, it will actually vary with the *square* of the rms line voltage. This results in very poor open loop line regulation, and requires strong closed loop intervention to correct. But it will be shown that the control loop bandwidth must be much less than 120 Hz. This causes considerable change in dc bus voltage when the line voltage changes rapidly. Without current limiting, input current may be excessive for several half-cycles.

The usual solution to this problem caused by low bandwidth is to add considerable additional control circuitry to sense and limit input current and/or power and to sense and limit over and under-voltage on the dc bus. These auxiliary circuits override the slow main control loop to achieve quick corrective intervention. Whenever this occurs, the input waveform is clipped and the power factor is low for several half-cycles while the main control loop slowly adapts to the new conditions.

A much better solution uses *input voltage feed-forward* to provide the main control circuit with good inherent open-loop line regulation. With input voltage feed-forward, the control circuit can respond to a line voltage change within one half cycle, maintaining low power factor and eliminating most of the additional control circuitry.

Control loop bandwidth limitation: As discussed previously, with a bulk filter capacitor of acceptable cost and size, there will be 120 Hz ripple voltage on the dc bus, perhaps $10V_{p-p}$ on a 380V bus at full load. This results in a 120 Hz control voltage component at the error amplifier output, which will oppose and reduce the ripple on the dc bus, depending upon the control loop gain at 120 Hz. While this ripple reduction is a laudable goal, the 120 Hz control voltage component will distort the half-sine current programming waveform and the input current, as shown in Fig. 5. This can make it impossible to achieve the desired power factor.

To prevent this distortion, *the control voltage must not be allowed to change significantly during each line half-cycle.* Control loop bandwidth must be much less than 120 Hz to keep the input sine wave distortion to an acceptable level. Circuit simulation shows that to achieve P.F. = .96, the *maximum* crossover frequency, f_c, is about 20 Hz at max. V_{in}. At lower V_{in}, f_c will be *much* less. This low bandwidth severely impairs the control loop dynamics. The dc bus voltage will respond very slowly to line or load changes, making it difficult to keep the dc bus voltage within desired limits. If a power factor greater than .98 is required, control loop bandwidth must be very low. (3% harmonic distortion requires P.F. = .999)
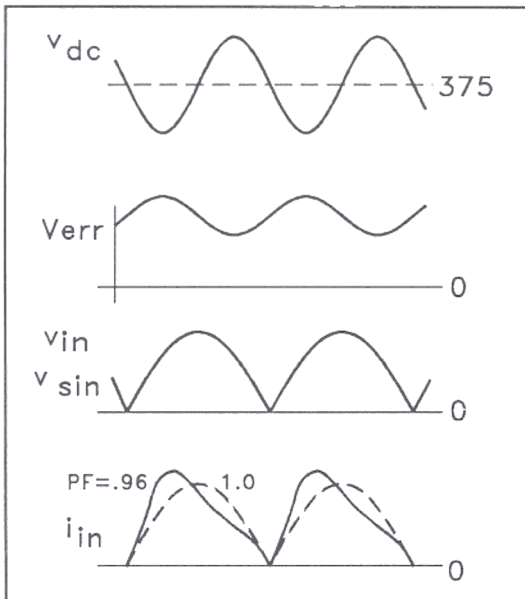

Fig. 5 - Input Current Distortion, PF = .96

Another technique that totally eliminates input current waveform distortion, achieving very high power factors without requiring extreme low bandwidth, is to *sample and hold* the control voltage, V_{ERR}, every half cycle when the line voltage crosses zero. Although the power factor is excellent with the sample and hold (S/H) technique, the crossover frequency is limited to about 20 Hz (one fifth the 120 Hz sampling frequency) for stability reasons.

So whether or not S/H is used, to maintain the dc bus voltage within desired limits requires either (a) extensive override control circuits or (b) input voltage feed-forward, which greatly improves the dynamics by making fast open-loop correction for line voltage changes.

Control loop gain and bandwidth variation: As shown in Eq. (5), the small signal gain from control to output (part of the overall voltage control loop gain) varies with the *square* of the rms input voltage:

$$\frac{v_{dc}}{v_{ERR}} = \frac{kV_{in}^2/V_{DC}}{j\omega C_{DC}} \qquad (5)$$

Thus, the loop gain with $V_{in} = 90V$ is only 1/9 (-19dB) of the loop gain with $V_{in} = 270V$.

The crossover frequency f_c is also directly proportional to the gain because the gain characteristic has a single pole (-20dB/decade) slope through crossover. Therefore f_c at 90V is also 1/9 of f_c at 270V.

Consider the difficulty covering this span of input voltages (the combined 120V − 220V range limits) without tap switching. The error amplifier gain is set to obtain $f_c = 20$ Hz maximum crossover frequency at the 270V high line. (A much higher f_c is desired but not possible because of input current distortion.) If the supply is then operated at the 90V low line condition, f_c drops to only 2.2 Hz. Control dynamics become unacceptable. The dc bus voltage, V_{DC}, drops well below the desired regulation range at 90V input because the low frequency loop gain is inadequate.

Again, the proper application of line voltage feed-forward can make the loop gain independent of line voltage variation. This makes it easy to achieve 90V − 270V operation with good dynamics and good dc bus regulation without range switching.

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Power/current limit variation: The relatively slow control loop is unable to keep pace with rapid line or load changes. If load power increases rapidly, the control circuit will belatedly try to make up the energy deficit in C_{DC} by drawing excessive current and power from the line for several half-cycles, unless limiting circuitry is provided. Otherwise, line current limits are violated, device current ratings may be exceeded, and excessive power can cause the dc bus voltage to overshoot.

The peak input current is naturally limited because the current programming voltage is clamped by the output voltage capability of the multiplier. The design should set this current programming limit so that 110 - 120% of full load power can be drawn from the line under minimum line voltage conditions.

When the line voltage is high, a fixed current limit allows excessive power input, and dc bus voltage will overshoot with line or load change. A fixed power limit requires the rms current limit to vary *inversely* with V_{in}. This is hard to accomplish without voltage feed-forward.

For example, for the same maximum power, max. rms input current I_{in} should be only 1/3 as much with 270V input as with 90V. But if the peak current limit is set for max. I_{in} needed at 90V, I_{in} at 270V actually increases 30%. This is because V_{sin} at the multiplier input calls for 3 times *larger* current, but the waveform at the multiplier output is clipped at the *peak* input current limit, becoming rectangular in waveshape. Thus the power limit is 4 times larger at 270 V than at 90 V line.

This situation is obviously intolerable, even with a much more limited input voltage range. Additional, rather elaborate control circuits are required to limit current and power, unless input voltage feed-forward is used.

Input Voltage Feed-Forward

It should be apparent by now that input voltage feed-forward is almost a panacea in eliminating a variety of serious problems inherent in the basic high power factor preregulator.

First, without feed-forward, the circuit of Fig. 1 applies voltage V_{sin}, derived from the line input, to one input of the multiplier. This generates a half sine voltage, V_i, patterned after the line voltage waveform and proportional to the amplified output error voltage, V_{ERR}. V_i

programs the input current half sine.

$$V_i = k_m V_{sin} \cdot V_{ERR} = k_m k_{in} V_{in} \cdot V_{ERR} \quad (7)$$

where k_m is the multiplier gain factor, and k_{in} is the input voltage divider ratio.

The current control loop (part of the preregulator block in Fig. 1) establishes I_{in} according to programming voltage V_i and current sense resistor R_{sense}. Vi is attenuated by factor k_i (which equals R_1/R_2 in Fig. 7).

$$I_{in} = k_i V_i / R_{sense}$$

Combining with (7) and let $k_1 = k_m k_{in} k_i$:

$$I_{in} = k_1 V_{in} \cdot V_{ERR} / R_{sense} \quad (8)$$

Assuming reasonably high power factor, with rms values:

$$P_{chg} = P_{in} = I_{in}V_{in} = k_1 V_{in}^2 V_{ERR} / R_{sense} \quad (9)$$

the instantaneous version:

$$p_{chg} = k_1 V_{in}^2 (1 - \cos 2\omega_m t) V_{ERR} / R_{sense} \quad (9a)$$

Eq. (9) shows clearly that "gain" P_{chg}/V_{ERR} varies with V_{in}^2, causing all of the problems mentioned earlier. It also points the way to apply input voltage feed-forward to eliminate this V_{in}^2 dependency: divide Eq. (9) by a voltage proportional to rms V_{in}^2, thus cancelling the V_{in}^2 term in the numerator, as in Eq. (10). The method of implementation is shown in the block diagram of Fig. 6., where terms are defined.

From (9) with the divider added:

$$P_{chg} = \frac{k_1 k_d V_{in}^2 V_{ERR}}{k_s k_f^2 V_{in}^2 R_{sense}} = \frac{k_1 k_2 V_{ERR}}{R_{sense}} \quad (10)$$

$$\text{where} \quad k_d/(k_s k_f^2 V_{in}^2) = \text{divider gain}$$
$$k_2 = k_d/(k_s k_f^2)$$

The feed-forward voltage must be *constant* during each half cycle. This fixes the divider gain during the half cycle in inverse proportion to V_{in}^2 to make the overall loop gain and bandwidth independent of V_{in}. But voltage $V_{sin} = k_{in}V_{in}$ applied to the multiplier is a half sine wave to serve as a pattern to obtain the desired high power factor current waveform.

It must be noted that any 120 Hz ripple in the feed-forward voltage applied to the divider will effectively add to the 120 Hz ripple from the error amplifier to increase the input current waveform distortion, reducing the power factor.
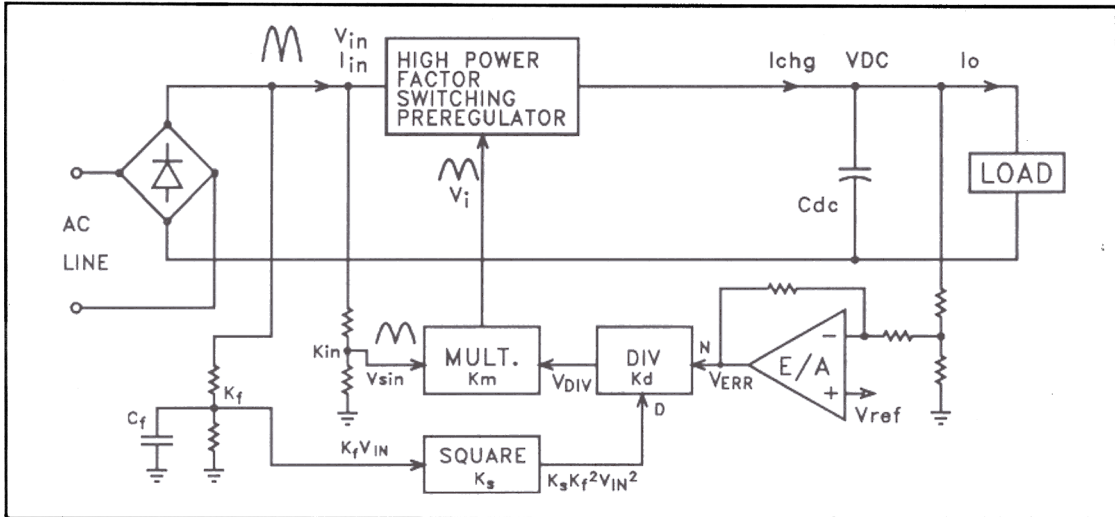
Fig. 6 - High Power Factor Preregulator with Input Voltage Feed-Forward

Capacitor C_f averages the V_{in} waveform and reduces the ripple to an acceptable level. If the time constant $C_f R_{divider}$ is too small, the power factor will be too low. If the time constant is too large, there will be too much feedforward delay, resulting in excessive overshoot and undershoot of the dc bus voltage when the line voltage changes rapidly by a large amount. This is a difficult problem to analyze mathematically, but computer simulation (which is an effective aid for high power factor circuit design) shows that a time constant of one cycle (16 msec at 60 Hz) results in only 4 V overshoot with an instantaneous line change from 180 to 270V, yet is able to achieve a power factor better than .96.

Current Mode Control Problems

Current mode control in its usual implementation is actually "peak inductor current control". When the ripple current is small, the peak inductor current is nearly equal to the average current, which is the actual control objective.

In high power factor preregulator applications, it is desired to control input current. The boost configuration is ideal for current mode control because boost inductor current *is* input current. But buck or flyback circuits are *not* ideal for input current mode control because their inductors are located elsewhere.

(In conventional switching voltage regulator applications, current mode control of *output* current is desired. The buck regulator topology is ideal in this case because the inductor is in the output. But continuous boost and flyback topologies are not well suited because their inductors are not in the output.)

Current mode works by turning off the transistor switch at the point where a voltage derived from the inductor current up-ramp intercepts a relatively constant current programming voltage level. Thus, peak inductor current is controlled. The error between peak and average current is minimized if the ripple current is small but this means the current ramp is shallow and this makes current mode control very noise sensitive.

When current mode control is used in any continuous mode application, slope compensation must be used to ensure stability when duty ratios exceed 0.5. With the boost topology in a high power factor preregulator, slope compensation is needed when the instantaneous line voltage is less than half the output dc bus volts, which occurs for a substantial portion of each line cycle. It is very difficult to achieve slope compensation with the boost preregulator. The inductor current downslope (which determines the amount of slope compensation required) varies with V_{in}, and V_{in} varies tremendously from zero to its large peak value during every line cycle.

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Average Current Mode Control

Middlebrook shows that with conventional current mode control, the current loop bandwidth is 1/6 - 1/3 of the switching frequency, f_s. For f_s of 100 kHz, the current loop crossover frequency, $f_{ci} > 15$ kHz. In conventional voltage regulator applications, this high bandwidth current loop causes the inductor to "disappear" from the small signal model and permits exceptionally high gain-bandwidth in the outer voltage control loop.

But in the high power factor preregulator, the outer loop crossover frequency, f_{co} is limited to less than $20 - 30$ Hz, by loop stability or waveform distortion considerations. This means current loop bandwidth f_{ci} does not really need to be more than 1 kHz.

Taking advantage of the wide frequency separation between f_s and f_{co}, the crossover frequency of the current control loop, f_{ci}, is purposely reduced so that the switching frequency ripple and switching noise is reduced to a negligible level. The duty ratio is controlled by comparing the averaged input current error against a sawtooth waveform.

Fig. 7 shows the inner "average current mode control" loop. The input current signal is compared to the 120 Hz current programming voltage V_i (from the multiplier in the outer loop). 100 kHz variations are averaged out through a current error amplifier. The amplified average current error is compared to sawtooth ramp V_s. The comparator output determines the duty ratio of the boost transistor switch which thereby controls the current.
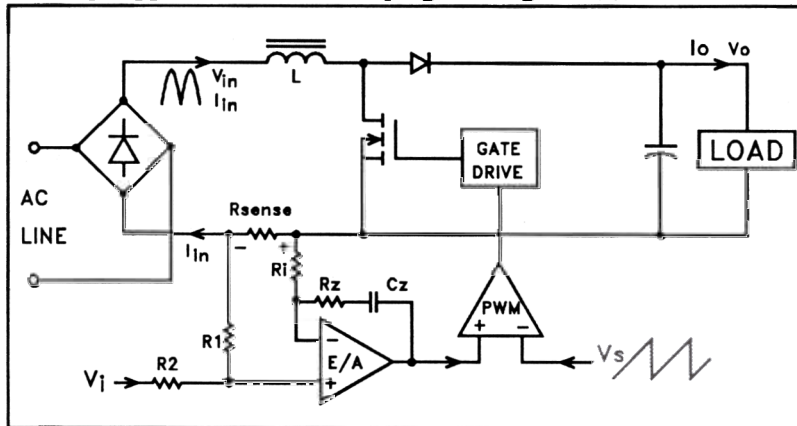
Design approach: The current programming voltage V_i is limited by the multiplier's output voltage swing. This in turn limits the peak input current. The peak voltage across R_{sense} is set by resistor ratio R_1/R_2. For example, suppose a max rms I_{in} of 5 A is desired. If $R_{sense} = 0.2$ Ω, its dissipation is 5 W, and its voltage is 1 V rms, or 1.414 Vpk. If V_i is limited to 3.0 V, an R_1/R_2 ratio of 1.5/3 = 1/2 establishes a peak input current of 7.5 A, with rms of 5.3 Amps.

To achieve current loop stability, the error amplifier gain, $k_e = R_z/R_i$, is flat from below crossover frequency f_{ci} to above the switching frequency, f_s. This is because a -1 slope (from the inductor) already exists at f_{ci}.

The E/A gain at f_s should be such that the 100 kHz ripple and noise at the E/A output is only one tenth the 3 V sawtooth amplitude, hence negligible. Assuming that inductor L = 700 μH and max Δi_{in} = 1 A have been previously determined, then for example:

$$k_e = \frac{R_z}{R_i} = \frac{V_s/10}{\Delta i_{in} R_{sense}} = \frac{3V/10}{1A \cdot 0.2\Omega} = 1.5 \tag{11}$$

Since the loop gain rolls off with a single pole between f_{ci} and f_s, the resulting crossover frequency is:

$$f_{ci} = \frac{V_o}{2\pi L} \frac{k_e R_{sense}}{V_s} = \frac{380 \cdot 1.5 \cdot 0.2}{2\pi \cdot 700 \cdot 3} = 8.6 \text{ kHz} \tag{12}$$

Zero $R_z C_z$ below $f_{ci}/3$ boosts low frequency gain to "average" the current feedback signal, leaving 45° phase margin at f_{ci}.

Some insights: The "average current control" loop operates in the same manner as old fashioned "voltage mode control", except that it: (a) controls current and (b) functions as the inner loop of a two-loop system. Note that the chopped input current in flyback or buck topologies can be averaged and controlled in the same manner. Average current mode control can be applied to any topology even when the inductor current is not equal to the input current. This makes the specific power circuit topology irrelevant to the outer control loop.

Fig. 7 - Average Current Mode Control Loop

In summary, the advantages of "average current mode control" are:

♦ No slope compensation required
♦ Good noise immunity
♦ No peak-avg error - inner loop actually controls "average input current" - even with flyback topology where inductor is not in input.

The one disadvantage is a somewhat reduced current loop bandwidth. This is not a problem in switching preregulator applications, considering the outer loop crossover frequency must be very low compared to the switching frequency.

(The same "average current mode control" technique can be used for multiple loop control in conventional switching voltage regulators using any power circuit topology, but at the cost of reduced current loop bandwidth.)

Sample and Hold

In a conventional switching power supply, the 0 dB loop gain crossover frequency, f_c, must be below 1/4 or 1/5 of the switching frequency, f_s. Otherwise, subharmonic oscillation occurs. This is definitely *not* a problem with a high power factor preregulator—f_c is *decades* below f_s.

In a high power factor preregulator there is a significant ripple component on the dc bus at the 120 Hz line frequency 2nd harmonic. Without sample and hold, the 120 Hz ripple passes through the control loop. This distorts the input current waveform (see Fig. 5). The amount of distortion depends on the 120 Hz loop gain. Also, if the 120 Hz loop gain is more than 1/4 - 1/5, the amplified ripple becomes so large that clipping occurs, impairing performance. Since the loop gain characteristic has a single pole rolloff (-20 dB/decade) in this region, crossover frequency f_c must be less than 1/4 - 1/5 the 120 Hz ripple frequency, or 25-30 Hz.
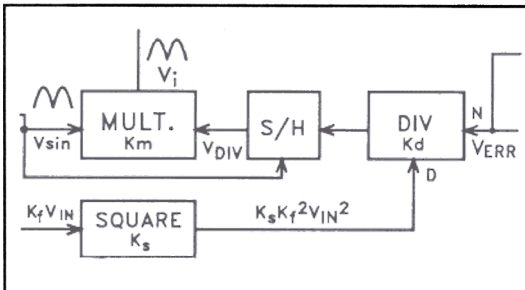
Additional 120 Hz ripple comes from the voltage feed-forward circuit, depending on the time constant of the averaging network. With an f_c of 20 Hz (120Hz/6) and a feed-forward time constant of 8 ms (1/2 line period), a P.F. of .95 - .98, (23% - 14% harmonic distortion) is achievable (see Table I).

If 3% input current distortion is required, f_c must be less than 120Hz/20, or 6 Hz, and the feed-forward time constant must be raised to 40 ms to reduce the harmonic levels from these sources. This *destroys* preregulator dynamics, forcing the addition of sensing/power/current limiting circuitry to override the slow loop.

As shown in Fig. 8, a sample and hold circuit placed at the control input to the multiplier is an excellent solution to this problem. The S/H samples the divider output at the very beginning of each half cycle and holds it for the entire half cycle. Thus the 120 Hz ripple from the error amplifier *and* from the feed-forward squaring circuit are eliminated. The input current programming waveform , V_i, becomes a perfect replica of V_{IN}, without distortion.

The crossover frequency is no longer limited by waveform distortion considerations, but a new limitation appears. The sampling frequency, f_{SH} (120 Hz), becomes the "switching frequency" in the small signal model of the outer loop. Also, a sampling delay is introduced in the control loop. The result is that f_c must be less than $f_{SH}/4$ to $f_{SH}/6$ or loop instability in the form of subharmonic oscillation will occur.

Also, when the sample is taken at the beginning of each half sine, the feed-forward voltage very closely approximates the average value of the input sine wave, regardless of the ripple amplitude. This means that high ripple from the feed-forward averaging network can be tolerated, and the time constant can be even shorter than 8 ms.

On the other hand, the sampling delay slows down the feed-forward response as well as the main loop. Computer simulation shows that *without* S/H and a PF of .96, slightly better dynamic response can be achieved than *with* S/H and a PF approaching 1.0.

The recommendation is: If a Power factor of .95 - .98 is acceptable, don't bother with the sample and hold. On the other hand, to achieve 3% distortion (P.F. = .999), the sample/hold technique is very useful.

Fig. 8 - Control Circuit with Sample and Hold

Small Signal Model

The simplified small signal model of the outer voltage control loop shown in Fig. 9 is accurate at frequencies below the 120 Hz rectified line. Because the loop gain crossover frequency f_c is considerably less than 120 Hz, and decades less than the preregulator switching frequency, factors such as the rolloff of the inner current loop, the ESR zero of the bulk capacitor and the right half-plane zero of the boost topology are so much higher in frequency than f_c they are completely irrelevant to the performance of the outer loop.

The switching preregulator has the small signal output characteristic of a controlled power source, modeled as a current source shunted by a resistor. This source resistance, r, is always equal to dc load resistance R_L, so r changes when R_L changes. The control-to-output gain has a single pole, associated with the bulk filter capacitor. With a resistive load, the parallel combination of r with ac load resistance r_L ($= R_L$) results in a pole frequency $\omega_p = 2/R_L C_{DC}$. This pole frequency will usually be less than 1 or 2 Hz.

However, a load consising entirely of high efficiency switching converters is not a resistive load—it is close to being a constant power load. (Power demand is fixed and independent of the dc bus voltage as long as it is within the input range capability of the downstream converters.) A constant power load has a negative ac resistance equal to its dc load resistance, i.e., $r_L = -R_L$. The parallel combination r_s ($= R_L$) and r_L ($= -R_L$) approaches *infinity*, so the capacitor pole approaches *zero*. The resistances cancel and the model becomes simply a current source driving capacitor C_{DC}, with a slope of -1 from nearly zero frequency to well above the crossover frequency.
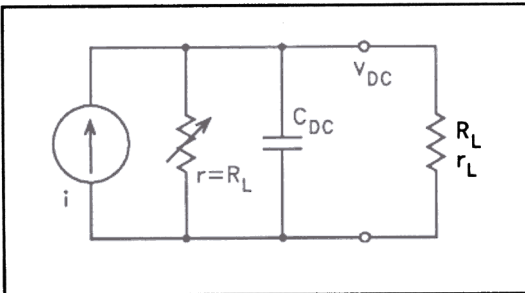

Fig. 9. - Outer Loop Small Signal Model

So r_L could be any value between $+R_L$ and $-R_L$, with the C_{DC} pole somewhere between 0 and 2 Hz. Fortunately, it really doesn't matter, and the gain in the region of interest can be expressed as:

$$v_{DC} = \frac{i_{chg}}{j\omega C_{DC}} = \frac{p_{chg}}{j\omega C_{DC} V_{DC}} \qquad (13)$$

(Note that a constant power source driving a constant power load is open-loop unstable at low frequency. The preregulator must never be tested with a negative resistance load while the voltage control loop is open—it will run away.)

The control-to-output gain also includes the modulator and ac waveshaping multiplier, as well as the feedforward divider and sample/hold, if used—everything from the error amplifier output to the dc bus preregulator output. The gain characteristic of these elements is flat with frequency, although the S/H introduces a delay of less than 1/2 line cycle, ultimately reducing the allowable crossover frequency.

Combining Eq. (13) with the small-signal version of (9) gives the control-to-output gain *without* feedforward:

$$\frac{v_{DC}}{v_{ERR}} = \frac{k_1 V_{in}^2}{j\omega C_{DC} V_{DC} R_{sense}} \qquad (14)$$

Combining Eq. (13) with the small-signal version of (10) gives the control-to-output gain *with* feedforward:

$$\frac{v_{DC}}{v_{ERR}} = \frac{k_1 k_2}{j\omega C_{DC} V_{DC} R_{sense}} \qquad (15)$$

Dimensionally, k_1 is V^{-1}, and k_2 is V^2, which resolves the dimensions of the above equations.

Because the control-to-output characteristic has a near-ideal single pole roll-off, the error amplifier gain should be flat for excellent loop stability. The gain required can be determined without a Bode plot. Simply calculate the arithmetic control-to-output gain at the desired crossover frequency using Eq. (14) at max. V_{in}, or (15) if feed-forward is used. The reciprocal of this number is the error amplifier gain required for a loop gain of 1, which is by definition the crossover frequency. The single 90° phase shift from C_{DC} assures loop stability.

A pole-zero pair could be incorporated in the error amplifier network to improve dc regulation of the dc bus voltage, but this is not recommended. There is no real advantage to

doing this because the low frequency boost cannot follow rapid line or load changes. The dc bus will have the same voltage excursions (although temporary) that would occur without this boost. In either case, the downstream converters will have to operate over the same voltage range. The only way to tighten this range is to (a) employ input voltage feed-forward, and (b) increase the bulk capacitor size, which reduces the loop gain, allowing a corresponding error amplifier gain increase.

Bulk Capacitor Selection and System Performance

In any off-line supply, the input filter capacitor makes up a significant portion of the cost and the volume. Factors entering into the selection of the capacitor and the microFarads required are:

(a) ac line voltage range
(b) Power demand
(b) Holdup time (# of half cycles)
(c) Ripple voltage on dc bus
(d) Regulation of dc bus voltage
(e) Dynamics -- overshoot, undershoot
(f) ac current ratings
(g) ESR

Requirements (a) to (e) collectively determine the total dc bus voltage range the system is expected to operate under, with a variety of line and load conditions.

Conventional low power factor systems: With a full wave rectifier off the 220 V line, or voltage doubler off the 115 V line, the usual dc bus voltage range has a 2 to 1 ratio, from 200 to almost 400 V. Half of this is due to line variation, the other half due to 120 Hz ripple and holdup requirements, if any. Regulation is not possible, but this eliminates the dynamics problems often encountered with regulated systems.

The peak current charging the capacitor at the peak of each line cycle is perhaps 8 times the dc current, I_{DC}. through the dc bus. This is why the input power factor is so bad, but it also causes the rms capacitor current to be extremely high for the power input involved. With present day electrolytics, capacitors usually should be selected on the basis of their rms current rating. When this is done, the capacitance value is usually greater than the

minimal size that otherwise might be used, and should provide a holdup time of one full cycle, 16 msec.

So rms current and holdup time usually dominate capacitor selection. For example with a full wave bridge rectifier, 150 μF is required with 100 W load for 20 msec holdup time to 200V from min 180V rms line. For a voltage doubler, 200 μF is needed for only 16 msec holdup time (two 400 μF in series).

High power factor systems: The $\sin^2$ charging current waveform has a peak-to-peak value only twice the dc current (Fig. 2), so the rms capacitor current is only $.707 \cdot I_{DC}$. Capacitor selection is now based primarily on holdup time, and reliability is much better because rms current is well below the rating.

With an optimized high power factor preregulator with a nominal dc bus voltage of 375 V and 100 W load, only 100 μF is required for 20 msec holdup to a minimum dc bus voltage of 320 V. Ripple is only 7 V_{p-p}. With voltage feed-forward, the preregulator handles line voltage changes from 90 to 270 V with negligible change in dc bus voltage. Instantaneous 2:1 changes in line voltage result in overshoot and undershoot less than 5 V on the dc bus.

When the load changes instantaneously from 100 W down to 20 W, bus voltage rises from 375 to 387 V with no overshoot.

P.F. is 0.97. Loop gain at 120 Hz is -18 dB, and the crossover frequency is 15 Hz.

The above results were obtained by computer simulation, which is an excellent way to experiment with high power factor systems.

The reason that ripple is so low and holdup much better with a smaller capacitor than the low power system is very simple. The capacitor always operates with a bus voltage close to 375 V, even at low line voltage, because of the "bonus" output regulation of the high power factor preregulator. Thus the smaller capacitor consistently stores more energy than in the conventional system at low line. At higher voltage, the ΔV with a given energy withdrawn is smaller than at lower voltage.

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Current Limiting with the Boost Topology

Unlike buck and flyback circuits, the boost topology cannot limit severe overcurrent because there is no series switch between input and output, only a shunt switch. High current occuring with fault load conditions and the start-up inrush current surge charging the bulk capacitor can not be limited or controlled without additional circuitry including a series switch.

Load Overcurrent Limiting: The boost topology can control and limit current only as long as the dc bus voltage, V_{DC}, is greater than v_{in}. If an overcurrent condition exceeds the preregulator power limit established by the control circuit, V_{DC} will eventually be dragged down below the peak value of the AC line voltage. When this occurs, the boost topology loses control. Current will rise rapidly and without limit through the series inductor and rectifier. Ultimately, the inductor will saturate and components will fail. The shunt switch is held *off* by the control circuit, since the current is above the desired level. It can't help to turn the switch ON -- the inductor current will rise even more rapidly and switch failure will occur.

Arguably, the downstream converters will have current limiting capability, eliminating concern about load faults. But a downstream converter or the bulk capacitor might fail. In some systems, the bulk capacitor voltage is bused to other boards or system modules, and there is a good possibility of a short circuit across this high voltage bus.

If it is considered necessary to limit the current to a safe value in the event of a downstream fault, some means external to the boost converter must be provided. This might be an additional series switching transistor or a fuse -- can it act rapidly enough??

Startup Inrush Current Limiting: Before start-up, V_o is zero. When V_{in} is switched on at the input of the boost converter, the bulk capacitor will attempt to charge resonantly to twice V_{in}. If V_{in} happens to be at the peak high-line 220 V condition (370 V) when the supply is turned on, the bulk capacitor will try to resonantly charge to 740 V. The peak resonant charging current through the inductor will be many times greater than normal full load current. To prevent saturation, the inductor must be much larger and more expensive. The boost shunt switch can do nothing to prevent this. The switch should not be turned on at all during start-up, or it will make the situation worse.

The current and voltage overshoot in the start-up scenario described above is intolerable. A fuse is no solution -- the fuse would blow each time to supply is turned on.

There are several methods that may be used to solve the start-up problem:

1. "**Start-up**" **bypass:** A additional rectifier bypassing the the boost inductor and rectifier diverts the start-up inrush current away from the boost inductor, as shown in Fig. 10. The bulk capacitor charges through D_{bypass} to the peak AC line voltage without resonant overshoot and without excessive inductor current. Under normal operating conditions, V_{DC} is higher than peak V_{in}, and D_{bypass} is reverse biased. If load overcurrent pulls down V_{DC}, D_{bypass} conducts, but this is probably preferable to having the boost inductor carry the overload.

Inrush current is high with this technique, limited only by line impedance, the same as a simple capacitor input filter. A resistor in series with D_{bypass} could theoretically limit the inrush, but a resistance large enough to have a significant effect passes most of the start-up inrush back to the inductor.
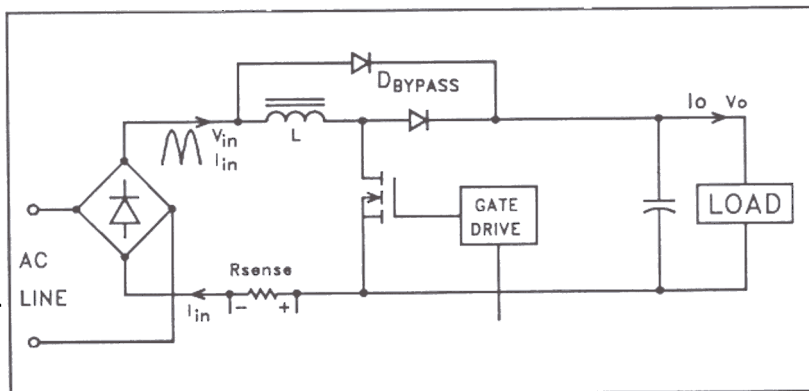

Fig. 10 - Rectifier Bypass of Start-Up Inrush Surge

2. **External inrush limiting circuit:** A thermistor in series with the preregulator input will limit the inrush current, but it has losses and is used only in low power systems. Also, the thermistor cannot respond fast enough to provide protection after a line dropout of a few cycles.

A more efficient approach uses a series input resistor shunted by a Triac or SCR which turns on toward the end of the surge, after the voltage across the inrush limiting resistor diminishes. A control circuit is necessary. This method can function on a cycle-by-cycle basis for protection after a dropout. It is frequently used at higher power levels, but its cost can be excessive for low power applications. It does not protect against load overcurrent.[2]

3. **"Buck or Boost" Topology:** Adding an additional series transistor and free-wheeling rectifier ahead of the boost inductor as shown in Fig. 11 provides a circuit which can limit load overcurrent as well as start-up inrush surge. It operates in *either* boost mode or buck mode. The series (buck) switch functions for current limiting only and has its own control circuit. Under normal conditions the buck transistor is continuously *on* and the circuit functions strictly as a boost converter. During load overcurrent or start-up surge conditions when V_{DC} is below v_{IN}, the shunt (boost) switch is kept continuously *off* by its independent control circuit and the buck switch is pulse width modulated by its overcurrent controller to limit the current to the desired level. Both controllers share the same current sense resistor.

In the buck regulator mode, input current is chopped, generating noise at the input, but this happens only under overcurrent conditions.

(This two-transistor topology can also be used, with a different control circuit, in the buck-boost (flyback) mode. This is achieved by pulse width modulating both switches in a complementary manner, with the buck switch *on* while the boost switch is *off*, and vice-versa. This is a two-transistor flyback configuration. It functions whether V_{DC} is greater or less than v_{IN} so it can be used in a high power factor preregulator supplying a 300 V bus from 220 V line, for example.)

Miscellaneous Considerations

The following considerations are pertinent in designing high power factor circuits:

Power Factor vs. harmonic content: Figure 5 shows the rectified input current waveform with 0.96 Power Factor. This rectified current waveform distortion is caused by the 120 Hz ripple on the dc bus and the 120 Hz feed-forward ripple which are both passed through the control circuit and distort the current programming waveform. As shown in Figure 5, the rectified current waveform distortion is mainly phase-shifted 120 Hz.

However, this 120 Hz *rectified* waveform distortion translates into a 90° leading 60 Hz component and a third harmonic component in the *unrectified* line current on the input side of the bridge rectifier. These two components have the same amplitude. With a Power Factor of 0.96, the 90° leading component is 20% and the 3rd harmonic distortion component is also 20% of the in-phase fundamental.
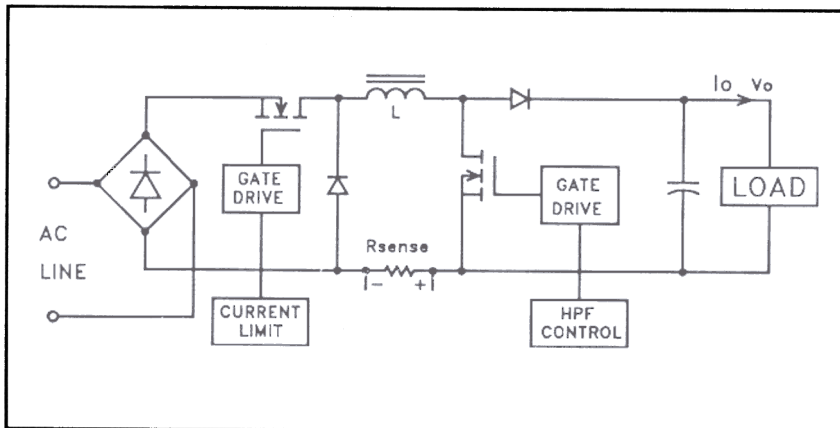

Fig. 11 - "Buck or Boost" Current Limiting Configuration

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The relationship between the total rms line current with its various components and the Power Factor is:

$$I_{rms} = (I_{f0}^2 + I_{f90}^2 + I_{H3}^2)^{1/2}$$

$$\text{P.F.} = I_{f0}/I_{rms}$$

where I_{rms} = total rms current
I_{f0} = in-phase fundamental
I_{f90} = 90° phase-shifted fund.
I_{3H} = third harmonic

Table I shows Power Factor vs. I_{3H} and I_{f90} as a percentage of I_{f0}.

Table I - *Power Factor vs. Phase Shifted and Third Harmonic Components*

P.F.	$\%I_{f90}/I_{f0}$	$\%I_{3H}/I_{f0}$
0.87	40	40
0.92	30	30
0.95	23	23
0.98	14	14
0.997	5	5
0.999	3	3

Limiting and clamping: All of the control circuit elements—error amplifier, multiplier, divider, squaring circuit—have inherent limits on their output voltage swings. This results in waveform clipping and input current or power limiting, depending on where in the control circuit this occurs. Careful planning is required to use these inherent bounds properly to limit peak current and power while avoiding unintended limiting at operating extremes. Referring to Fig. 6:

The multiplier output clips peak V_i, thus limits peak I_{in}. R_{sense} and the divider at the current error amplifier input should be set up so that peak I_{in} is adequate for full load power at minimum V_{in}.

Divider k_{in} should be set so that with min. V_{in} and max. V_{DIV} (or max. V_{ERR} with no feed-forward), peak V_i is just below the multiplier output range limit.

Feed-forward divider k_f should be set in conjunction with the squaring circuit gain, k_s, so that the divider output is near its range

boundaries at extremes of V_{in} and V_{ERR}.

With feed-forward, the error amplifier output limit can be used to limit maximum power input, regardless of Vin.

(Remember that with the boost topology, if an overload is severe enough to pull the output V_{DC} below v_{in}, the boost transistor remains off and current limiting no longer works, unless separate means are provided.)

Control circuit dc offsets: As the control signals propagate through the various control circuit stages, the original dc levels are frequently lost.

The intended zero point of the V_i current programming waveform is lost at the multiplier output. It must be brought into correspondence with the zero current level of the I_{in} waveform as seen across R_{sense}, or the I_{in} rectified sine wave will have its bottom clipped or elevated, resulting in distortion and reduced P.F.

DC offset through the feed-forward squaring and dividing circuits will hurt feed-forward linearity, reintroducing some loop gain and bandwidth variation with V_{in}, and perhaps interfering with input power limiting as set up at the error amplifier output.

The reference voltage at the error amplifier non-inverting input should be at the mid-range of the E/A output swing capability to minimize dc bus voltage offset error. Avoid using a capacitor in series with the E/A feedback to eliminate this offset—it will cause overshoot.

While these offsets can cause great difficulty in achieving very low harmonic distortion, they should be quite managable for P.F. up to 0.98. Watch out for temperature variations of these offsets.

Summary Comparison

High power factor preregulators provide many advantages and eliminate many of the problems compared with a simple capacitor input filter. In some systems, the reduced bulk capacitor cost and savings in the downstream converters because of the much narrower dc bus voltage range will pay for the increased cost of the preregulator.

Table II summarizes the comparison of a high power factor preregulator which can operate from 90 to 270 Volt rms line without range switching, vs. a conventional 90 to 135 V doubler and a 180 to 270 V full wave bridge.

Some aspects of the closed loop involving multipliers, dividers, and sample/hold elements do not fit into existing small signal models. Computer simulation is an ideal tool to evaluate and optimize high power factor circuits as part of the design process.

References

[1] R. D. Middlebrook, "Predicting Modulator Phase Lag in PWM Converter Feedback Loops," *Proceedings of Powercon 8*, pp. H4.1–H4.6, April 1981.

[2] R. Adair, "Incorporate Active Inrush Current Limiting to Improve Reliability and Efficiency of Power Supplies," *Unitrode Application Note U-83*.

[3] Power Electronics Group, California Institute of Technology, "Input-Current Shaped Ac-to-Dc Converters," *Final Report Prepared for NASA*, May, 1986.

[4] B. L. Wilkinson, J. Mandelcorn, "Unity Power Factor Supply," *U. S. Patent #4,677,366*, June, 1987

Table II - *Summary Comparisons*

100 WATT LOAD ON DC BUS

	115 V Doubler	220 V Bridge	High P. F. Preregulator
Line Voltage Range (Volts rms)	90 - 135 V	180 - 270	90 - 270
Bulk Filter Capacitance (μF)	2 x 400 μF	150	100
Holdup Time, milliseconds to min. V_{DC}:	16 ms 200 V	20 200	20 320
Normal dc Bus Voltage Range, V	228 - 381 V	226 - 381	360 - 390
Maximum Bus Ripple Voltage, p-p	18 V p-p	28	
Power Factor	0.6	0.65	0.96

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Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265