

*Designer's Data Sheet*

**TMOS IV**  
**Power Field Effect Transistors**  
**N-Channel Enhancement-Mode Silicon Gate**

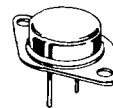
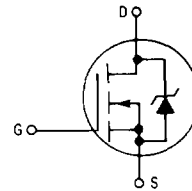
This advanced "E" series of TMOS power MOSFETs is designed to withstand high energy in the avalanche and commutation modes. These new energy efficient devices also offer drain-to-source diodes with fast recovery times. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating area are critical, and offer additional safety margin against unexpected voltage transients.

- Internal Source-to-Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode — Unclamped Inductive Switching (UIS) Energy Capability Specified at 100°C.
- Commutating Safe Operating Area (CSOA) Specified for Use in Half and Full Bridge Circuits
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- DC Equivalent to IRFZ40

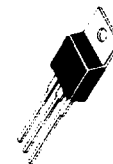


**MTM50N05E**  
**MTP50N05E**

**TMOS POWER FETs**  
**50 AMPERES**  
 $r_{DS(on)} \approx 0.028 \text{ OHM}$   
**50 VOLTS**



**MTM50N05E**  
**CASE 197A-02**  
**TO-204AE**



**MTP50N05E**  
**CASE 221A-04**  
**TO-220AB**

**MAXIMUM RATINGS** ( $T_J = 25^\circ\text{C}$  unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DS}$	50	Vdc
Drain-Gate Voltage ( $R_{GS} = 1 \text{ M}\Omega$ )	$V_{DGR}$	50	Vdc
Gate-Source Voltage — Continuous	$V_{GS}$	$\pm 20$	Vdc
— Non-repetitive ( $t_p \leq 50 \mu\text{s}$ )	$V_{GSM}$	$\pm 40$	Vpk
Drain Current — Continuous ( $T_C = 25^\circ\text{C}$ )	$I_D$	50	Adc
— Pulsed	$I_{DM}$	160	
Total Power Dissipation ( $T_C = 25^\circ\text{C}$ )	$P_D$	125	Watts
Derate above $25^\circ\text{C}$		1	$\text{W}/^\circ\text{C}$
Operating and Storage Temperature Range	$T_J, T_{stg}$	-65 to 150	$^\circ\text{C}$

**THERMAL CHARACTERISTICS**

Thermal Resistance				$^\circ\text{C}/\text{W}$
Junction to Case	$R_{\theta JC}$	1		
Junction to Ambient	$R_{\theta JA}$	30		
	MTM50N05E	62.5		
Maximum Lead Temperature for Soldering	$T_L$	275		$^\circ\text{C}$
Purposes, 1/8" from case for 5 seconds				

**Designer's Data for "Worst Case" Conditions** — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design

# MTM/MTP50N05E

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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### OFF CHARACTERISTICS

Drain-Source Breakdown Voltage (V <sub>GS</sub> = 0, I <sub>D</sub> = 0.25 mA)	V(BR)DSS	50	—	Vdc
Zero Gate Voltage Drain Current (V <sub>DS</sub> = Rated V <sub>DSS</sub> , V <sub>GS</sub> = 0) (V <sub>DS</sub> = 0.8 Rated V <sub>DSS</sub> , V <sub>GS</sub> = 0, T <sub>J</sub> = 125°C)	I <sub>DSS</sub>	—	10 80	μA
Gate-Body Leakage Current, Forward (V <sub>GSF</sub> = 20 Vdc, V <sub>DS</sub> = 0)	I <sub>GSSF</sub>	—	100	nAdc
Gate-Body Leakage Current, Reverse (V <sub>GSR</sub> = 20 Vdc, V <sub>DS</sub> = 0)	I <sub>GSSR</sub>	—	100	nAdc

### ON CHARACTERISTICS\*

Gate Threshold Voltage (V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA) T <sub>J</sub> = 100°C	V <sub>GS(th)</sub>	2 1.5	4 3.5	Vdc
Static Drain-Source On-Resistance (V <sub>GS</sub> = 10 Vdc, I <sub>D</sub> = 25 Adc)	r <sub>DS(on)</sub>	—	0.028	Ohm
Drain-Source On-Voltage (V <sub>GS</sub> = 10 V) (I <sub>D</sub> = 50 Adc) (I <sub>D</sub> = 25 Adc, T <sub>J</sub> = 100°C)	V <sub>DS(on)</sub>	—	1.4 1.3	Vdc
Forward Transconductance (V <sub>DS</sub> = 15 V, I <sub>D</sub> = 25 A)	g <sub>FS</sub>	17	—	mhos

### DRAIN-TO-SOURCE AVALANCHE CHARACTERISTICS

Unclamped Inductive Switching Energy See Figures 14 and 15 (I <sub>D</sub> = 160 A, V <sub>DD</sub> = 25 V, T <sub>C</sub> = 25°C, Single Pulse, Non-repetitive) (I <sub>D</sub> = 50 A, V <sub>DD</sub> = 25 V, T <sub>C</sub> = 25°C, P.W. ≤ 35 μs, Duty Cycle ≤ 1%) (I <sub>D</sub> = 20 A, V <sub>DD</sub> = 25 V, T <sub>C</sub> = 100°C, P.W. ≤ 35 μs, Duty Cycle ≤ 1%)	W <sub>DSR</sub>	—	55 100 35	mJ
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### DYNAMIC CHARACTERISTICS

Input Capacitance	(V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0, f = 1 MHz) See Figure 16	C <sub>iss</sub>	—	3000	pF
Output Capacitance		C <sub>oss</sub>	—	1200	
Reverse Transfer Capacitance		C <sub>rss</sub>	—	400	

### SWITCHING CHARACTERISTICS\* (T<sub>J</sub> = 100°C)

Turn-On Delay Time	(V <sub>DD</sub> = 25 V, I <sub>D</sub> = 0.5 Rated I <sub>D</sub> R <sub>gen</sub> = 4.7 ohms) See Figure 9	t <sub>d(on)</sub>	—	25	ns
Rise Time		t <sub>r</sub>	—	60	
Turn-Off Delay Time		t <sub>d(off)</sub>	—	70	
Fall Time		t <sub>f</sub>	—	25	
Total Gate Charge	(V <sub>DS</sub> = 0.8 Rated V <sub>DSS</sub> , I <sub>D</sub> = Rated I <sub>D</sub> , V <sub>GS</sub> = 10 V) See Figures 17 and 18	Q <sub>g</sub>	55 (Typ)	60	nC
Gate-Source Charge		Q <sub>gs</sub>	30 (Typ)	—	
Gate-Drain Charge		Q <sub>gd</sub>	25 (Typ)	—	

### SOURCE DRAIN DIODE CHARACTERISTICS\*

Forward On-Voltage	(I <sub>SD</sub> = 51 A, V <sub>GS</sub> = 0, di <sub>S</sub> /dt = 100 A/μs)	V <sub>SD</sub>	1.9 (Typ)	2.5	Vdc
Forward Turn-On Time		t <sub>on</sub>	Limited by stray inductance		
Reverse Recovery Time		t <sub>rr</sub>	(Typ)	250	ns

### INTERNAL PACKAGE INDUCTANCE (TO-204)

Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)	L <sub>D</sub>	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25" from the package to the source bond pad)	L <sub>S</sub>	12.5 (Typ)	—	

### INTERNAL PACKAGE INDUCTANCE (TO-220)

Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)	L <sub>D</sub>	3.5 (Typ) 4.5 (Typ)	— —	nH
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad.)	L <sub>S</sub>	7.5 (Typ)	—	

\*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

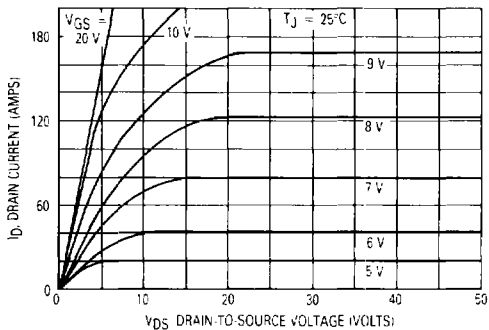


Figure 1. On-Region Characteristics

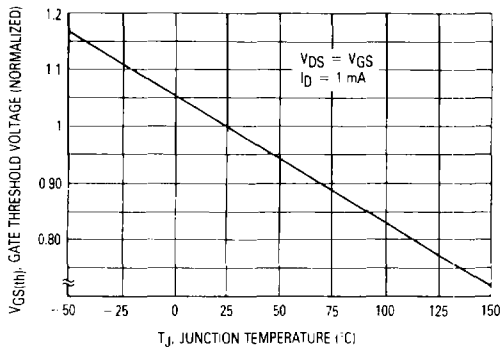


Figure 2. Gate-Threshold Voltage Variation With Temperature

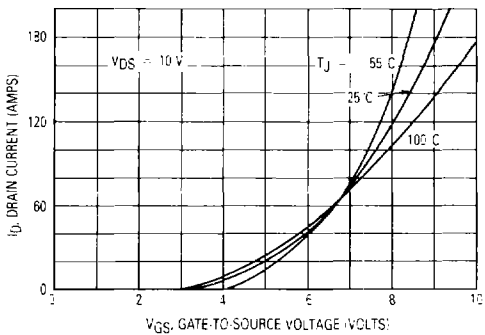


Figure 3. Transfer Characteristics

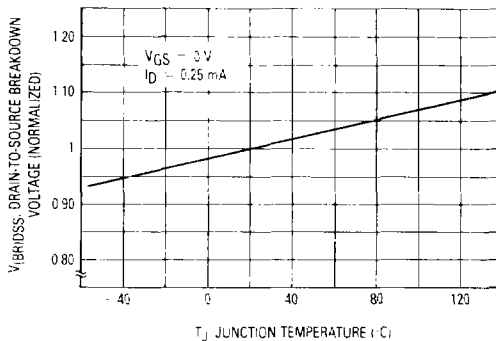


Figure 4. Breakdown Voltage Variation With Temperature

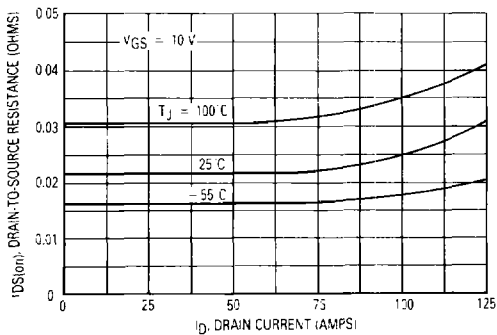


Figure 5. On-Resistance versus Drain Current

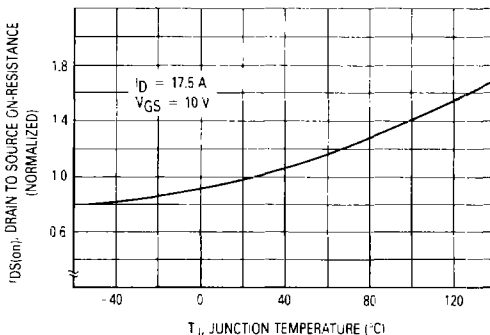


Figure 6. On-Resistance Variation With Temperature

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SAFE OPERATING AREA INFORMATION

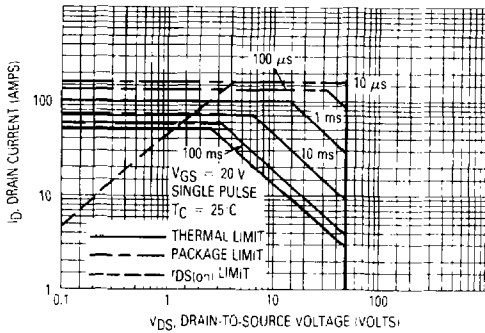


Figure 7. Maximum Rated Forward Biased Safe Operating Area

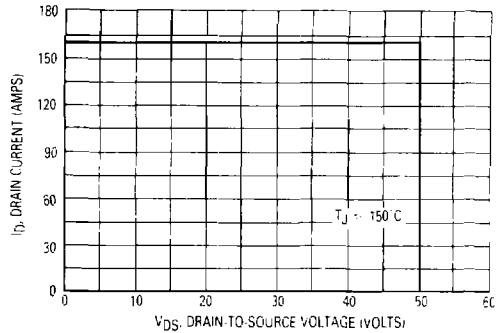


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25 °C and a maximum junction temperature of 150 °C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current,  $I_{DM}$  and the breakdown voltage,  $V(BR)_{DSS}$ . The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

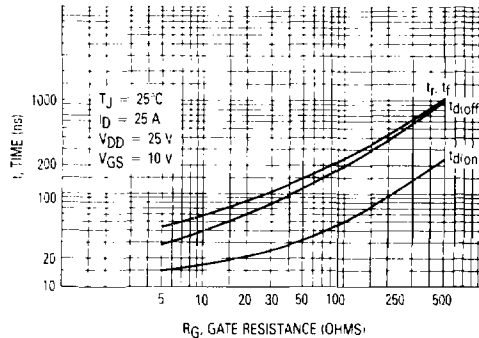


Figure 9. Resistive Switching Time Variation versus Gate Resistance

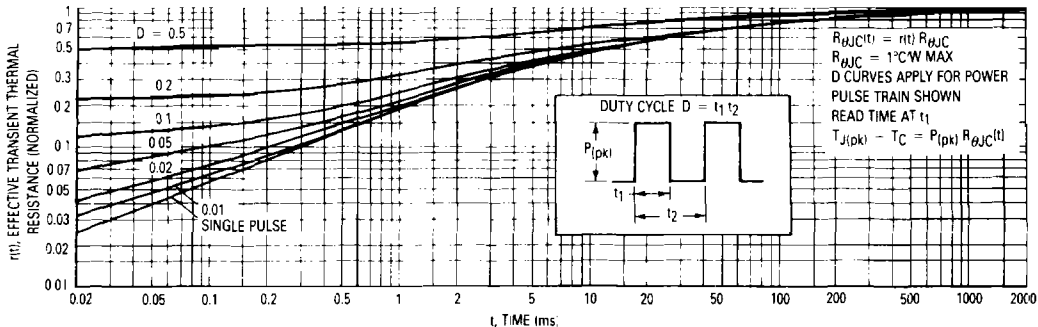


Figure 10. Thermal Response

COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 12 defines the limits of safe operation for commutated source-drain current versus re-applied drain voltage when the source-drain diode has undergone forward bias. The curve shows the limitations of  $I_{FM}$  and peak  $V_{DS}$  for a given rate of change of source current. It is applicable when waveforms similar to those of Figure 11 are present. Full or half-bridge PWM DC motor controllers are common applications requiring CSOA data.

Device stresses increase with increasing rate of change of source current so  $di_s/dt$  is specified with a maximum value. Higher values of  $di_s/dt$  require an appropriate derating of  $I_{FM}$ , peak  $V_{DS}$  or both. Ultimately  $di_s/dt$  is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during  $t_{rr}$  as the diode goes from conduction to reverse blocking.

$V_{DS(pk)}$  is the peak drain-to-source voltage that the device must sustain during commutation;  $I_{FM}$  is the maximum forward source-drain diode current just prior to the onset of commutation.

$V_R$  is specified at 80% of  $V_{(BR)DSS}$  to ensure that the CSOA stress is maximized as  $I_S$  decays from  $I_{RM}$  to zero.  $R_{GS}$  should be minimized during commutation.  $T_J$  has only a second order effect on CSOA.

Stray inductances in Motorola's test circuit are assumed to be practical minimums.  $dV_{DS}/dt$  in excess of 10 V/ns was attained with  $di_s/dt$  of 400 A/ $\mu$ s.

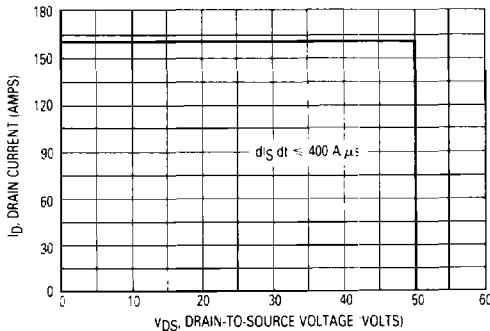


Figure 12. Commutating Safe Operating Area (CSOA)

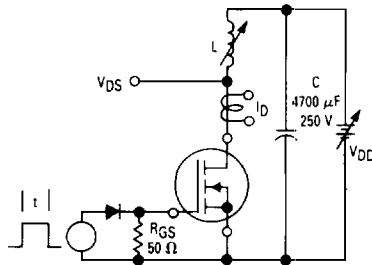


Figure 14. Unclamped Inductive Switching Test Circuit

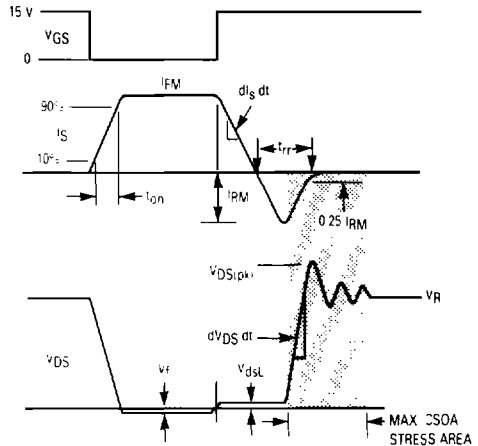


Figure 11. Commutating Waveforms

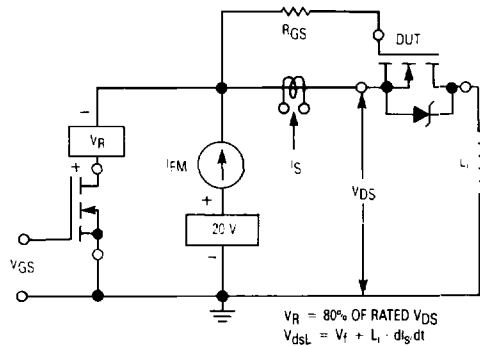


Figure 13. Commutating Safe Operating Area Test Circuit

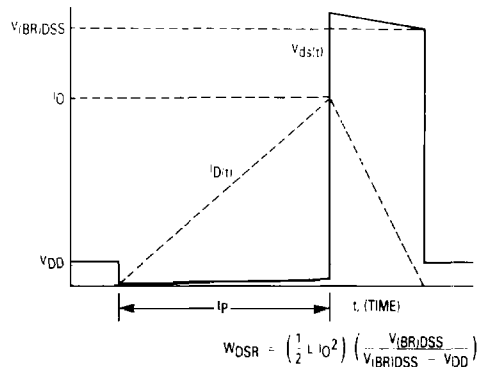


Figure 15. Unclamped Inductive Switching Waveforms

MTM/MTP50N05E

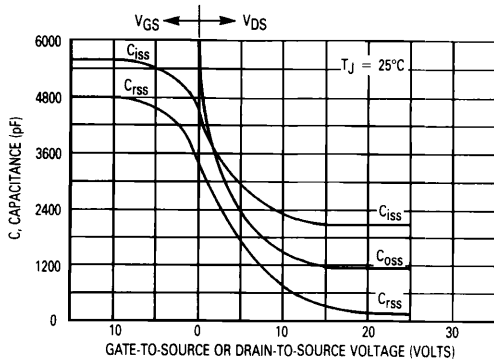


Figure 16. Capacitance Variation

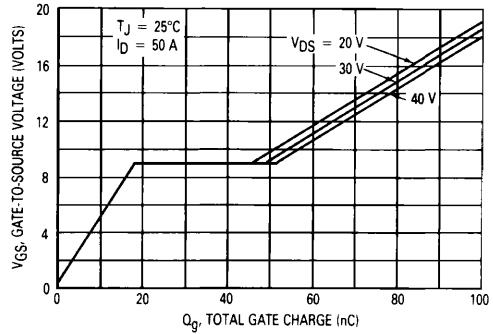
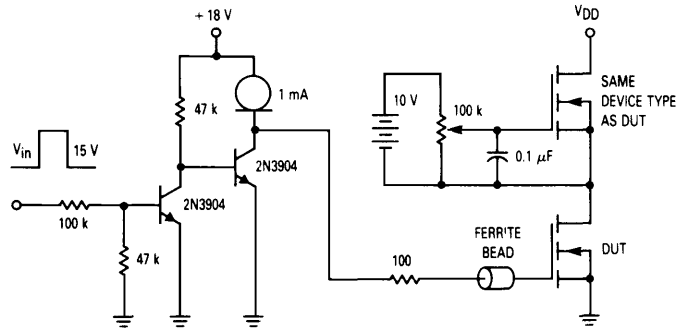


Figure 17. Gate Charge versus Gate-to-Source Voltage



$V_{in} = 15\text{ V}_{pk}$ ; PULSE WIDTH  $\leq 100\ \mu\text{s}$ , DUTY CYCLE  $\leq 10\%$

Figure 18. Gate Charge Test Circuit

### OUTLINE DIMENSIONS

**CASE 197A-02  
MTM50N05E**

STYLE 3:  
PIN 1 GATE  
2 SOURCE  
3 SOURCE  
CASE DRAIN

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	38.36	39.37	1.510	1.550
B	19.31	21.08	0.760	0.830
C	6.35	8.25	0.250	0.325
D	1.45	1.60	0.057	0.063
E	1.53	1.77	0.060	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	25.15	26.67	0.990	1.050
U	3.84	4.19	0.151	0.165

**CASE 221A-04  
MTP50N05E**

STYLE 5:  
PIN 1 GATE  
2 DRAIN  
3 SOURCE  
4 DRAIN

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.86	12.28	0.390	0.485
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.86	0.095	0.195
H	2.90	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
M	4.83	5.32	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

NOTES:  
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
2. CONTROLLING DIMENSION: INCH.  
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.