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CHAIRMAN'S MESSAGE

On behalf of the conference committee, I would like to welcome you to the 13th International Symposium on Power Semiconductor Devices and IC's (ISPSD'01) in Osaka. Following very successful meetings in Toronto in 1999 and in Toulouse in 2000, the ISPSD returns to Japan again. Since the establishment of ISPSD which was held in Tokyo in 1988, the ISPSD has continued to make progress and has today become the most important international conference in the field of power semiconductor devices and IC's. This symposium serves not only as a forum for expert discussions on the latest power device developments but also as a place where participants from all over the world can meet and exchange information and opinions.

ISPSD'01 is the first of the 21st century. In commemoration of this, the organizing committee set up the "ISPSD Contributory Award" for ISPSD members who have made outstanding contributions to launching and organizing the ISPSD from the very beginning. ISPSD'01 is expected to be even more significant and more suggestive for the development of power semiconductor devices in the new century. From such a view point, two plenary sessions and a workshop have been organized. The plenary sessions will feature invited presentations on six topics by leaders in the power electronics field. These are Transmission and Distribution by Dr. Rahul Chokhawala, Pulsed Power by Prof. Shozo Ishii, Car Electronics by Prof. John G. Kassakian, EMI/EMC by Prof. Tamotsu Ninomiya, Transportation by Dr. Ingo Herbst, and Home Appliances by Dr. Teruya Tanaka. The workshop will provide an opportunity to discuss road maps of power semiconductor development in the early 21st century. For discussion purposes, participants will be divided into four groups, high

power devices, discrete power devices, integrated power devices and radio frequency power devices. Furthermore, at the dinner banquet, we have been very fortunate in securing a Keynote Speech by Dr. Kunihiko Sawa, the president of IEE Japan.

The program committee received 140 abstracts. The international nature of the forum is reflected in the regional distribution of the submitted papers, from 17 countries in total; 23% from Europe, 25% from North America, 14% from Asia and 38% from Japan. From the abstracts, 43 papers were accepted for oral presentation with another 53 accepted as poster session papers. These papers will be presented during the four day-session. “Best Paper Award” and “Young Researcher Award” will be presented to excellent papers. The winners of the “Best Paper Award” will be selected from all the presented papers, while the “Young Researcher Award” will be presented to candidates who are 30 years old or younger.

To conclude, I would like to express my sincere appreciation to the members of the Program and Steering Committees for their outstanding job they have done in planning and arranging the 2001 forum. It is with great pleasure that I extend a warm welcome to all of you attending the ISPSD’01 in Osaka.

Yoshitaka Sugawara
General Chairman

ORGANIZATION OF ISPSD'01

ORGANIZING COMMITTEE:

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H. Uchida	Nihon Inter Electric Corp.

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M. Watanabe	Komatsu Electronic Metals Co., Ltd.
T. Watanabe	Railway Technical Research Institute
T. Yamao	Meidensha Corp.
F. Yokoyama	Oki Electric Industry Co., Ltd.
S. Yoshida	Shindengen Electric MFG. Co., Ltd.
K. Yoshinaka	Fujitsu Ltd.
K. Sawa	IEE of Japan
A. Tsuboi	IEE of Japan
M. Horikoshi	IEE of Japan
S. Ishii	IEE of Japan
M. Kobayashi	IEE of Japan

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G. Charitat	LAAS/CNRS
W. Fichtner	Swiss Federal Institute of Technology
L. Lorenz	Infineon Technologies
H. Ohashi	Toshiba Corp.
T. Ohmi	Tohoku University
M. Okamura	Japan Advanced Institute of Science and Technology, Hokuriku
C.A.T. Salama	University of Toronto
M.A. Shibib	Lucent Technologies
Y. Uchida	Fuji Electric Co., Ltd.
R.K. Williams	Advanced Analogic Technologies, Inc.

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Vice-Chairman:

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K. Sakamoto	Hitachi Ltd.
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H. Uramoto	ROHM Co., Ltd.
S. Nagao	Matsushita Electronics Corp.
T. Sakakibara	Denso Corp.

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H. Iwamoto	Program Committee Chairman
Y. Seki	Program Committee Vice-Chairman

IEE of Japan:

M. Kobayashi	IEE of Japan, Secretariat

PROGRAM COMMITTEE:

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Y. Seki	Fuji Electric Co., Ltd.
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SPONSORSHIP

The ISPSD '01 is sponsored by the Institute of Electrical Engineers of Japan and co-sponsored by IEEE Electron Devices Society, in cooperation with the Institute of Electronics Information and Communication Engineers of Japan and the Japan Society of Applied Physics.

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SYMPOSIUM DATE AND SITE

Date: **June 4-7, 2001**
Site: Osaka International Convention Center
5-3-51 Nakanoshima, Kita-ku, Osaka, 530-0005, Japan
Phone: +81-6-4803-5555, Fax: +81-6-4803-5620

OFFICIAL LANGUAGE

The official language is English and there will be no facilities for simultaneous translation.

REGISTRATION

REGISTRATION DESK

During the symposium, the registration desk will be open as following at Osaka International Convention Center.

June 3 (Sun.)	18:00 ～ 20:00	5F-Main Hall Foyer
June 4 (Mon.)	8:00 ～ 17:00	5F-Main Hall Foyer
June 5 (Tue.)	8:00 ～ 17:00	5F-Main Hall Foyer
June 6 (Wed.)	8:00 ～ 17:00	5F-Main Hall Foyer

REGISTRATION FEE

All applications fee should be accompanied by full payment of the registration fee in Japanese yen. Advanced registration fee is applied to those remittance by April 1, 2001.

	By April 1	After April 2
IEEJ, IEEE Member	¥40,000	¥45,000
Non-Member	¥45,000	¥50,000
Student*	¥10,000	¥15,000
(Student fee does not include banquet)		
Student, Accompanying Person Banquet	¥12,000	¥12,000
Extra Proceedings	¥10,000	¥10,000
Technical Tour	¥7,000	¥7,000

* For student registration, photocopy of current student ID is requested.

Registration fee includes attendance at the technical sessions, one copy of the Proceedings and banquet.

APPLICATION

Application for registration can be made by completing and submitting the enclosed REGISTRATION FORM in the booklet either in advance or at-door. Please return it to the Secretariat for ISPSD'01 together with a copy of your Bank's remittance advice. Send to: Secretariat for ISPSD'01
c/o Business Center for Academic Societies Japan
5-16-9 Honkomagome, Bunkyo-ku, Tokyo 113-8622, Japan
Phone: +81-3-5814-5800 FAX: +81-3-5814-5823
e-mail: ispsd@bcasj.or.jp

REMITTANCE

Please remit by bank transfer to the following account.
A/C No.: 2377278
A/C Name: ISPSD 2001
The DAI-ICHI KANGYO BANK LTD., Hongo Branch
Payment of registration and other fee should be made in Japanese yen.
Please attach a copy of your bank's receipt to your REGISTRATION FORM to avoid possible trouble. Lack of this evidence (a copy of your bank's receipt) is not tolerated as the application. For overseas attendee only, payment can be made by major Credit Cards(American Express, Visa, MasterCard, and Diners Club).

CONFIRMATION AND RECEIPT

Upon receiving your form and fees, the Steering Committee will send you a receipt. Please bring your receipt (Confirmation card) to the registration desk of the Symposium site.

CANCELLATION OF REGISTRATION

You are requested to notify the committee of your cancellation. When the written notice is received by April 1, 2001, the cancellation will be accepted and a refund of fees will be made after deducing a handling charge of ¥5,000. If you remit by bank transfer, your A/C No., A/C Name, Bank Name (Address) should be notified.

ISPSD'01 WORKSHOP
"Technology Roadmap of Power Devices/ICs"

(5F Multi Purpose Hall & 10F 1008-9)

The workshop consists of four workshop group panel discussions in parallel, covering the distinguished fields of power devices/ICs and their applications. The discussions will start from the technology roadmap, established at ISPSD'96 Hawaii, which can be downloaded in pdf-format from the ISPSD'01 Homepage (http://www.rdd.kepco.co.jp/ispsd).

Workshop Group 1 "High Power Devices"

Chairperson: Hansruedi Zeller, ABB
Vice-chairperson: Hideo Matsuda, Toshiba

This workshop will start from the device roadmap laid out at ISPSD'96 in Maui, Hawaii. The purpose is to review and refresh the roadmap for high power bipolar devices, IGBTs and other MOS controlled devices and extend it for another 5 year period. Panelists will present the system requirements in major application areas such as power transmission and distribution, industrial motor drives, traction and electrical vehicles. This will then be translated into device requirements in terms of electric and thermal properties, packaging, standardization vs. integration, reliability and robustness.

Workshop Group 2 "Discrete devices"

Chairperson: Leo Lorenz, Infineon
Vice-chairperson: Mutsuhiro Mori, Hitachi

The main focus in this workshop is a discussion about the future technologies (Si & SiC based materials), device concepts and packaging ideas on discrete devices. For power MOSFETs the future concepts might be very different between the ultra low voltage (VBr << 20 V) devices; the low voltage (VBr < 80 V) devices and high voltage (VBr > 300 V) devices. The main technology drives in the low voltage devices are the car applications and the DC/DC converters. In the high voltage and the CoolMOS concept will compete to the conventional power MOSFET structure and the fast switching IGBTs. The fast switching diode is still a drawback in many applications. In this meeting future diode concepts including SiC diodes will be discussed. In many applications the power density is increasing drastically which raises up new ideas on chip contacting technologies. The opening of this session will be done by short statements of experts on different devices followed by the group discussion. The outcome will be roadmaps of future device concepts/ideas in this very high volume market.

Workshop Group 3 "Integrated Power Devices"

Chairperson: Ayman Shibib, Lucent Technologies
Vice-chairperson: Hisao Shigekane, Fuji Electric

The focus of the Integrated Power Devices workshop is to address the issues relating to the system integration at the chip, package and module levels. At the chip or power IC level: process technologies, materials (including SOI) and devices will be considered from the perspective of current vesus future need and capabilities.
Similarly, an alternative to the system-on-chip, namely system-in-package or integrated module approach will be discussed.
The session will start with a review of the summary of the Power ICs Group report of ISPSD'96 Hawaii workshop, panel members' presentations followed by open discussions with audience participation. The goal of the session is to establish the basis of a technology roadmap of integrated power devices for the next 5 years.

Workshop Group 4 "RF power devices"

Chairperson: Colin Warwick, Lucent Technologies
Vice-chairperson: Isao Yoshida, Hitachi

A panel of international experts will lead "Gr.4. RF power devices workshop". The goal is to formulate a technology roadmap for RF power devices, including Si LDMOS, GaAs HBT, HEMT, MESFET, GaN & SiC devices for the next five years. The experts come from both industry (semiconductor suppliers and consumers) and academia.
The agenda is:
1. Short presentation by each panel member to inform and challenge the workshop participants.
2. Open discussion leading to a consensus on where technologies are and where they will evolve.

The resulting roadmap should be a very valuable planning tool for consumers and producers of RF power semiconductor devices.

INVITED PRESENTATIONS

Topic field	Title	Speaker
Power Transmission and Distribution	Power Semiconductors in Transmission and Distribution Applications	Mr. Rahul Chokhawala, ABB Semiconductors AG, Switzerland
Pulsed Power	Pulsed Power Application assisted by Power Semiconductor Devices	Dr. Shozo Ishii, Tokyo Institute of Technology, Japan
Car Electronics	The Future of Electronics in Automobiles	Dr. Jhon G. Kassakian, The Massachusetts Institute of Technology, USA
EMI	EMI Issues in Switching Power Converters	Dr. Tamotsu Ninomiya, Kyushu University, Japan
Transportation	Status and Future Trends of Propulsion Systems for Mass Transportation and their Correlation to Power Semiconductors	Dr. Ingo Herbst, ADtranz, Switzerland
Home Appliances	Environment Friendly Revolution in Home Appliances	Dr. Teruya Tanaka, Toshiba Corporation, Japan

AWARDS

BEST PAPER AWARD:

The Best Paper Award will be granted to the most outstanding paper presented at the ISPSD'01. This award is devised in recognition of original paper contributions with superior contents and quality. Selection for the award is based on the full paper contents and will take place in the period between ISPSD'01 and ISPSD'02. The Best Paper Award will be granted to the honored author(s) in a special ceremony during the ISPSD'02.

YOUNG RESEARCHER AWARD:

Young Researcher Award will be granted to two outstanding orally-presented papers at ISPSD'01. The applicant(s) must specially request their paper(s) to be considered for young Researcher Award at the time of the full paper submission. They should be 30 years old or younger at the time of presentation. The award will be presented at the closing session.

BANQUET

Wednesday, June 6, 6:30-9:00 pm., SANRAKU Room (2F) in Rihga Royal Hotel Osaka.

We will invite Dr. Kunihiko Sawa, the President of The Institute of Electrical Engineers of Japan, as a banquet speaker for keynote address in the power device field. In commemoration of the first ISPSD in the 21st century, the 'ISPSD Contributory Award' is established, and the award will be presented at the banquet. Also, traditional Japanese puppet show (Ningyo Joruri) will be provided as an attraction.

TECHNICAL TOUR

Date & Hours : June 8(Fri) 9:00～18:30
Tour Highlights:
Sharp Corp.(Memorial Hall & Technology Hall, Factory of manufacturing LCD driver IC)
Memorial hall was established in 1981 in honor of Sharp's founder, Tokuji Hayakawa. Exhibited here are historic products, including Japan's first crystal radio, the world's first electronic calculator, etc. In technology hall, Sharp's latest technological developments such as solar cells and LCD technologies are introduced in an easy-to-understand. (http://sharp-world.com/sc/event/showroom/tenri/eng/mthall.html)
Horyu-ji Temple
Its main hall and the five-storied pagoda are considered to be the oldest wooden structures in the world. The temple was designated as one of the first World Cultural Heritage in Japan by the UNESCO.
Todai-ji Temple
Its colossal wooden structure is dedicated to "Big Buddha," a 15m-high bronze statue. Designated as the World Cultural Heritage.
Fare: ￥7,000 per person (Box lunch included)
Getting together : the lobby of Rihga Royal Hotel June 8, 9:00 a.m.
Minimum attendance for operation - 30 persons
Those who wish to join this tour may sign up the registration form.

TRAVEL INFORMATION

OFFICIAL TRAVEL AGENT

JTB Corp. has been appointed as the Official Travel Agent for the Symposium and will handle all related travel arrangements including hotel accommodation.
Inquiries and applications concerning arrangements should be addressed to:

JTB Corp.
Tours & Convention Division, Kansai District
Nittochi-Dojima Bldg.
1-4-19 Dojimahama, Kita-ku
Osaka 530-0004, Japan
Tel: +(81)6-6345-9516 Fax: +(81)6-6345-0910
Email: itdw_ec1@kns.jtb.co.jp

HOTEL ACCOMMODATION

JTB has reserved a sufficient number of rooms at the following hotels for Symposium participants at special discount rates. Those persons who wish to apply for hotel reservation are requested to complete the enclosed application form, and send it to JTB not later than May 7 2001 with the necessary deposit(10,000 yen per room).

Hotel assignment will be made on a first-come, first-served basis.

Daily room charges are as follows:

Name of hotel	Room Rate(Japanese yen)		Access to the Conference site
	Single	Twin	
Rihga Royal Hotel	ST ¥10,500 DX ¥15,000	¥19,000	1min. on foot
Hotel NCB	¥6,420	¥10,430	3min. on foot
Hotel Links Osaka & Spa	¥6,300	¥11,000	7min. on foot

ST = Standard DX = Deluxe

Note:
1) Above rate includes service charge, and tax.
2) The deposit of ¥10,000 will be deducted when settling the bill with the hotel.
3) If your desired hotel (1st and 2nd choice) is already fully occupied, we will reserve for you another hotel instead.
4) Single : 1-bed Room
5) Twin : 2-bed Room

Cancellation
If you want to cancel your hotel, a written notification should be sent directly to JTB.
The deposit will be refunded, but the following cancellation fees will be charged depending on when the notification is received by JTB.

At least 9 days before the first night of stay
.....¥1,000 per room
8-2 days before
.....20% of the daily room charge
(minimum: ¥2,000)
One day before
.....50% of the daily room charge
The same day, or no notice given.
.....100% of the daily room charge

GENERAL INFORMATION

PASSPORT AND VISAS

All foreign visitors entering Japan must possess valid passports. Participants requiring visas should apply to Japanese Consulate or Missions in their countries prior to departure. For details, participants are advised to contact their travel agencies.

WEATHER AND CLOTHING

The climate in Osaka on June is hot and humid with an average temperature of 25°C (76°F) and humidity of 70%. A Shirt or blouse with half-length sleeves is suggested. Because the rooms in the hotel are air-conditioned, long-sleeved garments will be useful.

FOREIGN CURRENCY EXCHANGE

Most foreign currencies and traveler's checks can be exchanged at the airport, hotels, or banks. A passport is required for currency exchange services. Traveler's checks are exchanged at a more favorable rate than cash. The Organizing Secretariat will accept only Japanese yen.

TIPPING

In Japan the service charges are included in hotel and restaurant bills.

ELECTRICITY

The standard electrical voltage in Japan is 100V(AC), 60Hz in western Japan(Osaka), 50Hz in eastern Japan(Tokyo).

TRANSPORTATION TO CONFERENCE VENUE (RIHGA ROYAL HOTEL)

The most convenient and economical means to Osaka is to take a direct flight to Kansai International Airport.
From Kansai International Airport to Osaka;

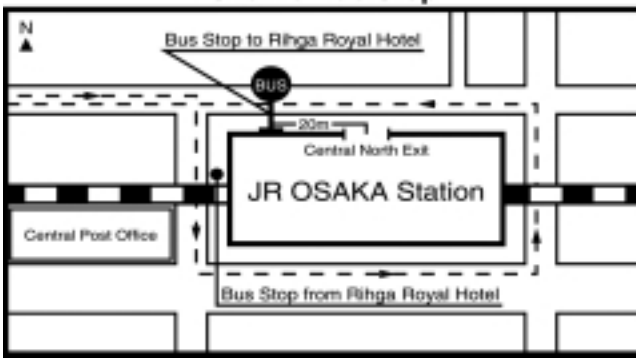
● **JR-West Japan [KIX (Kansai Int'l Airport) → JR (Japan Railways) Osaka Station (55min.)]**
Special Limited Express "Wings" : ￥1,160
(Optional reserved seat additional ￥500)
From Osaka station, take either taxi (10min. approx. ￥700-1,000) or Rihga Royal Hotel Shuttle Bus (every 20min. no charge)

● **Nankai Railway [KIX → Nankai Namba Station (29min.)]**
Airport Express Train "Rapi:t" :
Super seat ￥1,700 Regular seat ￥1,400
From Namba Station, take either taxi (20min. ￥1,500-￥2,000) or proceed to subway Midosuji Line.
Buy a ticket for ￥230 and go three stops (toward Senri Chuo) to Yodoyabashi Station.
From here, go outside exit #4 and take either Rihga Royal Hotel Shuttle Bus (every 15 min. no charge) or taxi (5-8 min. ￥700-800).

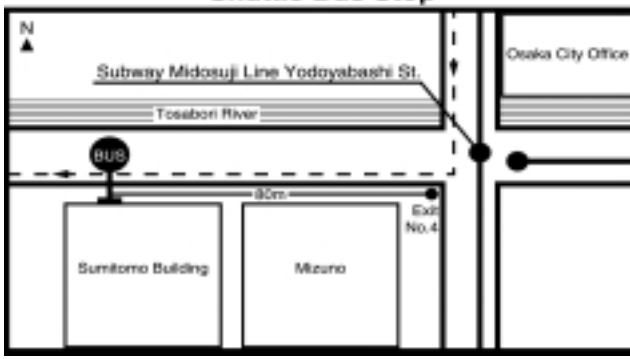
The Rihga Royal Hotel Shuttle Bus runs from 07:45 until 21:50.

☆ **Shuttle Bus Stop**

JR Osaka Station ~ Rihga Royal Hotel Shuttle Bus Stop



Yodoyabashi Subway St. ~ Rihga Royal Hotel Shuttle Bus Stop

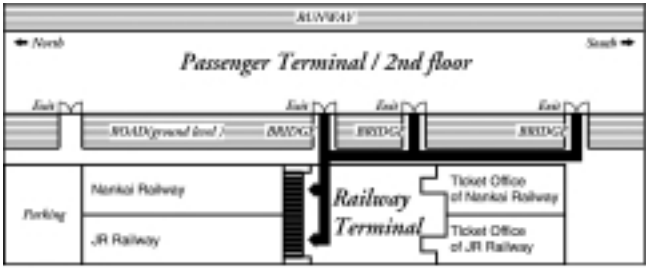


● **Airport Limousine Bus [KIX → Rihga Royal Hotel (80min.)]**
Limousine Bus : ¥1,300
(Leaves at 17:45 and only runs once in a day)

● **Airport Limousine Bus [KIX → Harbis Osaka (Osaka Station) (60min.)]**
Limousine Bus : ¥1,300
(It's runs every 20-30min.)

Travelers who are planning to stay at Hotel NCB, or Hotel Links & Spa, take taxi from Osaka Station.
(5-10 min. approx. ¥700-1,000)

☆ **Kansai International Airport Floor Map**



Participants arriving at New Tokyo International Airport (NARITA) may choose from the following three alternatives ;

- A limited number of domestic flights to Osaka Airport is available at NARITA. Board on a domestic flight to Osaka Airport. Take an airport limousine to Osaka.

- From NARITA, take an airport limousine to HANEDA Airport which takes about 100 minutes. Board a domestic flight to Osaka Airport and take an airport limousine to Osaka.

- Take an airport limousine or a Narita express train to JR Tokyo Station, the traveling time is about 100 minutes and 60 minutes, respectively. Board JR Shinkansen (Bullet Train)to JR Shin-Osaka Station, which runs every 15 minutes; the traveling time is 3 hours.

OSAKA, HOME-PAGE

Osaka city has a home page : http://www.city.osaka.jp/index2.html. At this web site, you can get various information: city history, transportation, tourist information.

OPTIONAL TOURS

The following tours are planned for participants and accompanying persons. For reservations, please contact JTB Corp. (JTB).

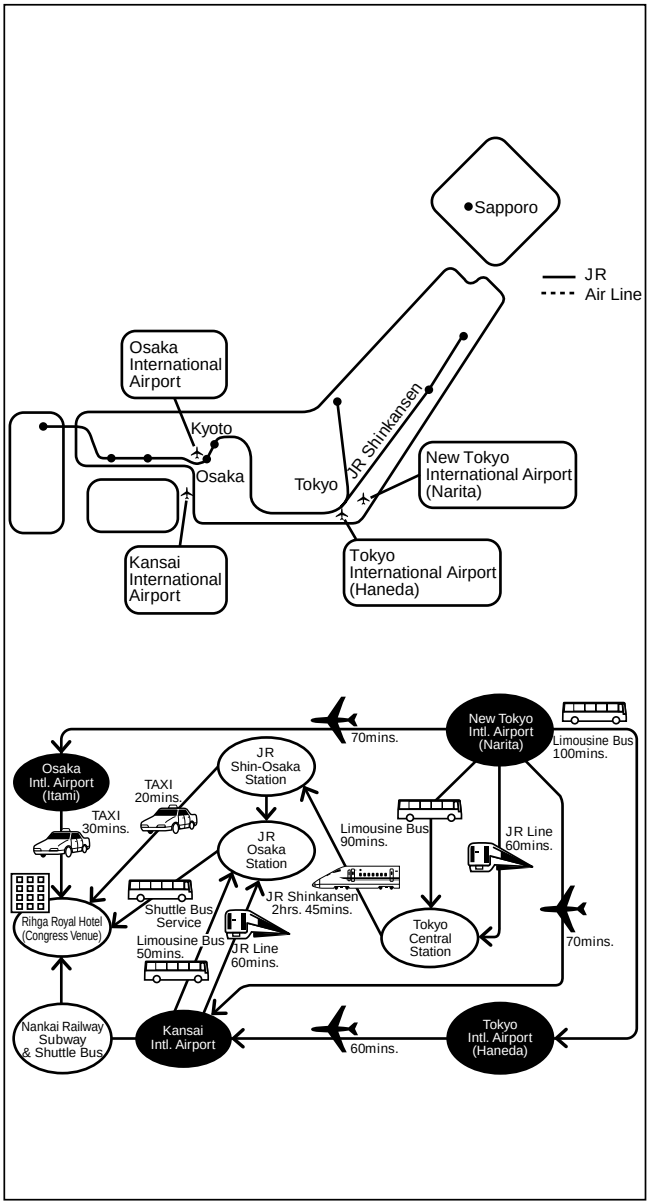
OP-1: KYOTO 1DAY TOUR
*Minimum attendance for operation - 2 persons
Date & Hours : Daily (07:30～18:30)
Departure point: Rihga Royal Hotel
(Tour ends upon arrival at JR Osaka Station at around 18:30)
Fare : ￥14,500 per person (Lunch included)
Places of visit: Nijo Castle, Golden Pavilion, Kyoto Imperial Palace, Kyoto Handicraft Center, Heian Shrine, Sanjusangendo Hall, Kiyomizu Temple

OP-2: NARA HALF-DAY TOUR
*Minimum attendance for operation - 2 persons
Date & Hours : Daily (12:00～18:00)
Departure point: Rihga Royal Hotel
(Tour ends upon arrival at Kintetsu Namba Station at around 18:00)
Fare : ￥9,700 per person
Places of visit: Todaiji Temple, Kasuga Shrine

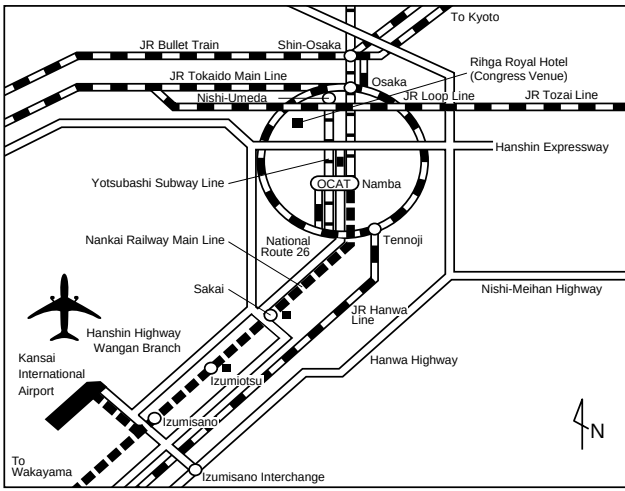
OP-3: WALKING IN OSAKA MORNING
*Minimum attendance for operation - 2 persons
Date & Hours : Daily (8:00～12:00)
Departure point: Rihga Royal Hotel
(Tour ends at JR Osaka Station)
Fare : ￥8,900 per person
Places of visit: Osaka Castle, Aqua Liner (Pleasure Boat)

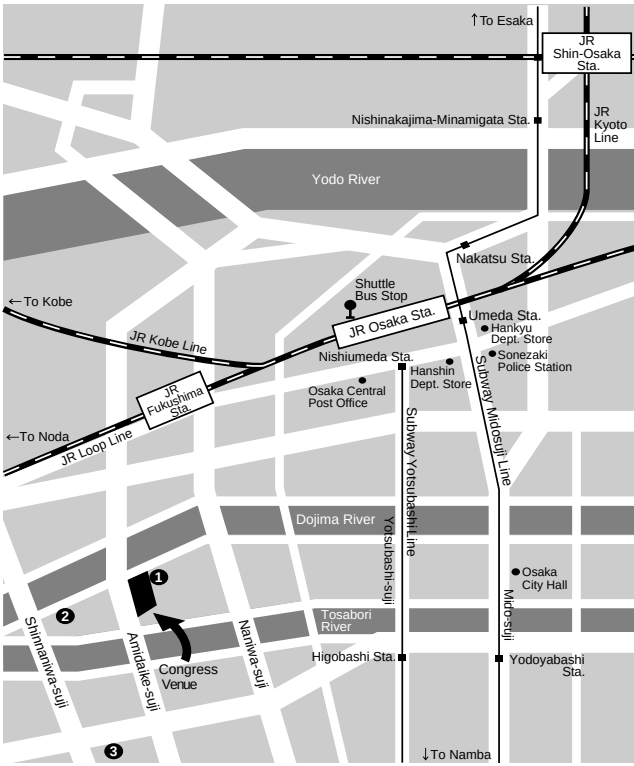
Access to Osaka

The most convenient and economical means to Osaka is to take a direct flight to Kansai International Airport.



Area Map of Osaka

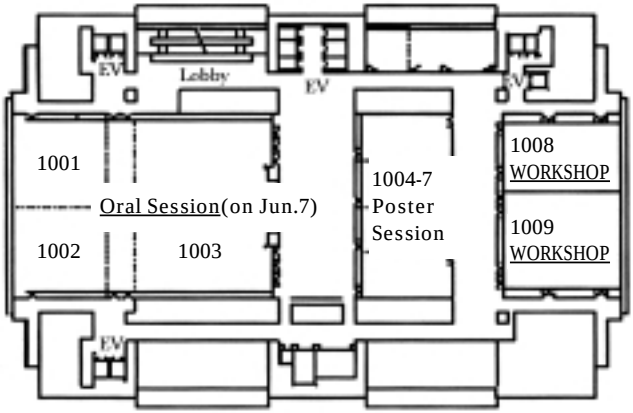




❶ Rihga Royal Hotel ❷ Hotel NCB ❸ Hotel Links Osaka & Spa

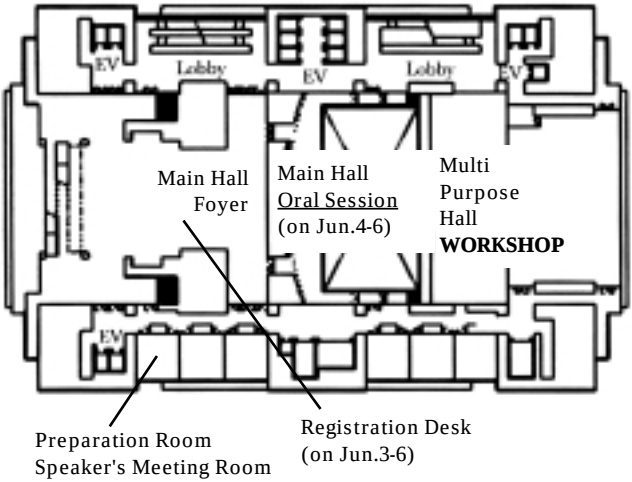
Osaka International Convention Center 10F

(Session 10-13)



Osaka International Convention Center 5F

(Plenary Session, Workshop & Session 1-9)



Rihga Royal Hotel / Banquet Room (2nd Floor)

TECHNICAL PROGRAM

Opening Remarks

Monday, June 4, 9:00-9:10, 5F Main Hall
Y. Sugawara, *Kansai Electric Power / General Chairman*

Plenary Session I

Monday, June 4, 9:10-11:10, 5F Main Hall
Chairperson: Y. Sugawara, *Kansai Electric Power*
T.R. Efland, *Texas Instruments*

1. Power Semiconductors in Transmission and Distribution Applications
R. Chokhawala and B. Danielsson*
*ABB Semiconductors and *ABB Power Systems, Switzerland*

2. Pulsed Power Application assisted by Power Semiconductor Devices
S. Ishii, K. Yasuoka and S. Ibuka
Tokyo Inst. of Technology, Japan

3. The Future of Electronics in Automobiles
J.G. Kassakian and D.J. Perreault
Massachusetts Inst. of Technology, USA

Session 1: SiC Devices I

Monday, June 4, 11:25-12:40, 5F Main Hall
Chairperson: P. Chow, *Renesseler Polytechnic Inst.*
H. Matsunami, *Kyoto Univ.*

1.1 5.5kV Normally-Off Low RonS 4H-SiC SEJFET
K. Asano, Y. Sugawara, S. Ryu*, R. Singh*, J. Palmour*, T. Hayashi and D. Takayama
*Kansai Electric Power, Japan and *Cree, U.S.A.*

1.2 12-19kV 4H-SiC pin Diode with Low Power Loss
Y. Sugawara, D. Takayama, K. Asano, R. Singh*, J. Palmour* and T. Hayashi
*Kansai Electric Power, Japan and *Cree, U.S.A.*

1.3 4.5kV 4H-SiC Diodes with Ideal Forward Characteristic
H. Lendenmann, A. Mukhidtinov, F. Dahlquist, H. Bleichner, P.A. Nilsson, R. Soderholm and P. Skytt
ABB Research, Sweden

Session 2: SiC Devices II

Monday, June 4, 14:00-15:15, 5F Main Hall
Chairperson: H. Lendenmann, *ABB Research*
K. Hara, *DENSO*

2.1 1.8 kV, 3.8A Bipolar Junction Transistors in 4H-SiC
S.-H. Ryu, A.K. Agarwal, J.W. Palmour and M.E. Levinshtein*
*Cree, U.S.A. and *Ioffe Institute of Russian Academy of Science, Russia*

2.2 Static and Dynamic Characteristics of 4-6 kV SIAFETs
D. Takayama, Y. Sugawara, T. Hayashi, R. Singh*, J. Palmour*, S. Ryu* and K. Asano
*Kansai Electric Power, Japan and *Cree, U.S.A.*

2.3 High Temperature Characteristics of 5 kV, 20 A 4H-SiC PiN Rectifiers
R. Singh, A. Hefner, Jr.*, D. Berning* and J. Palmour
*Cree and *NIST, U.S.A.*

Session 3: Packaging and Reliability I

Monday, June 4, 15:30-16:45, 5F Main Hall
Chairperson: R. Sittig, *Technical Univ., Braunschweig Inst. of Electrophysics*
M. Hoshi, *Nissan Motor*

3.1 Noble High Thermal Conductivity, Low Thermal Expansion Cu-Cu2O Composite Base Plate Technology for Power Module Application
R. Saito, Y. Kondo, Y. Koike, K. Okamoto, T. Suzumura* and T. Abe
*Hitachi and *Hitachi Cable, Japan*

3.2 Flip-Chip Flex-Circuit Packaging for Power Electronics
Y. Xiao, R. Natarajan, P. Jain, J. Barrett, E.J. Rymaszewski, R.J. Gutmann and T.P. Chow
Rensselaer Polytechnic Institute, U.S.A.

3.3 Innovative Press Pack Modules for High Power IGBTs
S. Kaufmann, T. Lang and R. Chokhawala
ABB Semiconductors, Switzerland

Session 4: Packaging and Reliability II

Monday, June 4, 17:00-18:15, 5F Main Hall
Chairperson: G. Charitat, *LAAS-CNRS*
R. Saito, *Hitachi*

4.1 Lead-Frame-On-Chip Offers Integrated Power Bus and Bond over Active Circuit
T.R. Efland, D. Abbott, V. Arellano*, M. Buschbom, M. Chang**, C. Hoffart, L. Hutter, Q. Mai, I. Nishimura***, S. Pendharker, M. Pierce, C.C. Shen, C.M. Thee**** and H. Vanhorn
*Texas Instruments, U.S.A., *Texas Instruments, Mexico, **Texas Instruments, Taiwan, ***Texas Instruments, Japan and ****Texas Instruments, Malaysia*

4.2 A Dimple-Array Interconnect Technique for Power Semiconductor Devices
S.S. Wen and G.-Q. Lu
Virginia Polytechnic Institute and State Univ., U.S.A.

4.3 Novel Monitoring Method and Long-Term Reliability Evaluation of Power Semiconductor Devices in Power Utility
T. Horiuchi and Y. Sugawara
Kansai Electric Power, Japan

Plenary Session II

Tuesday, June 5, 8:30-10:30, 5F Main Hall
Chairperson: H. Iwamoto, *Mitsubishi Electric*
D. Kinzer, *International Rectifier*

4. EMI Issues In Switching Power Converters
T. Ninomiya, M. Shoyama, C.-F. Jin, and G. Li
Kyushu Univ., Japan

5. Status and Future Trends of Propulsion Systems for Mass Transportation and their Correlation to Power Semiconductors
I. Herbst
ADtranz, Switzerland

6. Environment Friendly Revolution in Home Appliances
T. Tanaka
Toshiba, Japan

Session 5: RF Devices

Tuesday, June 5, 10:45-12:20, 5F Main Hall
Chairperson: C.A.T. Salama, *Univ. of Toronto*
T. Yachi, *NTT*

5.1 A High-efficiency 5-GHz-band SOI Power MOSFET Having a Self-aligned Drain Offset Structure
S. Matsumoto, Y. Hiraoka and T. Sakai
NTT, Japan

5.2 High Performance Stacked LDD RF LDMOSFET
J. Cai, C. Ren, N. Balasubramanian and J.K.O. Sin*
*Institute of Microelectronics, Singapore and *Hong Kong Univ. of Science and Technol., China*

5.3 High Power LDMOS for Cellular Base Station Applications
M. Shindo, M. Morikawa, T. Fujioka, K. Nagura, K. Kurotani, K. Odaira, T. Uchiyama* and I. Yoshida
*Hitachi and *Hitachi Tobu Semiconductor, Japan*

5.4 A High Efficiency High Power GaAs Push-Pull FET for W-CDMA Base Stations
K. Inoue, K. Ebihara, H. Haematsu, F. Yamaki, T. Igarashi, H. Takahashi and J. Fukaya
Fujitsu Quantum Devices, Japan

Workshop

Tuesday, June 5, 14:00-17:30, 5F Multi Purpose Hall & 10F Room 1008-9
Organizer: A. Nakagawa, *Toshiba*

Session 6: High Voltage Devices

Wednesday, June 6, 8:30-10:35, 5F Main Hall
Chairperson: P. Taylor, *Dynex Semiconductor*
M. Okamura, *JAIST*

6.1 A Study on Wide RBSOA of 4.5kV Power Pack IGBT
K. Yoshikawa, T. Koga, T. Fujii, A. Nishiura and Y. Takahashi*
*Fuji Electric R&D and *Fuji Electric, Japan*

6.2 6.5kV-Modules Using IGBTs with Field Stop Technology
J.G. Bauer, F. Auerbach, A. Porst, R. Roth*, H. Ruthing and O. Schilling**
*Infineon Technologies, *Infineon Technologies OHG and **Eupec, Germany*

6.3 Characterization of a Bi-Directional Double-Side, Double-Gate IGBT Fabricated by Wafer Bonding
K.D. Hobart, F.J. Kub, M. Ancona, J.M. Neilson*, K. Brandmier** and P.R. Waind***
*Naval Research Laboratory, *JMSN, **Silicon Power, U.S.A. and ***Dynex Semiconductor, U.K.*

6.4 Ultra-High Voltage Device Termination Using the 3D RESURF (Super-Junction) Concept - Experimental Demonstration at 6.5 kV
F. Udrea, T. Trajkovic, J. Thomson*, L. Coulbeck*, P.R. Waind*, G.A.J. Amaratunga and P. Taylor*
*Univ. of Cambridge and *Dynex Semiconductor, U.K.*

6.5 6kV 5kA RCGCT with Advanced Gate Drive Unit
H. Gruening, T. Tsuchiya, K. Satoh, Y, Yamaguchi*, F. Mizohata and K. Takao
*Mitsubishi Electric and *Fukuryo Semicon Engineering, Japan*

Session 7: MOSFETs I

Wednesday, June 6, 10:50-12:05, 5F Main Hall
Chairperson: A. Shibib, *Lucent Technologies*
H. Tadano, *Toyota Central Research & Development Labs.*

7.1 A Novel Process Technique for Fabricating High Reliable Trench DMOSFETs Using Self-Align Technique and Hydrogen Annealing
J. Kim, T.M. Roth, S.-G. Kim, D. W. Lee, J.G. Koo and K.-I. Cho
ETRI, Korea

7.2 A High Density, Low On-resistance, Trench Lateral Power MOSFET with a Trench Bottom Source Contact
N. Fujishima, A. Sugi*, T.Suzuki*, S. Kajiwara*, Y. Nagayasu* and C.A.T. Salama
*Univ. of Toronto, Canada and *Fuji Electric R&D, Japan*

7.3 An Ultra Dense Trench-Gated Power MOSFET Technology Using the Self-Aligned Process
J. Zeng, G. Dolny, C. Kocon, R. Stokes, T. Grebs, J. Hao, R. Ridley, J. Benjamin, L. Skurkey, S. Benczkowski, D. Semple, P. Wodarczyk and C. Rexer
Intersil, U.S.A.

Session 8: LD MOSFETs

Wednesday, June 6, 13:40-15:45, 5F Main Hall
Chairperson: M. Briere, *Cherry Semiconductor*
H. Kitaguchi, *Oki Electric Industry Co.,*

8.1 Avalanche-Induced Thermal Instability in LDMOS Transistors
P.L. Hower, C.-Y. Tsai, S. Pendharkar, E. Efland, R. Steinhoff and J. Brodsky
Texsas Instruments, U.S.A.

8.2 Robustness of LDMOS Power Transistors in SOI-BCD Processes and Derivation of Design Rules Using Thermal Simulation
B.H. Krabbenborg and J.A. van der Pol
Philips Semiconductors, The Netherlands

8.3 Using Two-Dimensional Filament Modeling to Predict LDMOS and SCRLDMOS Behavior under High Current ESD Conditions
S. Pendharkar and P. Hower
Texas Instruments, U.S.A.

8.4 Improvement of Breakdown Characteristics of LDMOSFETs with Uneven Racetrack Sources for PDP Driver Applications
T.M. Roh, D.W. Lee, J. Kim, J.G. Koo and K.-I. Cho
ETRI, Korea

8.5 0.6μm BiCMOS Based 15 and 25V LDMOS for Analog Applications
Y. Kawaguchi, K. Nakamura, k. Karouji, K. Watanabe, Y. Yamaguchi and A. Nakagawa
Toshiba, Japan

Session 9: Poster Session

Wednesday, June 6, 15:55-17:55, 10F Room 1004-7
Chairperson: K.T. Kornegay, *Conell Univ.*
T. Ise, *Osaka Univ.*

9.1 Dependence of Turn-On and Turn-Off Characteristics on Anode/Gate Geometry of High-Voltage 4H-SiC GTO Thyristors
J.B. Fedison, T.P. Chow, M. Ghezzo* and J.W. Kretchmer*
*Rensselaer Polytechnic Institute and *GE Corporate R&D*

9.2 Design Consideration for 2kV SiC-SIT
H. Onose, T. Yatsuo, A. Watanabe, T. Yokota, T. Ishikawa, I. Sanpei, T. Someya and Y. Kobayashi
Hitachi, Japan

9.3 Large Area 4H-SiC Power MOSFETs
A. Agarwal, S.-H. Ryu, M. Das, L. Lipkin, J. Palmour and N. Saks*
*Cree and *Naval Research Laboratory, U.S.A.*

9.4 Influence of Device and Circuit Parameters on the Switching Losses of an Ultra Fast CoolMOS/SiC-Diode Device-Set: Simulation and Measurement
J. Petzoldt, T. Reinmann and L. Lorenz*
*Ilmenau Technical Univ. and *Infineon Technologies, Germany*

9.5 Comparison and Optimization of Edge Termination Techniques for SiC Power Devices
D.C. Sheridan, G. Niu, J.N. Merrett and J.D. Cressler
Auburn Univ., U.S.A.

9.6 High Frequency Application of High Transconductance Surface-Channel Diamond Field-Effect Transistors
H. Umezawa, H. Taniuchi, T. Arima, Y. Ohba, M. Tachiki and H. Kawarada
Waseda Univ., Japan

9.7 Thyristor with Integrated Forward Recovery Protection Function
F.-J. Niedernostheide, H.-J. Schulze and U. Kellner-Werdehausen*
*Infineon and *Eupec, Germany*

9.8 Short on-Pulse Reverse Recovery Behavior of Free Wheeling Diode (FWD)
F. Nagaune, T. Miyasaka, S. Tagami* H. Shigekane and H. Kirihata*
*Fuji Hitachi Power Semiconductor and *Fuji Electric, Japan*

9.9 A New BRT (Base Resistance Controlled Thyristor) Employing Trench Gate and Self-Align Corrugated P-Base
J.-K. Oh, M.-S. Lim, B.-C. Jeon, M.-K. Han and Y.-I. Choi*
*Seoul National Univ. and *Ajou Univ., Korea*

9.10 A 6kV Thyristor Fabricated by Direct Wafer Bonding
K.D. Hobart, F.J. Kub, D. Pattanayak*, D. Piccone*, M. Patel*, D. Hits*, R. Rodrigues*, G. Ayele** and C.A. Colinge**
*Naval Research Laboratory, *Silicon Power and **California State Univ., U.S.A.*

9.11 A Novel 6.5 kV IGCT for High Power Current Source Inverters
A. Weber, P. Kern and T. Dalibor
ABB Semiconductors, Switzerland

9.12 Impacts of Channel Implantation on Performance of Static Shielding Diodes and Static Induction Rectifiers
K. Yano, N. Hattori, Y. Yamamoto and M. Kasuga
Yamanashi Univ., Japan

9.13 Modeling of Ion-Induced Charge Generation in High Voltage Power Devices
W. Kaindl, G. Solkner*, P. Voss** and G. Wachutka
*Munich Univ. of Technology, *Infineon Technologies and **EUPEC, Germany*

9.14 Fine Pattern Effect Leakage Current and Reverse Recovery Characteristics of MPS Diode
T. Naito, M. Nemoto, A. Nishiura, M. Otsuki*, M. Kirisawa* and Y. Seki*
*Fuji Electric R&D and *Fuji Electric, Japan*

9.15 Power Diodes with Active Control of Emitter Efficiency
D. Druecke and D. Silber
Univ. of Bremen, Germany

9.16 A Fast & Soft Recovery Diode with Ultra Small Qrr (USQ-Diode) Using Local Lifetime Control by He Ion Irradiation
K. Nishiwaki, T. Kushida and A. Kawahashi
Toyota Motor, Japan

9.17 Low-Voltage SiGe Power Diodes
G.A.M. Hurkx, E.A. Hijzen, M.A.A. in 't Zandt
Philips Research Laboratories, The Netherlands

9.18 100V Trench MOS Barrier Schottky Rectifier Using Thick Oxide Layer (TO-TMBS)
T. Shimizu, S. Kunori, M. Kitada and A. Sugai
Shindengen Electric Mfg., Japan

9.19 Lateral SOI Static Induction Rectifier
K. Yano, S. Honarkhah* and C.A.T. Salama*
*Yamanashi Univ., Japan and *Univ. of Toronto, Canada*

9.20 Flip Chip Power MOSFET: A New Wafer Scale Packaging Technique
A. Arzumanyan, R. Sodhi, D. Kinzer. H. Schofield and T. Sammon
International Rectifier, U.S.A.

9.21 A 700V Lateral Power MOSFET with Narrow Gap Double Metal Field Plates Realizing Low On-Resistance and Long-Term Stability of Performance
N. Fujishima, M. Saito*, A. Kitamura*, Y. Urano*. G. Tada* and Y. Tsuruta*
*Fuji Electric R&D and *Fuji Electric, Japan*

9.22 60V Field NMOS and PMOS Transistors for the Multi-Voltage System Integration
T. Terashima, F. Yamamoto, K. Hatasako and S. Hine
Mitsubishi Electric, Japan

9.23 High Voltage Device Implementation in 0.5µm LBC6 (BiCMOS-Power) Technology
S. Pendharkar, T. Debolske, T. Efland, W. Leitz, W. Nehrer, J. Smith and R.V. Taylor
Texas Instruments, U.S.A.

9.24 Low On-Resistance SOI Power MOSFET Using Dynamic Threshold (DT) Concept for High Efficient DC-DC Converter
Y. Hiraoka, S. Matsumoto and T. Sakai
NTT, Japan

9.25 Smart PWM Driver in SO-8 for Automotive Solenoid Controls
K. Yoshida, S. Kiuchi, H. Tobisaka, N. Yaezawa, T. Ohe, S. Furuhata and T. Fujihira
Fuji Hitachi Power Semiconductor, Japan

9.26 Mechanism of Power Dissipation Capability of Power MOSFET Devices: Comparative Study between LDMOS and DMOS Transistors

Y.S. Chung, O. Valenzuela and B. Baird

Motorola, U.S.A.

9.27 A Half-Bridge Driver IC with Newly Designed High Voltage Diode

K. Watabe, K. Shimizu, H. Akiyama, T. Araki, J. Moritani and M. Fukunaga

Mitsubishi Electric, Japan

9.28 Recessed Trench MOSFET Process without Critical Alignments Makes Very High Densities Possible

A. Finney, J. Evans*, P. Blair, J. Earnshaw, P. Jerred, K. Lowe, D. Mottram and A. Wood

*Zetex and *Totem Semiconductors, U.K.*

9.29 Optimization of Safe-Operating-Area Using Two Peaks of Body-Current in Submicron LDMOS Transistors

S.K. Lee, J.H. Kim, Y.C. Choi, C.J. Kim, H.S. Kang and C.S. Song

Fairchild Semiconductor, Korea

9.30 Charge Model for SOI LDMOST with Lateral Doping Gradient

N. D'Halleweyn, L. Tiemeijer*, J. Benson and W. Redman-White

*Univ. of Southampton, U.K. and *Philips Research Laboratories, The Netherlands*

9.31 A Dual-Voltage Self-Clamped IGBT for Automotive Ignition Application

Z.J. Shen and S.P. Robb*

*Univ. of Michigan-Dearborn and *ON Semiconductor, U.S.A.*

9.32 Wide Cell Pitch 1200V NPT CSTBTs with Short Circuit Ruggedness

H. Nakamura, K. Nakamura, S. Kusunoki, H. Takahashi, Y. Tomomatsu, M. Harada and S. Hine

Mitsubishi Electric, Japan

9.33 An Ignition IGBT with Smart Functions in Chip on Chip Technology

L. Leipold, H. Fischer, W. Kanert, J. Kositza, T. Theobald and C. Xu

Infineon Technologies, Germany

9.34 Great Improvement in IGBT Turn-On Characteristics with Trench Oxide PiN Schottky (TOPS) Diode

M. Nemoto, M. Otsuki*, M. Kirisawa*, Y. Seki*, T. Naito, R.N. Gupta**, C.R. Winterhalter** and H.-R. Chang**

*Fuji Electric R&D, *Fuji Electric, Japan and **Rockwell Science Center, U.S.A.*

9.35 The Influence of Body Effect on the Short Circuit Ruggedness of Emitter Ballasted IGBTs

P.M. Shenoy, G.M. Dolny and A. Bhalla

Intersil, U.S.A.

9.36 High-Functionality Compact Intelligent Power Unit (IPU) for EV/HEV Applications

G. Majumdar, K.H. Hussein*, K. Takanashi, M. Fukada, J. Yamashita, H. Maekawa, M. Fuku, T. Yamane and T. Kikunaga

*Mitsubishi Electric and *Fukuryo Semicon Engineering, Japan*

9.37 Soft-Switching Turn-off Characterization at High Temperature of 1200V Trench IGBT Using Local Lifetime Control

S. Azzopardi, A. Kawamura and H. Iwamoto*

*Yokohama National Univ. and *Mitsubishi Electric, Japan*

9.38 A Novel, 1.2kV Trench Clustered IGBT with Ultra High Performance

O. Spulber, M. Sweet, K. Vershnin, N. Luther-King, M.M. de Souza and E.M.S. Narayanan

De Montfort Univ., U.K.

9.39 Destruction Mechanism of PT and NPT-IGBTs in the Short Circuit Operation Which Can Explain Various Kinds of Simulated Results

I. Takata

Mitsubishi Electric, Japan

9.40 A Study of GTBT Characteristics Driven by Pulse Current

K. Throngnumchai, Y. Shimoida, T. Karaki and H. Kaneko

Nissan Motor, Japan

9.41 Failure Mechanisms of SOI High-Voltage LIGBTs and LDMOSFETs under Unclamped Inductive Switching

D.M. Garner, F. Udrea, G. Ensell*, K. Sheng, A.E. Popescu, G.A.J. Amaratunga and W.I. Milne

*Univ. of Cambridge and *Univ. of Southampton, U.K.*

9.42 Design Consideration of 1000V Merged Pin Schottky Diode Using Superjunction Sustaining Layer

E. Napoli, A.G.M. Strollo

Univ. of Naples "Federico II", Italy

9.43 New Benchmark for RESURF, SOI, and Super-Junction Power Devices

R.P. Zingg

Philips Semiconductors, The Netherlands

9.44 A 650V Rated RESURF-Type LDMOS Employing an Internal Clamping Diode for Induced Bulk Breakdown without EPI or Buried Layer

M.H. Kim, J.J. Kim and Y.S. Choi

Fairchild Semiconductor, Korea

9.45 Multiring Active Analogic Protection for Minority Carrier Injection Suppression in Smart Power Technology

O. Gonnard, G. Charitat, M. Bafleur, P. Lance*, M. Suquet**, J.P. Laine and A. Peyre-Lavigne

*LAAS/CNRS, *Motorola and **Siemens Automotive, France*

9.46 800V/1A, 1-Chip Process for Battery Charger IC
C.K. Jeon, J.J. Kim, Y.S. Choi, M.H. Kim, S.L. Kim, H.S. Kang and C.S. Song
Fairchild Semiconductor, Korea

9.47 Investigation of the Gate Dielectric Oxidation Treatment in Trench Gate Power Devices
M.-J. Lin, C.-W. Liaw, J.-J. Chang, F.-L. Zhang, T.-K. Yen and H.-C. Cheng
National Chiao Tung Univ., Taiwan

9.48 Fabrication of High Aspect Ratio Doping Region by Using Trench Filling Epitaxial Si Growth
S. Yamauchi, Y. Urakami, N. Tsuji and H. Yamaguchi
Denso, Japan

9.49 The Monolithic Bidirectional Switch (MBS) in a Matrix Converter Application
F. Heinke and R. Sittig
Technische Univ. Braunschweig, Germany

9.50 Soft-Switching Type Multiple-Chip Power Device (M-Power)
H. Ota, Y. Minoya, N. Terasawa, K. Kuwabara, S. Igarashi*, Y. Nishikawa* and T. Nozawa
*Fuji Hitachi Power Semiconductor and *Fuji Electric R&D*

9.51 A Novel Gate Drive Circuit for Low-loss System Using IGBT Saturation Voltage Characteristics
S. Takizawa, S. Igarashi and K. Kuroki
Fuji Electric R&D, Japan

9.52 Physics-Based Dynamic Electro-Thermal Models of Power Bipolar Devices (Pin Diode and IGBT)
P.M. Igic, P.A. Mawby and M.S. Towers
Univ. of Wales Swansea, U.K.

9.53 Using Two-Dimensional Structures to Model Filamentation in Semiconductor Devices
P.L. Hower and S. Pendharkar
Texsas Instruments, U.S.A.

Session 10: Super Junction

Thursday, June 7, 8:30-10:35, 10F Room 1001-3
Chairperson: G. Amaratunga, *Cambridge Univ.*
R.K. Malhan, *DENSO*

10.1 Breaking the Silicon Limit Using Semi-Insulating Resurf Layers
R. van Dalen, C. Rochefort and G.A.M. Hurkx
Philips Res. Labs., The Netherlands

10.2 Lateral Unbalanced Super Junction (USJ) for High Breakdown Voltages in SOI Technology
R. Ng, F. Udrea, K. Sheng, K. Ueno*, G.A.J. Amaratunga and M. Nishiura*
*Univ. of Cambridge, U.K. and *Fuji Electric R&D, Japan*

10.3 A New 800V Lateral MOSFET with Dual Conduction Paths
D.R. Disney, A.K. Paul, M. Darwish, R. Basecki and V. Rumennik
Power Integrations, U.S.A.

10.4 Implementation of High-Side, High Voltage RESURF LDMOS in a Sub-Half Micro Smart Power Technology
R. Zhu, V. Parthasarathy, V. Khemka, A. Bose and T. Roggenbauer
Motorola, U.S.A.

10.5 Lateral Smart-Discrete Process and Devices Based on Thin-Layer Silicon-on-Insulator
T. Letavic, J. Petruzzello, M. Simpson, J. Curcio, S. Mukherjee, J. Davidson*, S. Peake*, C. Rogers*, P. Rutter*, M. Warwick* and R. Grover*
*Philips Research USA, U.S.A. and *Philips Semiconductors, U.K.*

Session 11: IGBTs I

Thursday, June 7, 10:50-12:05, 10F Room 1001-3
Chairperson: M.-K. Han, *Seoul National Univ.*
Y. Seki, *Fuji Electric*

11.1 600V-IGBT with Reverse Blocking Capability
M. Takei, Y. Harada and K. Ueno
Fuji Electric R&D, Japan

11.2 Novel 600V Trench High-Conductivity IGBT (Trench HiGT) with Short Circuit Capability
K. Oyama, Y. Kohno, J. Sakano, K. Ishizaka, D. Kawase and M. Mori
Hitachi, Japan

11.3 The 5th Generation Highly Rugged Planar IGBT Using Sub-Micron Process Technology
J. Yamashita, C. Yoshida, C. Fujii, K. Takanashi and J. Moritani
Mitsubishi Electric, Japan

Session 12: MOSFETs II

Thursday, June 7, 13:40-14:55, 10F Room 1001-3
Chairperson: P. Hower, *Texas Instruments*
S. Shinohara, *Origin Electric*

12.1 Shallow Angle Implantation for Extended Trench Gate Power MOSFETs with Super Junction Structure
Y. Hattori, T. Suzuki, E. Hayashi, M. Kodama and T. Uesugi
Toyota Central R&D Labs., Japan

12.2 Characterization of Gate Oxide Degradation Mechanisms in Trench-Gated Power MOSFETS Using the Charge Pumping Technique

G. Dolny, N. Gollagunta*, S. Suliman*, L. Trabzon*, M. Horn*, O.O. Awadelkarim*, J. Ruzyllo*, S.J. Fonash*, J. Hao, R. Ridley, T. Grebs, J. Zeng and C. Kocon

*Intersil and *Pennsylvania State Univ., U.S.A.*

12.3 Rewrite the Silicon Limit to Compete with Superjunction MOSFETs

T. Kobayashi, H. Abe, Y. Niimura, T. Yamada, A. Kurosaki, T. Hosem and T. Fujihira

Fuji Hitachi Power Semiconductor, Japan

Session 13: IGBTs II

Thursday, June 7, 15:10-16:20, 10F Room 1001-3

Chairperson: L. Lorenz, *Infineon Technologies*

T. Ogura, *Toshiba*

13.1 Advanced 60µm Thin 600V Punch-Through IGBT Concept for Extremely Low Forward Voltage and Low Turn-Off Loss

T. Matsudai, H. Nozaki, S. Umekawa, M. Tanaka, M. Kobayashi, H. Hattori and A. Nakagawa

Toshiba, Japan

13.2 600V CSTBT Having Ultra Low On-State Voltage

H. Takahashi, S. Aono, E. Yoshida*, J. Moritani and S. Hine

*Mitsubishi Electric and *Ryoden Semiconductor System Engineering, Japan*

13.3 A 600V 200A Low Loss High Current Density Trench IGBT for Hybrid Vehicle

K. Hamada, T. Kushida, A. Kawahashi and M. Ishiko*

*Toyota Motor and *Toyota Central R&D Labs., Japan*

Award & Closing

Thursday, June 7, 16:25-16:45, 10F Room 1001-3

Chairperson: Y. Sugawara, *Kansai Electric Power*

H. Iwamoto, *Mitsubishi Electric*