ISPSD'2000

The 12th International Symposium on Power Semiconductor Devices & ICs

Advance Program

May 22-25, 2000
Centre de Congrès Pierre Baudis
Toulouse, France

Sponsor: IEEE Electron Devices Society
Co-Sponsor: The Institute of Electrical Engineers of Japan
http://www.laas.fr/ISPSD2000

	Monday May 22		Tuesday May 23		Wednesday May 24		Thursday May 25	
8:00								
			8:30	**HVIGBT**	8:30	**SiC**	8:30	**Advanced BCD**
9:00	9:00							
10:00		Registration at «Palais des Congrès»	10:10	*Break 15 mn*	10:10	*Break 15 mn*	10:10	*Break 15 mn*
			10:25	**LDMOS**	10:25	**Diodes**	10:25	**Energy Capability**
11:00								
12:00			12:05	LUNCH	12:05	LUNCH	12:05	LUNCH
13:00			13:30	**Superjunction**	13:30	Poster prep.	13:30	**IGBT**
14:00	14:00	Welcome			14:00	**POSTER SESSION**		
	14:15	Pr. H. Matsunami Dr. T. Kimoto Kyoto University					15:10	*Break 15 mn*
15:00		A. Ludikhuize Philips Research Laboratories	15:35	*Break 15 mn*			15:25	**Trench**
	15:45	*Break 15 mn*	15:50	**Process Integration**	15:45	*Break 15 mn*		
16:00	16:00	R.K. Williams Advanced Analogic Technologies, Inc			16:00	Workshop «Tcad tools for Power Devices & Circuits» Pr. W. Fichtner		
	16:45						17:05	Concluding remarks
17:00	17:30	**Reception Mairie Cocktail**	17:05				17:15	
18:00					18:00			
19:00								
20:00				**Conference Banquet**				

TABLE OF CONTENTS

NOTES

Page

CHAIRMAN'S MESSAGE

On behalf of the ISPSD Conference Committee, I would like to invite you to the 12th International Symposium on Power Semiconductor Devices and IC's (ISPSD'2000).

ISPSD provides a yearly international forum for technical discussion in all areas of Power Semiconductor Devices, Power ICs and their Applications. This conference has grown to become today the most important international conference in this field.

Fundamentally international, it has the very peculiarity to be held each year, not simply in a different place, but in a different "continent" with a rotation accross the world from Japan, to North America and to Europe. Following last year very successful meeting in Toronto, Canada, the Symposium returns for the third time to Europe. After Davos, Switzerland, in 1994 and Weimar, Germany in 1997, Toulouse, France, will host the Symposium for the very famous year 2000.

The plenary invited talks on Monday afternoon mirror the geographical rotation of the conference and feature the following presentations:

From Japan: "Progress in Wide-bandgap Semiconductor SiC for Power Devices", by Hiroyuki Matsunami and Tsunenobu Kimoto from Kyoto University,

From Europe: "A Review of RESURF Technology", by Adriaan W. Ludikhuize, Philips Research, Eindhoven, The Netherlands.

From North America: "Beyond Y2K: Technology Convergence as a Driver of Future Low-Voltage Power Management Semiconductors", by Richard K. Williams, Advanced Analogic Technologies, Inc., Sunnyvale CA,

Interestingly, these invited talks also fairly represent the domains covered by ISPSD, ie materials, devices and applications.

The number of submitted abstracts reached a total number of 159. From this number, 65 where from "pure" academic research groups, 68 from "pure" industrial research teams and 26 where co-signed by universities and industries, as a result of their strong collaboration in the power device domain. The global character of ISPSD is reflected by submissions originating from 25 countries; 40.8% from Europe, 24.5% from America, 15.9% from Japan, 11.4% from Asia and 7.4% from the rest of the world.

41 papers were accepted for oral presentation with another 46 accepted as poster session papers.

Student papers, oral or poster presentation, are eligible for a "Best Student Paper Award" which will be announced at the end of the conference.

A special event is planned on Wednesday 24th: a plenary workshop on "TCAD Tools for Power Devices and IC's" will be organised by Pr. Wolfgang Fichtner. You are all invited to share your thoughts, worries and experience, about the adequacy of modern TCAD microelectronics frameworks for simulating power structures.

It is with great pleasure that I thank the ISPSD'2000 Organising and Technical Program Committees and specially the Technical Program Committee Chair, Albert Senes, for their outstanding efforts in planning the Symposium.

We are all looking forward to welcoming you in Toulouse.

Dr. Georges Charitat
General Chairman

Organizing Committee

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Sponsorship

ISPSD'2000 is technically sponsored by the Electron Device Society (EDS) of the Institute of Electrical and Electronic Engineers (IEEE). It is co-sponsored by the Institute of Electrical Engineers of Japan (IEEJ) and by the European Conference on Power Electronics (EPE). It has also received support from the European Community, the CNRS (French National Scientific Research Centre), the Midi-Pyrénées Council, the Toulouse Paul Sabatier University, Motorola Semiconductor, On Semiconductor, Schneider Electric and ST Microelectronics.

CONFERENCE INFORMATION
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Symposium Date & Site

Dates: May 22-25, 2000

Location: Centre de Congrès Pierre Baudis
11, Esplanade Compans Caffarelli
31000 Toulouse
France
Saint-Exupery Auditorium
http://www.centre-congres-toulouse.fr

Registration

Conference Registration
All persons attending the conference are required to register. Please register by returning the enclosed registration Form. Registration can also be made by Fax or e-mail (see the conference Web Server: http://www.laas.fr/ISPSD2000/ressourc, where you can download the registration form). The registration will be effective only after the payment has arrived. Registration Forms are to be sent to:

Mme Sylvie Barrouquère
ADERMIP
3, Avenue Didier Daurat – 31400 Toulouse, France
Phone: +(33) 5 62 47 49 89 – Fax: +(33) 5 61 80 81 75
e-mail: barrouqu@cict.fr

Registration Fees

IEEE/IEEJ Member		Non Member		Student*	
Before April 1st	After April 1st	Before April 1st	After April 1st	Before April 1st	After April 1st
2500 FF	3000 FF	3000 FF	3500 FF	1300 FF	1500 FF
381 €	457 €	457 €	533 €	198 €	228 €

Registration fees cover admission to the conference, conferrence proceedings and CDROM, coffee breaks, lunches, welcome reception and banquet.

Additional Banquet ticket: 600 FF/91 €

Payment
Payment is accepted in French Francs or in Euro:
By credit card (CB, Visa, Eurocard or Mastercard),
By Bank Draft or check payable to ADERMIP, bank account 12719500200 at Banque Courtois, Toulouse Rémusat, branch reference agence 10268, bank identification 02504 key 49
For French organization only, by purchase order payable to ADERMIP.
Please mention "ISPSD'2000", your name and address on the Bank Draft or purchase order.

Cancellation
Refunds of 50% will be made if a written request is received before May 12, 2000.
No refunds can be made for cancellations received after this date.

Registration Desk
The ISPSD'2000 conference will be held in the Saint-Exupery Auditorium located on the 2nd level of the Pierre Baudis Congress Centre. The registration desk will be open on the ground level of the Congress Centre the first day of the conference, Monday 22nd, from 9 a.m. to 4:45 p.m.
From Tuesday 23rd, the registration desk will be transfered to room Argos, on the 1st level and will be open from 8 a.m. to 5 p.m.
Information, additional proceedings and extra event tickets will be available at this desk.

Other Informations

Secretariat Service during the conference
Telephone and fax messages may be directed through the Secretariat at the following number:
Tel: +(33) 5 62 30 40 66 - Fax: +(33) 5 62 30 47 44

Presentation
All oral presentations will use overhead projection viewgraphs.

Official Language
The official language of the ISPSD is English. There will be no facilities for simultaneous translation.

Meeting Facilities
All the papers will be presented in the Saint-Exupery Auditorium on the 2nd level of the Pierre Baudis Congress Centre.

Liability
Participants are reminded to obtain adequate international health and personal property insurance. The organizers cannot be held responsible for medical costs or for loss or damage to personal property.

Technical Tours
On Friday 26th of May, the day immediately after ISPSD'2000 completion, some technical tours could be organised, depending on the number of interested people, to the following places:
- Airbus Industries, (http://www.airbus.com)
- Toulouse Space City, (http://www.cite-espace.com/)
- Motorola Semiconductor.

More information will be given on the Web site at http://www.laas.fr/ISPSD2000/techvisit.
So please check this address if you plan to participate in these tours.

Workshop
On Wednesday 24th, at 4 p.m. a workshop will be organised in the main conference room. Entitled «TCAD Tools for Power Devices and Circuits», it will be lead by Pr. Wolfgang Fichtner. You will have the opportunity to share your experience with industry and university representatives and try to define what are the main inadequacies and most wanted advancements in this domain. Some documents will be ready before the workshop itself in order to let you prepare it correctly, just look at http://www.laas.fr/ISPSD2000/workshop.

Social Events
Morning and afternoon breaks are scheduled. A non-stop coffee and juice bar is planned during poster session. Lunches, from 12:05 to 1:30 p.m., are included in the registration fees and will be served inside the Congress Centre. This will help to keep the program on time and will also favour exchanges of ideas and information among participants.

A welcome reception, sponsored by the mayor of Toulouse, is scheduled on Monday 22nd, in a very famous place of Toulouse, the "Salle des Illustres" at city hall.
The banquet, along with a typical french show, will happen on Tuesday 23rd. Details will be disclosed later.

Web Site

For further information on the conference, please visit the web site at: http://www.laas.fr/ISPSD2000. From this site, you can download all documents necessary to register and prepare your venue.

HOTEL/TRAVEL/TRANSPORTATION

Hotel Reservations
Toulouse has over one hundred hotels covering a wide range of comfort and price. A sufficient number of rooms have been reserved in Downtown hotels. List is given below and will be updated at http://www.laas.fr/ISPSD2000/accomod.
DEADLINE for the hotel registration is March 15th. We cannot guarantee reservations beyond this date.
IMPORTANT: Many events take place from May 22nd to May 27th here in Toulouse, so please make your hotel reservation as soon as possible.
For your reservation, please contact DIRECTLY the hotel of your choice mentioning ISPSD.

Hotel list:
***** (price around 500 FF)**
Hôtel Athénée, 13 bis rue Matabiau, 31000 Toulouse
Tel: +33 5 61 63 10 63 - Fax: +33 5 61 63 87 80
Hôtel Capoul, 13 Place Wilson, 31000 Toulouse
Tel: +33 5 61 10 70 70 - Fax: +33 5 61 21 96 70
Hôtel Jean-Jaurès, 29 Allées Jean-Jaurès, 31000 Toulouse
Tel: +33 5 61 62 63 33 - Fax: +33 5 61 63 15 17
Hôtel Mermoz, 50 Rue Matabiau, 31000 Toulouse
Tel: +33 5 61 63 04 04 - Fax: +33 5 61 63 15 64
Hôtel de Paris, 18, Allées Jean-Jaurès, 31000 Toulouse
Tel: +33 5 61 62 98 30 - Fax: +33 5 62 73 34 09
Hôtel Phoenica, 7 Boulevard Bonrepos, 31000 Toulouse
Tel: +33 5 61 63 81 63 - Fax: +33 5 61 63 02 06

**** (price around 300 FF)**
Hôtel Albert 1er, 8 Rue Rivals, 31000 Toulouse
Tel: +33 5 61 21 17 91 - Fax: +33 5 61 21 09 64
Hôtel Albion, 28 Rue Bachelier, 31000 Toulouse
Tel: +33 5 61 63 60 36 - Fax: +33 5 61 62 66 95
Hôtel de France, 5 Rue d'Austerlitz, 31000 Toulouse
Tel: +33 5 61 21 88 24 - Fax: +33 5 61 21 99 77
Hôtel du Taur, 2 Rue du Taur, 31000 Toulouse
Tel: +33 5 61 21 17 54 - Fax: +33 5 61 13 78 41
Hôtel Grand Balcon, 8 Rue Romiguières (Place du Capitole), 31000 Toulouse
Tel: +33 5 61 21 48 08 - Fax: +33 5 61 21 59 98
Hôtel Le Capitole, 10, Rue Rivals, 31000 Toulouse
Tel: +33 5 61 23 21 28 - Fax: +33 5 61 23 67 48
Hôtel Ibis, 2 Rue Claire Pauilhac (Place Jeanne d'Arc), 31000 Toulouse
Tel: +33 5 61 63 61 63 - Fax: +33 5 61 63 07 46
Hôtel Le Président, 43, Rue Raymond IV, 31000 Toulouse
Tel: +33 5 61 63 46 46 - Fax: +33 5 61 62 83 60
Hôtel Le Trianon, 7 Rue Lafaille, 31000 Toulouse
Tel: +33 5 61 62 74 74 - Fax: +33 5 61 99 15 44
Hôtel Orsay, 8 Boulevard Bonrepos, 31000 Toulouse
Tel: +33 5 61 62 71 61 - Fax: +33 5 61 62 64 46
Hôtel Arnaud Bernard, 33 Place Tiercerettes, 31000 Toulouse
Tel: +33 5 61 21 37 64 - Fax: +33 5 61 29 86 91
Hôtel Victor Hugo, 26 Boulevard de Strasbourg, 31000 Toulouse
Tel: +33 5 61 63 40 41 - Fax: +33 5 61 62 66 31
Hôtel La Chartreuse, 4bis Boulevard Bonrepos, 31000 Toulouse
Tel: +33 5 61 62 93 39 - Fax: +33 5 61 62 58 17

About Toulouse
Toulouse is a city of 600 000 inhabitants located in the South of France, and is the capital of the Midi-Pyrénées region. It is located on the banks of the Garonne River, close to the Pyrénées Mountains and halfway between the Atlantic Ocean and the Mediterranean Sea.
The city is southern in feel and climate – winters are mild and summers hot.
Toulouse is well known for several remarkable monuments like Basilique St-Sernin, the largest conserved Romanesque church in Europe. Toulouse is also the European Capital of Aeronautics and Space and a leading centre in Industry, Technology and Research.

Access to Toulouse
Toulouse is about 1 hour from Paris by air, 5 hours by rail (TGV via Bordeaux) and 7 hours by freeway. There are about 40 flights daily between Toulouse and Paris. There are also daily flights between Toulouse and Amsterdam, Brussels, Dusseldorf, Frankfort, Geneva, Lisbon, London, Madrid, Milan, Munich, Porto.
A shuttle, which departs every 20 minutes, is available between the airport and the City centre (http://www.navettevia-toulouse.com/english/index.html). Fare: about 28 FF. The first stop of the shuttle from the airport is the Pierre Baudis Congress Centre.
Taxi fare is around 130 FF to City centre.

9:00 a.m. Registration at Palais des Congrès
2:00 p.m. Welcome
2:15 p.m. Invited papers

Plenary Session: Invited Papers

Chairmen: A. Senes - H. Iwamoto

2:15 p.m.
Progress in Wide-bandgap Semiconductor SiC for Power Devices, Hiroyuki Matsunami and Tsunenobu Kimoto, Kyoto University
The potential of wide-bandgap semiconductor silicon carbide (SiC) for low-loss power devices has been recognized for a long time. Breakthroughs in large-diameter bulk crystal growth and high-quality epitaxial growth have triggered the feasibility of SiC power devices. Many of prototype power devices, such as Schottky and pin diodes, MOSFETs, SITs, VJFETs, Thyristors, and GTOs, have been reported up to now, some of which are now attracting strong interest for real applications.
In the talk, starting from the progress in crystal growth including bulk and epitaxial layers, process technologies for SiC power devices are briefly summarized. The state-of-the-art development in Schottky and pin diodes is introduced. Then, typical demonstrations of transistors for switching devices are described. Among them, the most important issue, "on-resistance", in vertical power MOSFETs, which determines the power loss, is discussed. The main cause to give large value of on-resistance is the mobility value in the inversion channel. Some of trials in oxidation processes to improve the on-resistance of MOSFETs are explained. The idea to utilize the larger value of mobility in accumulation layers, ACCUFETs, is described.
Recent findings of dramatic increase in the inversion channel mobility using different crystal orientations, which the authors have been involved in, will be introduced.

3:00 p.m.
Beyond Y2K: Technology Convergence as a Driver of Future Low-Voltage Power Management Semiconductors, Richard K. Williams, Advanced Analogic Technologies, Inc., USA
The convergence of technology in the 21st century has major implications in the future of electronic products – in design, in semiconductor integration, in portability, in performance, and in power architecture. No longer can power management remain an "afterthought" in the design of such products. The integration of wireless communication into thin-type notebook computers and the addition of computing, Internet access, and video into cell phones greatly complicate the power-management considerations in such portable-connectivity products. Choices regarding the tradeoffs between LDO linear regulators and switching power supplies involve unavoidable compromises regarding cost, noise, size, and battery life. In the office and home, the integration of faster CPUs, high-speed Internet access, high-definition video, and large-area flat-panel monitors are converging into a whole new type of product. In these tethered applications, thermal management, cost, and processor performance are paramount, offering a challenging, albeit totally unique, set of power management issues.
Despite these distinctions, technology convergence is also occurring in semiconductors. The newest generations of analog and power semiconductors under development employ wafer fabrication technologies once limited to only leading edge digital ICs. Mid and deep submicron wafer fabs are now being employed to produce power ICs, discrete power MOSFETs, and mixed-signal ICs with new line-widths and cell densities once thought impossible. The key to such breakthroughs relies not upon upgrading old processes to new fabs, but in customizing new processes to take full advantage of the most modern tools available. Efforts focus on combining recent improvements in silicon etching, anisotropic depositions, low-thermal-budget techniques, CMP planarization and metal plating with novel device and process concepts such as Super-Self-Alignment (SSA), 2D lateral current spreaders, constrained diffusion, and 3D contacts. Improvements in power device electrical performance and resistance are demonstrated to exceed existing technology by factors of 2.5 or better. In power management ICs, integration capability is also improved substantially. The implications of bond-wireless (BWL) and chip scale (CSP) package technologies are also considered.
In the final outcome, connectivity and computer products of the 21st century may comprise only three chips – a highly integrated digital system-on-a-chip / microcontroller, a massive volatile and non-volatile memory array, and an analog-interface / power management system-on-a-chip.

4:00 p.m.
A Review of RESURF Technology, Adriaan W. Ludikhuize, Philips Research, The Netherlands
1. Invention. A higher breakdown voltage usually requires a thicker and lower doped epitaxial layer. Experimental samples with lateral isolation/stopper showed that in this case a thinner layer gives a much higher breakdown voltage: the surface field at the isolation is decreased by 2-D depletion. This Reduced Surface Field (RESURF) effect has an optimum at a top-layer charge of about 1e12 at/cm2 and leads to 2 field peaks, one at the n+ contact, one at the p+ isolation. An integrable 300V LDMOS was observed already in 1972 [1]. The new RESURF technology is published in 1979 [2]: it will allow monolithic integration beyond 1000V and reduce the R-on of HV MOS devices considerably.
2. Resurf in discretes. The first examples use epitaxy for edge termination in 1000V discrete bipolar transistors and in J-FETs. Related work by others uses ion implantation for Junction Termination Extension [G.E., ..], for multiple p- rings, for Kao rings with p- and for graded doping [..] offering generally more flexibility at a lower price. Special care is needed for the surface stability due to the sensitivity for oxide charges and for ambient influences by package and moisture [..].
3. Resurf in J.I. IC's. For IC's the new technology was elaborated in 2 ways. Improvement was obtained by lateral steps in Resurf effect, using stepping field plates[..], multiple implants [..], a local buried p-layer [..] or an extra well at the drain. Improvement was also obtained using vertically profiled layers [3] allowing more charge, leading to double-acting Resurf [4] for lower R-on and for high-side operation in IC's [..]. The explorations resulted in integrated LDMOS and LIGBT up to 1200V [5a,b] using both epitaxial and implantation [..] technology. Resurf devices offer lower feedback capacitance for HF use [..]. Apart from surface stability problems [..] the technology has restriction on its use by bipolar parasitics to the substrate [..], especially with inductive loads (no buried layers), and restriction at high current density by the Kirk effect [..]. IC devices with heavy injection are not allowed.
4. Resurf in SOI. As 2-D depletion effects also work through an intermediate oxide layer, this allows for isolated HV Resurf devices as was done in Dielectric Isolation [..]. The novel wafer-bonded technology allows for the economic integration of all kind of HV and LV devices, including

IGBT and Thyristors. The buried oxide stops all parasitic injection, but has still capacitive coupling (inversion, cross-talk). LDMOS and LIGBT up to 700V on very thin SOI were optimized by using a graded dope increase towards the drain [6], resulting in a constant high field and record-low R-on [7]. Others use thicker SOI isolated by trenches for Resurf devices up to 1000V [..]. The capacitive coupling (no buried or wrap-around heavily-doped layers) and the surface stability still need special attention.

5. Multiple Resurf. As early as 1980 it was conceived to use multiple Resurf regions in charge balance as stacked horizontal layers or vertical regions [8]. Recently, such structures were realized as vertical regions [CoolMOS, 9; Superjunctions, ..] and stripes on SOI [..] with record-low R-on. As in other work, some multiple Resurf designs use 3-D complexity for optimum effect. Resurf is also applied in combination with Trench-type devices [..]. The structures have still to conquer a share in the market.

6. Conclusion. A wide-spread gamma of applications has evolved from the original idea of using 2-D and 3-D depletion effects for a higher breakdown voltage using relatively thin and highly-doped regions. The highest fields do not always occur at the surface, but still the name 'Resurf' is a practical one to indicate the way of operation.

Session: HVIGBT

Chairmen: Y. Seki - H.R. Zeller

8:30 a.m.

IEGT design concept against operation instability and its impact to application

I. Omura, T. Ogura, H. Ohashi*, Toshiba Corp. Semiconductor Company, , *Toshiba Corp. R&D Center, Japan

8:55 a.m.

A high voltage IGBT and diode chip set designed for the 2.8 kV DC link level with short circuit capability extending to the maximum blocking voltage

F. Bauer, N. Kaminski, S. Linder, H.R. Zeller, ABB Semiconductors AG, Switzerland

9:20 a.m.

4.5 kV-2000 A power pack IGBT (Ultra high power flat-packaged PT type RC-IGBT)

T. Fujii, K. Yoshikawa, T. Koga, A. Nishiura, Y. Takahashi*, H. Kakiki*, M. Ichijyou*, Y. Seki*, Semiconductor Device R&D Center, Fuji Electric Co. Ltd., Japan, *Fuji Electric Co. Ltd., Japan

9:45 a.m.

Experimental study of plasma engineering in 6500 V IGBTs

T. Wikström, F. Bauer*, S. Linder*, W. Fichtner, Integrated Systems Laboratory, Switzerland, *ABB Semiconductors AG, Switzerland

10:10 a.m. Break

Session: LDMOS

Chairmen: M. Darwish - I. Yoshida

10:25 a.m.

Low voltage CMOS compatible power MOSFET for on-chip DC/DC converters

S.G. Nassif-Khalil, S. Honarkhah and C.A.T. Salama, University of Toronto, Department of Electrical and Computer Engineering, Canada

10:50 a.m.

Improved 20 V lateral trench gate power MOSFETs with very low on-resistance of 7.8 mΩ.mm2

A. Nakagawa, Y. Kawaguchi*, Advanced Semiconductor Device Research Laboratories Toshiba R&D Center, Japan, *Microelectronics Center, Toshiba Corporation Semiconductor Company, Japan

11:15 a.m.

Folded gate LDMOSFET for low on-resistance and high transconductance

Shuming Xu, Yuanzheng Zhu, Pang-Dow Foo, Yung C. Liang* and Johnny K.O. Sin**, Institute of Microelectronics (IME), Singapore, *Center for Power Electronics, Department of Electrical Engineering, National University of Singapore, Singapore, **Department of Electrical & Electronics Engineering, The HK University of Science & Technology, China

11:40 a.m.

Complementary LDMOS transistors for CMOS/ BiCMOS process

S. Whiston, D. Bain, A. Deignan, J. Pollard, C. NiChleirigh, C. Musgrave, Analog Devices, Ireland

12:05 p.m. Lunch

Session: Superjonction

Chairmen: L. Lorenz - A. Nakagawa

1:30 p.m.

Analysis of the forward biased safe operating area of the super junction MOSFET

B. Zhang, Z. Xu and A.Q. Huang, Center for Power Electronics Systems, USA

1:55 p.m.

MDmeshTM: innovative technology for high voltage power MOS

M. Saggio, D. Fagone, S. Musumeci, ST Microelectronics, Italy

2:20 p.m.

A new generation of power unipolar devices: the concept of the floating islands MOS transistor (FLIMOST)

N. Cézac, P. Rossel, F. Morancho, H. Tranduc, A. Peyre-Lavigne* and I. Pagès*, LAAS-CNRS, France, *Motorola Semiconducteurs SA, France

2:45 p.m.

Which is cooler, trench or multi-epitaxy ?

T. Minato, T. Nitta, A. Uenishi, M. Yano, M. Harada and S. Hine, ULSI Development Center, Power BiCMOS device development Dept., HVIC development group C Mitsubishi Electric Co., Japan

3:10 p.m.

Experimental results and simulation analysis of 250V super trench power MOSFET (STM)

T. Nitta, T. Minato, M. Yano, A. Uenishi and M. Harada,
Mitsubishi Electric Co., ULSI Development Center, Japan

3:35 Break

Session: Process Integration

Chairmen: C.A.T. Salama - J. K.O. Sin

3:50 p.m.

Advantages of thick CVD gate oxide for trench MOS gate structures

K. Nakamura, S. Kusunoki, H. Nakamura and M. Harada
Mitsubishi Electric Co., ULSI Development Center, Japan

4:15 p.m.

Trench corner rounding technology using hydrogen annealing for highly reliable trench DMOSFETs

S.G. Kim, J. Kim, J. Gun Koo, K. Koo Nam, K.I. Cho
Micro-Electronics Technology Laboratory, ETRI, Korea

Tuesday, May 23

4:40 p.m.

Advanced on-chip polysilicon CMOS analog and driver circuit technology for intelligent discrete devices

T. Matsudai, T. Kojima, A. Nakagawa*, Discrete Semiconductor Div, Toshiba Corporation, Japan, *Advanced Discrete Semiconductor Technology Laboratory, Toshiba Corporation, Japan

Session: SiC

Chairmen: T.P. Chow - J.L. Glenn

8:30 a.m.

High temperature static and dynamic characteristics of high voltage 4H-SiC JBS

K. Asano, T. Hayashi, Y. Sugawara and R. Saito*, Technical Research Center, The Kansai Electric Power Company, Japan, *Hitachi Research Lab., Hitachi Ltd., Japan

8:55 a.m.

1500 V, 4 Amp 4H-SiC JBS diodes

R. Singh, S.H. Ryu, J.W. Palmour, A. Hefner Jr.*, J.S. Lai**

Cree Research Inc., USA, *NIST, USA, **Virginia Tech, CPES, USA

9:20 a.m.

A novel high voltage high performance SiC-FET "SIAFET"

Y. Sugawara, K. Asano, R. Singh*, J. Palmour* and D. Takayama, Technical Research Center, The Kansai Electric Power Company, Japan, *CREE Research Corporation, USA

9:45 a.m.

A novel trench-gate power MOST (RMOS) with a narrow band-gap SiGe source region

Ping Li, Yajuan Su, Mengsi You, Xuening Li, Research Institute of Microelectronics, University of Electronic Science and Technology of China, China

10:10 a.m. Break

Session: Diodes

Chairmen: P. Spirito - W. Fichtner

10:25 a.m.

6.5 kV ultra soft & fast recovery diode (U-SFD) with high reverse recovery di/dt capability

M. Mori, H. Kobayashi, Y. Yasuda, Hitachi Research Laboratory, Hitachi Ltd., Japan

10:50 a.m.

Advanced FWD design concept with superior soft reverse recovery characteristics

M. Nemoto, A. Nishiura, T. Naito, M. Otsuki*, Y. Seki*

Semiconductor Device R&D Center, Fuji Electric Co. Ltd.

*Fuji Electric Co., Ltd., Japan

11:15 a.m.

A new degree of freedom in diode optimization: Arbitrary axial lifetime profiles by means of ion irradiation

P. Hazdra, J. Vobrcky, N. Galster*, O. Humbe**, T. Dalibor*

Dept. of Microelectronics, CTU Prague, Czech Republic, *ABB Semiconductors AG, Switzerland, **Integrated Systems Laboratory, ETH Zurich, Switzerland

11:40 a.m.

Real time calculation of the chip temperature of power modules in PWM inverter using a 16 bit microcontroller

T. Reimann, R. Krümmer, U. Franke, J. Petzoldt*, L. Lorenz**

Ilmenau Technical University, Dept. of Power Electronics, Germany, *University of Rostock, Dept of Power Electronics, Germany, **Infineon Technologies, Germany

12:05 p.m. Lunch

Poster Session

P1

High voltage driver built in a low voltage 0.18 μm CMOS for cache redundancy applications in microprocessors

A. Bergemont, I. Saadat, P. Francis, A. Kalnitsky*, Analog Process Technology Developement Group, National Semiconductor, USA, *Maxim Integrated Products, Beaverton

P2

A SOI LDMOS/CMOS/BJT technology for fully-integrated RF poser amplifiers

Y. Tan, M. Kuamr, J. Sin, L. Shi, J. Lau, Department of EEE, The Hong Kong University of Science and Technology, Chine

P3

Advanced power copper technology for Smartmos application designs

I. Pages, B. Baird*, J. Wang*, T. Sicard, J.M. Dorke*I, P. Dupuy, P. Lance, E. Huynh, Y. Chung*, Motorola Semiconducteurs SA, France, *Motorola SPS USA, **LAAS-CNRS, France

P4

Optimization of the body-diode of power MOSFETs' for high efficiency synchronous rectification

J. Zeng, C.F. Wheatley*, R. Stokes, C. Kocon and S. Benczkowski, Intersil Corporation, USA, *Consultant, Intersil Corp., USA

P5

A fast-switching SOI SA-LIGBT without NDR region

J.H. Chun, D.S. Byeon, M.K. Han*, Y.I. Choi, School of Electrical Engineering, Seoul National University, Korea

* School of Electrical Eng., Ajou University, Korea

P6

Improved device ruggedness by floating buffer ring

A.W. Ludikhuize, A. Heringa, R. Van Roijen*,

Philips Research Laboratories, The Netherlands, *Philips Semiconductors, The Netherlands

P7

Implant spacer optimization for the improvement of power MOSFETs' unclamped inductive switching (UIS) and high temperature breakdown

C. Kocon, J. Zeng, R. Stokes, Intersil Corporation, USA

P8

Comparison of high-frequency performance of quasi-SOI and conventional SOI power MOSFETs
Y. Hiraoka, S. Matsumoto, T. Sakai, NTT Telecommunications Energy Laboratories, Japan

P9

Reliability characterization of LDMOS transistors submitted to multiple energy discharges
J.M. Bosc, I. Garcon, E. Huynh, P. Lance, I. Pages, J.M. Dorkel*, G. Sarrabayrouse*, Motorola, France, *LAAS-CNRS, France

P10

Substrate current protection in smart power IC's
O. Gonnard, G. Charitat, Ph. Lance*, E. Stefanov*, M. Suquet**, M. Bafleur, N. Mauran, A. Peyre-Lavigne*, LAAS-CNRS, France, *Motorola SA, France, **SIEMENS Automotive, France

P11

Physical compact modeling of layout dependent metal resistance in integrated LDMOS power devices
M. Kniffin, R. Thoma*, J. Victory**, Digital DNA Laboratories, Motorola SPS, USA, *Digital DNA Laboratories, Motorola SPS, USA, **AMSTC, Motorola SPS, Switzerland

P12

A single poly EEPROM for smart power IC's
E. Carman, P. Parris, I. Pages, H. Chaffai, F. Cotdeloup, S. Debortoli, E. Hemon, J. Lin-Kwang, O. Perat and T. Sicard, Motorola Inc., Switzerland

P13

Tungsten and tungsten silicide (WSix) as gate materials for trench MOSFETs
S. Ambadi, K. Kitt, C. Garcia and J. Pearse, Technology Module Development, ON Semiconductor, USA

P14

Resurfed lateral bipolar transistors for high-voltage, high-frequency applications
G.J. Cao, M.M. De Souza, E.M.S. Narayanan, Emerging Technologies Research Centre, De Montfort University, UK

P15

A unifield high accuracy SPICE library for the power semiconductor devices built with the analog behavioral macromodeling technique
A. Maxim*, D. Andreu, J. Boucher, ENSEEIHT-INP, France
*CIRRUS LOGIC Inc., USA

P16

A 0.8 μm standard CMOS merges one-wire protocol interpreter and 2.5 A-18 V power switch to accomplish low-cost automotive network
C.A. dos Reis Filho, J.A.P. Seminario, M. Jara, S. Finco*, W. Luque, Fundacao Centro Tecnologico para Informatica, Instituto de Microeletrônica, Brasil, *CTI, Centro Tecnologico para Informatica, Brasil

P17

A proposed vertical deep trench RESURF DMOS (VTR-DMOS)
J.L. Glenn, Delphi Delco Electronics Systems, USA

P18

Minority carrier injection across the 3D resurf junction
F. Udrea, R. Ng, A. Popescu, G.A.J. Amaratunga, Department of Engineering, Cambridge University, UK

P19

Dielectric charge traps: A new structure element for power devices
H. Kapels, R. Plikat*, D. Silber, University of Bremen, Germany, *GmbH, Germany

P20

IGBT modul setup with integrated micro-heat sinks
T. Steiner, R. Sittig, Institut für Elektrophysik, Technische Universität Braunschweig, Germany

P21

SiC power devices with low on-resistance for fast switching applications
P. Friedrichs, H. Mitlehner, K.O. Dohnke, D. Peters, R. Schorner, U. Weinert, B. Weis*, D. Stephani, Siemens AG, Corporate Research and Development, *A&D SD E6, Germany

P22

High performance 300 V IGBTs
P.M. Shenoy, J. Yedinak, J. Gladish, Intersil Corporation, Discrete Power Product Development, USA

P23

4500 V trench IEGTs having superior turn-on switching characteristics
H. Ninomiya, J. Takahashi, K. Sugiyama, T. Inoue, S. Hasegawa, T. Ogura, H. Ohashi*, Discrete Semiconductor Div., Toshiba Corporation, *Advanced Discrete Semiconductor Technology Company, Toshiba Corporation, Japan

P24

Evaluation of 600 V/100 A NPT-IGBT with a non-self-align shallow p-well formation technique
M. Otsuki, S. Momota, M. Kirisawa, H. Wakimoto*, Y. Seki, Semiconductor Device R&D Center, Matsumoto Factory, Fuji Electric Co. Ltd., *Fuji Electric Co. R&D LtD., Japan

P25

Double-side packaged, high power IGBTs for improved thermal and switching characteristics
S. Zhao, J. Sin, Department of EEE, The Hong Kong University of Science and Technology, Chine

P26

Static and dynamic characteristics of 600 V, 10 A trench bipolar junction diodes
B. You, A.Q. Huang, J.K.O. Sin* and A. Xu, Center for Power Electronics Systems, USA, *Department of EEE, The Hong Kong University of Science and Technology, Hong Kong

P27

Monolithic bidirectional switch (MBS)
F. Heinke, R. Sittig, Institut für Elektrophysik, Technische Universität Braunschweig, Germany

P28

Characterization of fast 4.5 kV SiC pn-diodes
D. Peters, P. Friedrichs, H. Mitlehner, R. Schoerner, U. Weinert, B. Weis*, D. Stephani, Siemens AG, Corporate Technology, *A&D SD, Germany

P29

Over 2000 V FLR termination technologies for SiC high voltage devices

H. Onose, S. Oikawa, T. Yatsuo, Y. Kobayashi, Hitachi Research Laboratory, Hitachi Ltd., Japan

P30

A newly structured high voltage diode highlighting oscillation free function in recovery process

K. Satoh, K. Morishita*, Y. Yamaguchi*, N. Hirano**, H. Iwamoto, A. Kawakami, Mitsubishi Electric Corp., Power Device Division, *Fukuryou Semicon Engineering Corp., **Melnic Corp. Fukuoka Branch, Japan

P31

Physical phenomena in Si power diodes operating at high carrier injection levels and high temperature

L.M. Hillkirk, B. Breitholtz*, J. Lutz**, KTH, Royal Institute of Technology, Department of Electronics, Sweden, *ABB Corporate Research, Sweden, **Semikron Elektronik GmbH, Germany

P32

Junction termination technique for super junction devices

Y. Bai, A.Q. Huang and X. Li, Center for Power Electronics Systems, USA

P33

The effect of static and dynamic parasitic charge in the termination area of high voltage devices and possible solutions

T. Trajkovic, F. Udrea, P.R. Waind*, G.A.J. Amaratunga, Department of Engineering, Cambridge University, UK, *Mitel Semiconductor, UK

P34

Light triggered thyristor with integrated protection functions

F.J. Niedernostheide, H.J. Schulze, J. Dorn*, U. Kellner-Werdehausen*, D. Westerholt*, Siemens Corporate Research, Germany, *Eupec GmbH, Germany

P35

Thermal analysis of high power IGBT modules

Z. Khatir, S. Lefebvre*, INRETS, France, *LESIR-ENS de Cachan, France

P36

Comparison of stripe and cellular geometry for short circuit rated trench IGBT

C.M. Yun, H.C. Kim, K.H. Lee, J.I. Kim, T.H. Kim, Fairchild Semiconductor, Korea

P37

600 V trench gate NPT-IGBT with excellent low on-state voltage

M. Tanaka, S. Teramae, Y. Takahash*i, T. Takeda, M. Yamaguchi, T. Ogura, T. Tsunoda, S. Nakao, Toshiba Corp. Semiconductor Company, Japan, *Toshiba Corporation, Semiconductor Company, Japan

P38

Experimental measurements of recombination lifetime in proton irradiated power devices

S. Daliento, A. Sanseverino, P. Spirito, G. Busatto*, J. Wyss**, Dip. Ingegneria Elettronica e delle Telecomunicazioni, Italy,*DAEIMI, Universita degli Studi di Cassino, Italy, **ECT European Center of Theoretical nuclear physics and related areas, Italy

P39

Electrical and electrothermal 2D simulations of a 4H-SiC high voltage current limiting device for serial protection applications

F. Nallet, A. Senes*, D. Planson, M.L. Locatelli, J.P. Chante, D. Renault, Centre de Génie Electrique de Lyon (CEGELY), France, *Schneider Electric SA, France

P40

Comparison between finite-Element and analytical calculations for the lifetime estimation of bond wires in IGBT modules

C. Hager, A. Stuck*, Y. Tronel, R. Zehringer*, W. Fichtner, Integrated Systems Laboratory, Swiss Federal Institute of Technology Zürich, Switzerland, *ABB Corporate Research, Switzerland

P41

A novel free wheeling diode for 1700 V IGBT module

N. Iwamuro, T. Iwaana*, F. Nagaune*, Y. Seki*, Fuji Electric Corporate R&D Ltd., Device Technology Laboratory, *Fuji Electric Co., Ltd., Japan

P42

Carrier lifetime characterization using an optimized free carrier absorption technique

F. Hille, H.J. Schulze*, G. Wachutka, Institute for Physics of Electrotechnology, Munich University of Technology, Germany, *Siemens AG, Corporate Research, Germany

P43

Modelling and simulation of the transient electromagnetic behavior of high power bus bars under switching conditions

P. Böhm, G. Wachutka, Institute for Physics of Electrotechnology, Munich University of Technology, Germany

P44

2.3 kVac 100 MHz multi-channel monolithic isolator IC

Y. Kojima, M. Nemoto, S. Yukutake, T. Iwasaki, M. Amishiro, N. Kanekawa, A. Watanabe, Y. Takeuchi*, N. Akiyama, Hitachi Research Laboratory, Japan, *Hitachi Device Development Center, Japan

P45

A novel "cool" insulated base transistor

M.M. De Souza, O. Spulber and E.M.S. Narayanan, Emerging Technologies Research Centre, De Montfort University, UK

P46

A 0.35 μm CMOS based smart power technology for 7 V-50 V applications

V. Parthasarathy, R. Zhu, A. Bose, R. Baird, T. Roggenbauer, D. Collins, S. Chang, P. Hui, M.L. Ger and M. Zunino, SPS, Motorola Inc., USA

4:00 p.m.

Workshop

Tcad tools for Power Devices & Circuits
Pr. W. Fichtner
Integrated Systems Laboratory, Switzerland

Session: Advanced BCD

Chairmen: T.R. Efland - C. Contiero

8:30 a.m.
DMOS implementation in a 0.35 μm BCD technology (BCD6)
C. Contiero, P. Galbiati, A. Merlini, A. Moscatelli, ST Microelectronics, Italy

8:55 a.m.
An economic 100 V RESURF silicon-on-insulator BCD technology for consumer and automotive applications
J. Van der Pol, A. Ludikhuize*, H. Huizing*, B. van Velzen, R. Hueting*, B. van Lijnschoten, G. Hessels, J. Mom, E. Hooghoudt, R. van Huizen, M. Swanenberg, J. Egbers, H. Schligtenhorst*, J. Soeteman, Philips Semiconductors, The Netherlands, *Philips Research, The Netherlands

9:20 a.m.
Multi-voltage device integration technique for 0.5 μm BiCMOS & DMOS process
T. Terashima, F. Yamamoto, K. Hatasako, ULSI Development Center, Mitsubishi Electric Corporation, Japan

9:45 a.m.
A 65 V, 0.56 mΩ.cm2 resurf LDMOS in a 0.35 μm CMOS process
R. Zhu, V. Parthasarathy, A. Bose, R. Baird, T. Roggenbauer, D. Collins, S. Chang, P. Hui, M.L. Ger and M. Zunino, SPS, Motorola Inc., USA

10:10 a.m. Break

Session: Energy Capability

Chairmen: M.A. Briere - A. Ludikhuize

10:25 a.m.
SCR-LDMOS - A novel LDMOS device with ESD robustness
S. Pendharkar, R. Teggatz, J. Devore, J. Carpenter, T. Efland, C.Y. Tsai, Texas Instruments Inc., USA

10:50 a.m.
Using "adaptive Resurf" to improve the SOA of LDMOS transistors
P.L. Hower, J. Lin, S. Merchant, S. Paiva, Unitrode Corporation, USA

11:15
A new power MOSFET having excellent avalanche capability
T. Uesugi, T. Suzuki, T. Murata, S. Kawaji and H. Tadano, Toyota Central R&D Labs., Japan

12:05 p.m. Lunch

Session: IGBT

Chairmen: Y. Uchida - G. Amaratunga

1:30 p.m.
The Field Stop IGBT (FS IGBT) - A new power device concept with a great improvment potential
T. Laska, M. Münzer*, F. Pfirsch, C. Schäffer**, T. Schmidt***
Infineon Technologies, Germany, *Eupec, Warstein, **Infineon Technologies EZM, Villach, ***Infineon Technologies OHG, Villach

1:55 p.m.
Analysis on the low current turn-on behavior of IGBT module
M. Otsuki, S. Momota, K. Ishii, H. Takubo, Y. Seki, Semiconductor Device R&D Center, Matsumoto Factory, Fuji Electric Co. Ltd., Japan

2:20 p.m.
Optimizing 600 V punchthrough (PT) IGBT's for uncfor unclamped inductive switching (UIS)
J. Yedinak, P. Shenoy, G. Dolny, B. Wood, T. Morthorst, D. Lange, Intersil Corporation, Discrete Power Product Development, USA

2:45 p.m.
A new void free soldering process in large-area, high power IGBT modules
J. Onuki*, M. Nihei, R. Saito, M. Kitano*, Hitachi Research Laboratory, Japan, *Akita Prefectural University, Faculty of Science and Technology, Japan, **Mechanical Engineering Research Laboratory, Japan

Session: Trench

Chairmen: D.M. Kinzer - R.K. Williams

3:25 p.m.

High density, sub 10 mohm rdson 100 Volt N-channel FETs for automotive applications

S. Sobhani, D. Kinzer, L. Ma, D. Asselanis, International Rectifier Corp., USA

3:50 p.m.

A 0,35 μm trench gate MOSFET with an ultra low on state resistance and a high destruction immunity during the inductive switching

A. Narazaki*, J. Maruyama**, T. Kayumi, H. Hamachi***, J. Moritani and S. Hine, Mitsubishi Electric Corp., *Ryouden Semiconductor System Engineering Corp., **Kyokuyou Semiconductor Corp., ***Fukuryou Semiconductor Engineering Corp., Japan

4:15 p.m.

High-density low on-resistance trench DMOSFETs employing oxide spacers and self-align technique

Jongdae Kim, Sang-Gi Kim, Jin Gun Koo, Kee Soo Nam, Kyoung-Ik Cho, Micro-Electronics Technology Laboratory, Electronics and Telecommunications Research Institute Yusong, Korea

4:40 p.m.

Dummy gated VDMOSFET with high breakdown voltage and low feedback capacitance

Shuming Xu, Changhong Ren, Pang-Dow Foo, Yong Liu and Yi Su, Institute of Microelectronics (IME), Singapore

5:05 p.m.

Concluding remarks