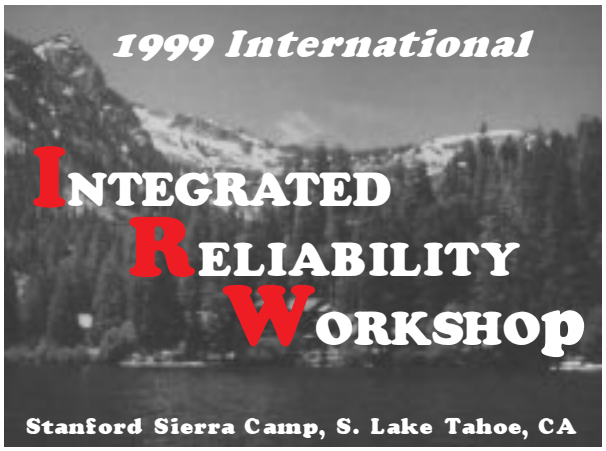

October 18-21, 1999

http://www.irps.org/irw/

IEEE/Integrated Reliability Workshop
P.O. Box 308
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PROGRAM ANNOUNCEMENT!

Workshop Experience

You are cordially invited to participate in the 1999 Integrated Reliability Workshop. It provides a unique environment for envisioning, developing, and sharing reliability technology for present and future semiconductor applications. Here you will closely interact with your peers at moderated discussion groups, open poster sessions, technical presentations, and special interest groups. All Workshop activities take place in a relaxed and rustic setting that promotes an atmosphere of interactive learning and knowledge sharing. You should come away from the workshop intellectually refreshed!

'99 Workshop Features:

- ★ **Keynote**
  - Semiconductor System Design *Influencing Factors for consideration of Future Generation System Design*
- ★ **Group Discussions**
  - Fast WLR monitoring
  - Burn In
  - Thin Oxide Limits
  - Electromigration
  - Hot-Carriers
- ★ **Tutorials**
  - Basic Reliability
  - Hot-Carriers
- ★ **24+ Technical Presentations on:**
  - Customer Product Reliability Requirements
  - Reliability Test Structures
  - Reliability Models
  - Identification of Reliability Effects
  - Wafer Level Reliability
- ★ **Open Poster Sessions**
- ★ **Special Interest Groups**

Major Technical Themes

Increased performance, reduced cost, shortened design cycles, new markets – these have driven rapid growth and still unprecedented technical innovation in the semiconductor industry. To meet these demands, new materials and processes are continually introduced for use in deep sub-micron technology; necessitating updated and or new models for reliability determination.

Reflecting these trends, discussion groups will focus on a broad range of topics that reflect the diversity of the engineers and scientists who attend the workshop. **Electromigration** (EM) remains a reliability concern for the IC industry and that discussion group will address EM in Cu metallizations, wafer level EM testing and the effects of low-K dielectrics on EM and EM testing. Since traditional testing techniques are not applicable for monitoring and characterizing **the integrity and reliability of ultra-thin oxides**, a discussion group devoted to the topic is also planned for this year's workshop. Issues such as intrinsic reliability limits and the controversy over constant voltage vs. constant current testing will be among those discussed by the participants in this group. Another group planned for this year will be devoted to sampling experiences with **Burn-In** among the participants. They will be evaluating recent developments and discussing possible strategy changes to address future industrial needs regarding Burn-In. Participants will also have the opportunity to continue their discussion on **Hot Carrier Degradation** from tutorial #1, addressing issues such as the impact of proposed drain structures on reliability, interface trap generation and the charge trapping/detrapping phenomena under Hot-Hole injections and Hot-Electron injections.

The technical program begins with a challenging keynote on end user factors that can influence system design methodology.

A session on customer product reliability requirements focuses on present day challenges; the reliability impact of low temperature operation; burn-in design, the use of circuits repaired by focus ion beam, and stress voiding in sub micron metallization. An identification of reliability effects session discusses copper and low dielectric constant interconnects and optimized WLR for aluminum evaluations. Reliability modeling brings papers on hot carriers, thermal interconnect reliability effects, and many limiting oxide failure types for discussion. A session on reliability test structures focuses heavily on future electromigration test structure needs including the accounting for temperature gradients, and also describes a non destructive means to study oxide plasma damage. Concluding the workshop is a very exciting session on wafer level reliability. The physics of thin oxide failures both soft and hard are discussed in conjunction with many new analysis techniques such as a fast detection ramp, constant current versus constant voltage acceleration, and test structure designs and stress for discerning these scaled oxides.

Discussion groups will meet on Tuesday and Wednesday evenings. This year you may participate each evening in one of five moderated topics (WLR monitoring, Burn-In, Thin Oxide Limits, Electromigration, Hot Carriers) *...don't forget to circle your choice on the registration form.*

The **Special Interest Groups (SIGs) program** at the Workshop has been very successful in fostering collaborative work on important reliability issues and we look forward to continuing growth and renewal in our SIGs. The formation of SIGs is encouraged as a natural extension of the Discussion Group sessions. Anyone interested in more information on SIGs see http://www.irps.org/irw/sig/.

–over–

KEYNOTE: INDUSTRY SYSTEM DESIGN:

INFLUENCING FACTORS FOR CONSIDERATION OF FUTURE GENERATION SYSTEM DESIGN—*Benjamin DeLuca, International Business Machines, Austin, Tx*

Customer expectations for future systems continue to increase year to year. One of the key drivers are web based applications. As these applications become ever more pervasive customers expect and require 24 hour a day, 7 days a week availability. Systems engineers are now required to develop systems with this in mind so that competitive products are offered. In many cases our customers business directly depends on having virtually continuous availability. Examples such as airline reservation systems, on-line banking, and on-line catalog shopping are becoming the norm. Customers demand and expect high reliability, ease of use, flexible growth and high value for the dollar.

These customer requirements translate into several important system characteristics. Systems are now designed in a manner to eliminate single points of failure. One aspect of this is to offer redundant elements like cooling fans, power supplies, data storage devices, memory, and in some cases CPU's. In the case of adapters we sometimes need to use multi-ports to provide multiple paths to data storage devices or networks. Given that some system failures are inevitable we need to protect the customer environment to carefully manage the effects of these incidents. This management requires a robust software environment and an effective warning system to identify units that need replacement prior to an unscheduled outage. We can then use concurrent maintenance to replace the failing element without having to take the customers application down. We also can utilize remote service facilities to automatically call the suppliers' service center to dispatch the replacement elements. Many of these actions are dependent on effective system diagnostics and effective failure isolation.

As we design future systems we need to carefully consider the component reliability and failure characteristics such that they support robust system functionality. Given thermal considerations and its effect on reliability one must carefully consider the power of the devices required. Selecting low power components with highly integrated functions eliminate multiple points of failure and keep thermal loads down. System designs need to reduce opportunities for failure, by minimizing cables, connectors and cards required providing necessary function. These considerations must be primary in the design of our systems since the reliability, availability and serviceability are the elements one can use to further differentiate oneself in the marketplace. Our designs need to begin with the end user in mind since our performance will ultimately be limited by the fundamental technology choices we make.

TUTORIALS

TUTORIAL 1 – BASIC RELIABILITY

A. ELECTROMIGRATION—*Tim Sullivan, IBM Microelectronics*

Electromigration is the electron-flow-induced migration of metal atoms in a conductor, and can lead to resistance increases and failure.Time to failure is generally lognormally distributed, and the median time to failure is related to the applied current density and temperature by Black's equation, $t_{(50)} = Aj^{-n}\exp(h/kT)$. Electromigration has been studied for over 30 years, and considerable understanding of the process has been gained. However, metallization-specific phenomena occur frequently enough to prevent many global generalizations. Structural effects can be large enough to obscure or enhance EM damage. Electromigration testing for a technology is therefore somewhat of an art in which the reliability engineer combines knowledge of physics and electronics with intuition experience to create test structures which will probe the electromigration robustness of a new technology. These structures are tested under accelerated conditions to produce a distribution of failure times, which are then fit to a lognormal distribution, and extrapolated to use conditions. The extrapolated failure time is compared to the business target to determine the allowed current density for the technology.

B. (ULTRA)THIN OXIDE BREAKDOWN(S), AN OVERVIEW—*Emmanuel Vincent, STMicroelectronics, Central R&D Labs*

Silicon dioxide layer reliability has always been a major issue for semiconductor manufacturers. In particular the gate oxide breakdown is well known to be one of the potential limiting failure modes affecting the MOS devices. Moreover, as the gate oxide thickness scales from the thin (above 5nm) down to the ultrathin (below 5nm) range, the oxide reliability becomes more and more critical and, before the classical breakdown, novel phenomena appear for ultrathin oxides such as quasi-breakdown events. This evolution, these changes require at least revised, even novel approaches in order to realistically address the ultrathin oxide reliability in deep-submicron technologies.

This tutorial will give a general overview of the breakdown phenomena in thin and ultrathin SiO_2 films highlighting the behavior differences between both thickness ranges and their impact on the ultrathin oxide reliability. The following items will be addressed:

Testing methodology

Physical understanding of the failure mechanisms

Extrapolation modeling

C. BURN-IN—*Rolf-P Vollertsen, Infineon Technologies Corp.*

Burn-In is used to screen weak parts from a population of completely processed chips. Thereby it helps to meet reliability requirements. This tutorial will provide a general introduction to Burn-In. It will show how Burn-In improves the failure rate and in which cases it is useful. The benefits and disadvantages will be addressed as well as the Burn-In conditions, models and failure mechanisms. There will be a section discussing the impact of Burn-In on technology reliability (hot carriers, gate oxide, electromigration). Frequently the upper limits of the Burn-In conditions are controlled by technology reliability.

TUTORIAL 2 – HOT CARRIERS:

A. HOT CARRIER DEGRADATION EVOLUTION IN DEEP SUBMICROMETER CMOS TECHNOLOGIES—*Alain Bravaix, ISEM*

Since the beginning of the seventies, the performance increase of microelectronics industry has been obtained mainly by decreasing the size of circuit features. This strong miniaturization obtained by process optimization and technology improvement has imposed to change the circuit scaling scheme as device reliability is become a major challenge. Hot-Carrier (HC) degradation has been one of these limiting factors in MOSFET's for digital and memory applications which has led to new technological processes, *e.g.* new drain structures (LDD, LATID, GOLD) and hardened gate-dielectrics (nitrided oxide). For the new generation technologies, DC lifetime evaluation obtained on single devices needs to be adapted to the case of real circuits as the interaction between the different damage mechanisms complicate the evaluation of the resultant damage during AC operations. This tutorial will address the following topics:

1. HC injection phenomena in MOSFET's will be reviewed focussing on the different degradation behaviors in N- and P-channel MOSFET's.
2. The impact of some proposed drain structures on the HC reliability will be discussed. Emphasis will be put on AC alternating stress conditions in order to assess the role of the interface trap generation and the charge trapping/detrapping phenomena under Hot-Hole (HH) injections and Hot-Electron (HE) injections.
3. The correlation between transistor degradation and circuit reliability will be discussed based on duty-cycle calculations focussing on the gate-oxide thickness (T_{ox}) reduction for digital applications. Hence, the degradation of inverter and ring oscillators will be investigated which exhibit new competitive damage mechanisms.
4. The particular case of pass transistor degradation used in SRAM cells will be further analysed as it represents a more severe case than the two latter circuits.
5. Finally the effect of temperature on the defect generation in the range –40° to 125°C will be discussed.

B. SIMULATION, MODELING AND LIFETIME PREDICTION FOR HCI—*Bruce W. McGaughy, BTA Technology, Inc.*

This part of the tutorial will provide an overview of simulation, modeling and lifetime prediction of hot carrier degradation as follows:

(1) Modeling the Hot Carrier Effect.
- a. Interface states.
- b. Gate oxide trapping.
- c. Degraded SPICE models.
- d. Delta-Mos model.
- e. Gate level macromodeling of speed degradation.

(2) Simulating the Hot Carrier Effect
- a. Transistor-level simulation
- b. Gate-level simulation.

(3) Lifetime Prediction
- a. Device Level
- b. Circuit Level

(continued on back of registration form)

1999 *International*
INTEGRATED RELIABILITY WORKSHOP

PRELIMINARY PROGRAM

MONDAY, October 18

1:00 – 8:00 p.m. Lodge check-in. Get room assignment (prearranged) & room key, with lodge area map and information. (ADA please notify desk of special needs)

1:00 – 6:00 p.m. Registration: Pick up badges & handout (*Dining Room Lounge*)
Discussion Group Assignments / SIG Signup

1:30 – 3:30 p.m. Tutorial Session #1: "Basic Reliability" *(Angora Room)*
"Electromigration"
"Ultra Thin Oxide Breakdown"
"Burn-In"

3:45 – 5:45 p.m. Tutorial Session #2: "Hot-Carriers" *(Angora Room)*
" Simulation, modeling and lifetime prediction"
"Hot Carrier degradation evolution in deep submicrometer CMOS technologies"

5:45 – 6:15 p.m. Registration: Pick up badges and handout (*Dining Room Lounge*)
Discussion Group Assignments/SIG signup

6:15 – 7:30 p.m. DINNER, *(Dining Room)*

7:00 – 7:30 p.m. Registration for Late Arrivals (*Dining RoomLounge)*

7:30 – 9:00 p.m. Mixer & Poster Session, *(Cathedral Room)*

9:00 – 10:00 p.m. SIG Meeting (all SIGs), *(Angora Room)*

TUESDAY, October 19

6:30 – 8:00 a.m. BREAKFAST *(Dining Room)*

8:15 – 8:30 a.m. Welcome & Introduction: Eric Snyder, General Chair, *(Angora Room)*
Technical Program Overview: William Tonti, Technical Program Chair

8:30 – 9:30 a.m. Keynote: "Influencing Factors for Consideration of Future Generation System Design"—Benjamin DeLuca, International Business Machines, Austin, Tx

9:30 – 10:00 a.m. Break

10:00 – 11:40 a.m. Session #1: Customer Product Reliability Requirements (CPR), Chairs: Bill Vigrass, Texas Instruments & Rolf-P. Vollertsen, Infineon Tech. Corp.

- CPR-1 "A Methodology to Assess the Influence of Burn-In Relating to Long Term Reliability of Submicron CMOS Transistors," S. Holzhauser and A. Narr of Infineon Technologies AG I.Gr.
- CPR-2 "Signal Margin Test to Identify Process Sensitivities Relevant to DRAM Reliability and Functionality at Low Temperatures," E. Nelson of IBM Microelectronics, Essex Jct. VT; Y. Li, D. Poindexter of IBM Semiconductor R&D Center, Hopewell Jct NY; M. Ruprecht of Infineon Corp., E. Lim of Semiconductor R&D Center, Hopewell Jct NY; Y. Matsubara, H. Sawasaki of Toshiba Corp.; Q.Ye of Infineon Corp., W. Tonti of IBM Microelectronics, Essex Jct. VT
- CPR-3 "Reliability Aspects of Stress Induced Voiding in 0.25 µm Metallization," A.E. Zitzelsberger, M.U. Lehr of Infineon Technologies
- CPR-4 "Reliability Test Results for W FIB Interconnect Structures," M. Zaragoza, Z. Zhang of Cadence Design Systems and M. Abramo of IBM Microelectronics

11:40 – 12:10 p.m. Group Picture

12:10 – 1:30 p.m. LUNCH, *Dining Room*

2:00 – 3:40 p.m. Session #2 Reliability Test Structures (RTS), Chairs: Homi Nariman, Advanced Micro Devices and Tim Sullivan, IBM Microelectronics

- RTS-1 "Predicting Plasma Charging Damage to Ultrathin Gate Oxide by Using Nondestructive DCIV Technique," H. Guan, M.F. Li, Y.H. Zhang, S. Ma, and B.J. Cho of National University of Singapore
- RTS-2 "Temperature Gradient Effects in Electromigration Using an Extended Transition Probability Model and Temperature Gradient Free Tests," K. Jonggook, V.C. Tyree, and C.R. Crowell of University of Southern California
- RTS-3 "An Evaluation of Electrical Linewidth Determination Using Cross-Bridge and Multi-Bridge Test Structures," , L.M. Head of Rowan University and H.A. Schafft of National Institute of Standards and Technology
- RTS-4 "Impact of Test-Structure Design and Test Methods for Electromigration Testing," S. Menon of LSI Logic; J. Fazekas, J. von Hagen of Infineon; L.M. Head of Rowan University; and H.A. Schafft of National Institute of Standards and Technology

3:40 –4:00 p.m. Break

4:00 – 5:15 p.m. Session #3 Reliability Models A (RMA), Chairs: Gordon Claudius, Conexant and John Suehle, National Institute of Standards and Technology

- RMA-1 "Second Order Thermal Dissipation Effects for Embedded Interconnects," J.P. Gill, D.L. Harmon, J. Furukawa, and T.D. Sullivan of IBM Microelectronics
- RMA-2 "Hot-Carrier Damage In Deep-Submicrometer CMOS Technologies," A. Bravaix, D. Goguenheim of ISEM, and N. Revil, E. Vincent of STMicrolectronics
- RMA-3 "Dependence of HCI Mechanism on Temperature and Direct Tunneling Oxide Thickness for 0.18 µm Technology and Beyond," W. Wang, J. Tao and P. Fang of Advanced Micro Devices

5:15 – 6:00 p.m. Poster Session/Late News Papers

6:00 – 7:30 p.m. DINNER, *Dining Room*

7:30 – 9:00 p.m. Discussion Groups,: Chairs: Linda M. Head, Rowan University and Prasad Chaparala, National Semiconductor Corp.
(90 minute parallel sessions for each topic) Attendees are to participate in one of the five groups:

1. Fast WLR monitoring: *Carole Graas , Infineon Technologies & Ehren Achee, Centaur Technology*
2. Burn In: *Rolf-P Vollertsen, Infineon Technologies and Raif Hijab, Cirrus Logic Inc.*
3. Thin oxides limits: *Emmanuel Vincent STMicrolectronics and John Suehle National Institute of Standards and Technology*
4. Electromigration*: Tim Sullivan, IBM Microelectronics and Harry A. Schafft, National Institute of Standards and Technology*
5. Hot Carriers: *Alain Bravaix, ISEM*

9:00 – 10:30 p.m. Individual SIG Meetings, Chair: Linda M. Head, Rowan University

WEDNESDAY, October 20

6:30 – 8:00 a.m. BREAKFAST *(Dinning Room)*
8:15 – 8:30 a.m. Announcements, *(Angora Room)*
8:30 – 9:20 a.m. Session #4: Identification of Reliability Effects (IRE), Chairs: Udo Schwalke, Infineon Technologies and Raif Hijab, Cirrus Logic Inc.
- IRE-1 "Conduction Mechanisms in Cu/Low-K Interconnect," G. Bersuker, V. Blaschke, D. Pekker, and W. Wick of Sematech
- IRE-2 "A Successful Application of WLR Fast Test on Al Via Process Optimisation," X. Liu, K.F. Lo, Q. Guo, and J. Cai of Chartered Semiconductor Manufacturing Ltd.

9:20 – 10:00 a.m. Break
10:00 – 12:10 p.m. Session #5 Reliability Models B (RMB), Chairs: John F. Conley Jr., Dynamics Research Corp. and Prasad Chaparala, National Semiconductor Corp.
- RMB-1 "Limiting Oxide Failure Mode versus Oxide Thickness. Some Insights for Deep-submicron Technologies.," S. Bruyere of STMicroelectronics and LPCS/ENSERG; E. Vincent of STMicroelectronics; and G. Ghibaudo of LPCS/ENSERG
- RMB-2 "Breakdown Voltage Distribution and Extrinsic TDDB Failures of MOS Gate Oxides," H. Katto, Science University of Tokyo, Suwa College
- RMB-3 "Simulation of Hot-Carrier Degradation Using Self-Consistent Solution of Semiconductor Energy-Balance Equations and Oxide Carrier Transport Equations," M.P. Pagey, S.K. Mukundam, R.D. Schrimpf, and K.F. Galloway of Dynamics Research Corporation
- RMB-4 "Product Reliability and Maximum Voltage Limits from Extrinsic Gate Oxide Voltage Ramp Data," R. Hijab of Cirrus Logic Inc.

12:15 – 1:30 p.m. LUNCH, *(Dining Room* — Take out Lunch bags available)
1:30 – 4:30 p.m. Open The afternoon is free for discussion, hiking and other recreation
4:30 – 6:00 p.m. Mixer & Poster Session, *(Cathedral Room)*
6:00 – 7:30 p.m. DINNER, *(Dining Room)*
7:30 – 9:00 p.m. Discussion Groups,: Chairs: Linda M. Head, Rowan University and Prasad Chaparala, National Semiconductor Corp.
(90 minute parallel sessions for each topic) Attendees are to participate in one of the five groups:
1. Fast WLR monitoring: *Carole Graas , Infineon Technologies & Ehren Achee, Centaur Technology*
2. Burn In: *Rolf-P Vollertsen, Infineon Technologies and Raif Hijab, Cirrus Logic Inc.*
3. Thin oxides limits: *Emmanuel Vincent STMicrolectronics and John Suehle National Institute of Standards and Technology*
4. Electromigration*: Tim Sullivan, IBM Microelectronics and Harry A. Schafft, National Institute of Standards and Technology*
5. Hot Carriers: *Alain Bravaix, ISEM*

9:00 – 10:30 p.m. Individual SIG Meetings

THURSDAY, October 21

6:30 – 8:00 a.m. BREAKFAST (*Dining Room*)
8:15 – 8:30 a.m. Announcements, *(Angora Room)*
8:30 – 9:45 a.m. Session #6: Wafer Level Reliability, Chairs: Doug Menke, Motorola, and Harry A. Schafft, National Institute of Standards and Technology
- WLR-1 "New Experimental Findings on Constant Voltage and Current Soft-Breakdown in Ultra-Thin Oxides," D. Brisbin of Keithley Instruments and P. Chaparala, National Semiconductor Corp.
- WLR-2 "The Sensitivity and Correlation Study on Jramp Test and High-Field, Constant-Voltage Stress Test for WLR," Y. Chen, F. Li, P.M. Mason, Y. Ma, and A.S. Oates of Bell Labs, Lucent Technologies
- WLR-3 "Analysis of Evolution To and Beyond Quasi-breakdown in Ultra-thin Oxide and Oxynitride," M. Okandan, S.J. Fonash of The Pennsylvania State University; B. Maiti, H.H. Tseng, and P. Tobin of Motorola APRDL

9:45 – 10:30 a.m. Break (checkout at this time if not staying for JEDEC meeting)
10:30 – 11:45 a.m.
- WLR-4 "New Experimental Findings on SILC and Soft Breakdown of Ultra-Thin Gate Oxides," M.G. Chen , C.H. Liu, M.T. Lee, and K.Y. Fu of United Microelectronics Corp.
- WLR-5 "A New Fast Ramp Technique to Detect Breakdown in Ultra-thin Dielectrics," E.S. Snyder and D.G. Pierce of Sandia Technologies
- WLR-6 "WLR Monitoring Stresses and Suitable Test Structures for Future Product Reliability Targets," A. Martin, M. Kerber, and G. Diestel of Infineon Technologies AGi. Gr.

11:45 – 12:00 p.m. Discussion Group Summaries
12:00 – 12:15 p.m. SIG Report
12:15 – 12:30 p.m. Wrap-Up
12:30 – 1:30 p.m. LUNCH, *(Dining Room)* and then the Workshop Ends—Leave the Stanford Sierra Camp unless attending JC14.2
2:00 p.m. JEDEC 14.2 Committee on Wafer Level Reliability Meeting

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1999 IRW REGISTRATION FORM (Use also for reserving accommodations to EIA/JEDEC Committee JC14.2 meeting, Oct. 21-22)

(Please type, print or attach business card) *Meeting registration automatically includes a room reservation.*

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** Includes all meals, lodging, Handout, & Final Report. (Mon. eve., Oct. 18–Thur. noon, Oct. 21)*

EXTRA COPIES of Workshop Final Report ..... Qty: _____ x $80 _____
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TOTAL REMITTED $ _____

Cancellation fees: $50 after Sept. 24 ; full fee after Oct. 8

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TAHOE CASINO EXPRESS: The Tahoe Casino Express **runs from Reno to Tahoe** between 6 a.m. and midnight with departures from Reno at: 6:15 a.m., 8:15, 9:15, 10:15, 11:15, 12:15 p.m., 1:15, 2:15, 3:15, 5:30, 7:30, 9:30, 10:30 and 12:30 a.m. The Express costs $17 each way ($30 round trip) and tickets can be purchased at the Express counter located in the baggage area in the Reno airport. Travel time is approximately 1½ hours. The Casino Express can be reached at 800-446-6128. The Express **leaves the Horizon Casino at Lake Tahoe and returns to Reno** on the following schedule: 4:10 a.m., 6:10, 8:10, 9:10, 10:10, 11:10, 12:10 p.m., 1:10, 2:10, 3:10, 4:10, 5:10, 7:25, and 10:25 p.m. Tickets may be purchased in the Horizon Casino at the main cashier's cage.

Stanford Sierra Camp offers courtesy transportation for conference attendees from the Horizon Casino between 10 a.m. and 10 p.m. on Registration Day (Monday, Oct. 18). Return trips to the Casino are offered on the last day of the conference only. If you are planning on using the Casino Express, please notify Stanford Sierra Camp (530-541-1244) at least ONE WEEK prior to your arrival date. If you find yourself stranded, please call the camp at the same number. The IRW Arrangements Committee may be able to provide emergency service to and from the casino.

(continued from page 2)

Discussion Groups: *Chairs: Linda M.Head, Rowan University and Prasad Chaparala, National Semiconductor Corp.*

The evening discussion group program is regarded as a favorite highlight of the workshop experience. Attendees will have a choice of 5 topics on both Tuesday and Wednesday evenings. The same 5 topics will be discussed for 90 minutes each night. This year's topics are:

1. FAST WLR MONITORING: *Carole Graas , Infineon Technologies & Ehren Achee, Centaur Technology*

Wafer Level reliability, or WLR, refers to a category of stresses which are performed by directly applying temperature, voltage, and/or current stress on specially designed test structures, thus quickly providing data on a wide range of reliability issues. Because of their flexible design and use, WLR tests have become pervasive in the Microelectronics Industry, for applications ranging from technology/process development, to the monitoring of manufacturing lines.

By and large, the success of WLR has resided in its ability to provide useful data at elevated stress conditions in a very small amount of time (sec to min), compared to package-level testing. In a fast paced, high volume development or production environment, stepping from "WLR" to "fast WLR" is easily done. But what exactly is "fast WLR", and how can it be useful to you — and your boss?

We hope that by participating in this discussion group, you will come away with answers to these, and other questions, such as:

- Advantages/disadvantages of fast WLR.
- Isn't WLR fast enough?
- How widely is fast WLR used – should you switch?
- Use which physical models for the interpretation of fast WLR data?
- Success stories, etc...

2. BURN IN: *Rolf-P Vollertsen, Infineon Technologies and Raif Hijab, Cirrus Logic Inc.*

Burn-In is an integral part of IC productions. It serves to screen weak parts and improve the failure rate during early life. Besides this benefit it is expensive and it might degrade intrinsic properties by the high stress conditions or introduce additional fails due to ESD or handling problems. Considerations on how to reduce Burn-In cost and increase screen efficiency lead to concepts like wafer level Burn-In or IDDQ measurements. However, the success of alternative measures depends on the failure mechanism.

The goal of the discussion group is to sample the experience with Burn-In among the participants, evaluate recent developments and discuss possible strategy changes to address future needs.

Discussion topics of interest are:

- How effective is Burn-In in general and for certain failure mechanisms?
- What are the risks of Burn-In and how to limit those?
- Why is the usefulness of Burn-In product dependent?
- How can Burn-In be optimized?
- Do we need Burn-In at all and why?
- How to replace or eliminate Burn-In?
- What are the alternatives and do they work reliably?

3. THIN OXIDES LIMITS: *Emmanuel Vincent, STMicrolectronics and John Suehle, National Institute of Standards and Technology*

Characterizing Ultra-thin Gate Dielectrics: Do we know what we are doing ?
Characterizing the reliability of ultra-thin gate oxides presents a new challenge to quality and reliability engineers. Traditional testing techniques are not applicable for monitoring and characterizing the integrity and reliability of ultra-thin films.
Discussion topics include:

- soft breakdown detection and physics
- constant voltage vs. constant current testing
- validity of charge-to-breakdown
- intrinsic reliability limits
- SILC
- alternative dielectric materials.

4. ELECTROMIGRATION: *Tim Sullivan, IBM Microelectronics and Harry A. Schafft, National Institute of Standards and Technology*

Focal points for discussion will include the following.

- New observations and issues in Al-based metallization, such as comparison of and/or standardization of structures for qualification purposes, effects of more complex shapes (e.g., branches), and bridging from one structure to another.
- EM in Cu metallizations; differences from Al, (e.g.,linewidth dependence, deposition method, etc.); failure criteria, possible pitfalls of high-temperature testing
- Wafer level EM for both Cu and Al; effects of different structures on failure distributions, self-heating, type test algorithm.
- Effects of low-K dielectrics on EM and EM testing.

The intent of the discussion group will be to explore areas of interest to the participants in a casual environment. The moderators will have material to stimulate discussion, but no set agenda will be followed.

5. HOT CARRIERS: *Alain Bravaix, ISEM*

Hot-Carrier (HC) degradation has been one of the limiting factors for performance increases in MOSFET's for digital and memory applications. Efforts to minimize HC degradation have led to new technological processes, *e.g.* new drain structures (LDD, LATID, GOLD) and hardened gate-dielectrics (nitrided oxide). This discussion group will focus on the HC injection phenomena in MOSFET's. Some of the topics that will be addressed are:

- The impact of some proposed drain structures on reliability.
- Interface trap generation and the charge trapping/detrapping phenomena under Hot-Hole (HH) injections and Hot-Electron (HE) injections.
- The correlation between transistor degradation and circuit reliability.
- Effect of temperature on the defect generation in the range –40° to 125°C will be discussed.

TWO OPEN POSTER SESSIONS. *All attendees have the opportunity to present a poster to communicate their ideas and results on a technical project or issue.* Please indicate your intention to bring a poster by reserving a poster display board (32"×40" or 81 cm×100 cm) in the space provided on the registration form. Your work should be in Landscape format on 8½×11" or A4 paper with a maximum of twelve pages. In addition, you are invited to submit a two-page abstract of your poster presentation for inclusion in the Workshop Final Report. See www.irps.org/irw/poster/ for details and deadlines. This is a great opportunity for you to share your work with your peers.

JEDEC 14.2 MEETING. The JEDEC 14.2, Wafer Level Reliability Standards Committee, meeting will be held immediately after the Workshop at the Stanford Sierra Camp on Thursday afternoon and Friday morning. Members, alternates, and guests are welcome. The cost for the accommodations is $160.00, which includes Thursday night dinner and lodging *and* Friday breakfast and lunch. All attendees must leave the camp after lunch on Friday. If you have any questions or if you want to become a member of JC-14.2, please call the JEDEC office at (703) 907-7558 or www.jedec.org or call Mike Dion, JC-14.2 Chair, at (407) 724-7067.

MORE INFORMATION. We expect an exciting workshop again this year. We look forward to your active participation in the many Workshop activities and your valuable contribution to the technical discussions. If you have additional questions, please contact the Technical Program Chair, William R. Tonti, by phone, 802-769-6561; fax ...6567; or e-mail: wtonti@us.ibm.com, or the General Chair, Eric S. Snyder, at 505-872-0011; fax...0022; or e-mail: snyderST@aol.com. Web site: www.irps.org/irw .

REGISTER NOW!

Complete and send in the enclosed registration form. Please register early. We have sold out in past years. Space at the Camp limits IRW to roughly 120 attendees. We look forward to seeing you at the '99 Workshop!

Sincerely,

William R. Tonti
Technical Program Chair

RESPONSIBILITIES OF ATTENDEES

You are expected to come prepared to participate actively in the discussions and meetings by sharing your experiences, concerns, questions, views, technical information, and test data, as appropriate. Your active involvement in the formal, as well as in the informal meetings and activities, is the key ingredient for maximizing the value of the workshop for you and your fellow attendees.

ARRANGEMENTS INFORMATION

AIR TRAVEL GROUP RATES: The IEEE/EDS has arranged for Group rates with **United Airlines**: 5% off the lowest available fare. Call 1-800-521-4041 to check restrictions and fares. Provide United with the Meeting ID Number: 524XA.

TRANSPORTATION NOTE: The Stanford Sierra Camp is located on Fallen Leaf Lake, a few miles from South Lake Tahoe. The nearest major airport is the Reno International Airport. Reno is approximately two hours from Stanford Sierra Camp. Currently no commercial flights are available to the South Lake Tahoe Airport.

- Transportation is available from Reno International Airport to the South Lake Tahoe terminus at Horizons Casino via the ***Tahoe Casino Express***. For ***Tahoe Casino Express*** schedule details see back of registration form or call 800-446-6128.

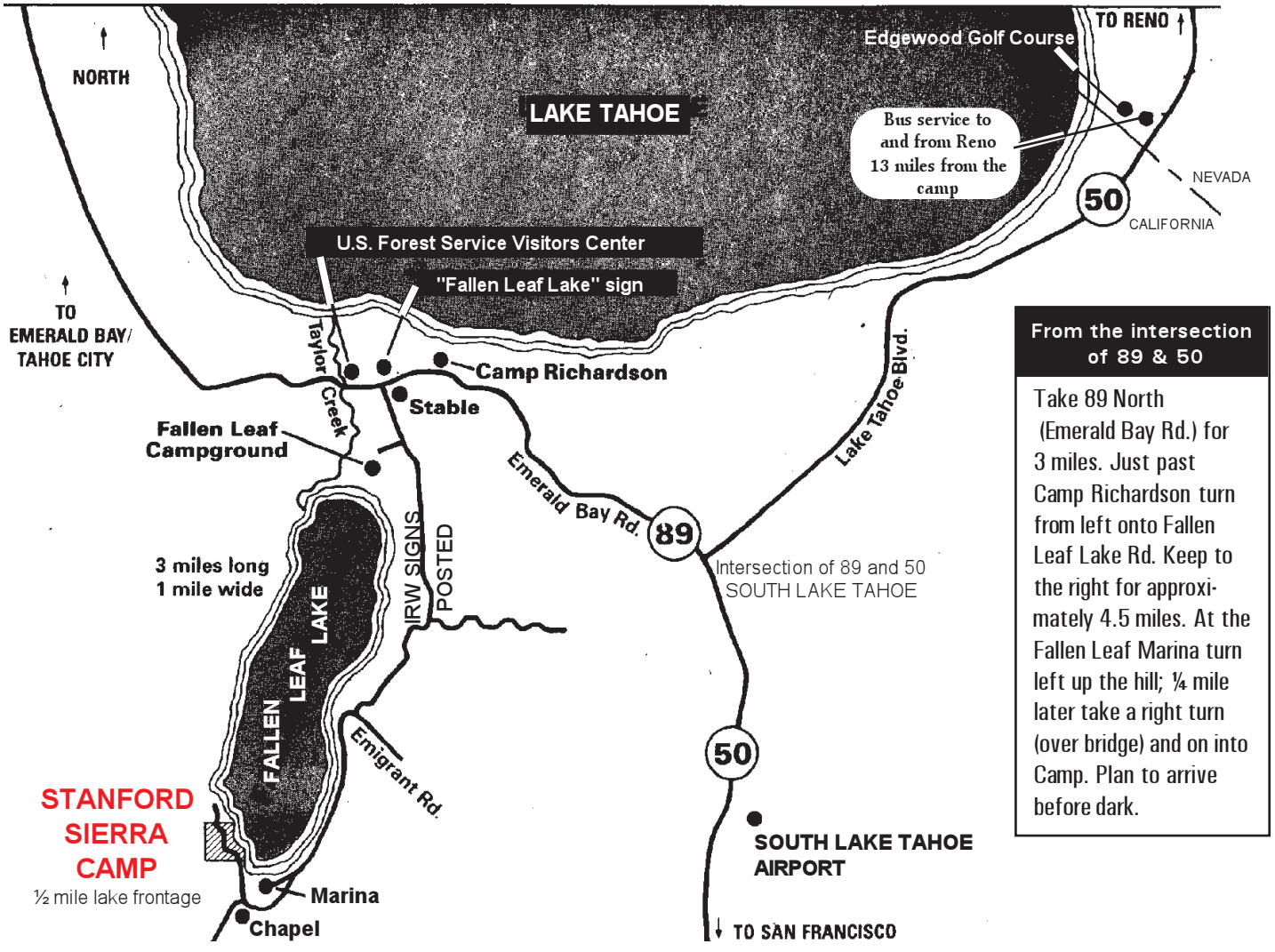
ACCOMMODATIONS

The Stanford Sierra Camp provides an ideal setting for the workshop. The isolated location and the absence of distractions, such as in-room phones and television sets, encourages extensive interaction among the Workshop attendees. Clusters of 2 and 3 bedroom cabins are nestled throughout the pines and cedars along the shoreline of Fallen Leaf Lake. Please note; while each attendee is assigned a bedroom, bathroom facilities within each cabin are shared. All rooms have decks with magnificent views of Fallen Leaf Lake and surrounding Sierra peaks.

- **All participants must stay at the camp during the workshop.**
- **We cannot accommodate spouses or any companions at the camp.**
- **Accommodations are *not* available at the Stanford Camp for any day before or after the workshop.**
- Smoking is permitted outdoors only. Smoking will not be permitted in the sleeping or meeting rooms.
- Arrangements can be made for those with special dietary or physical requirements. Please send your requirements with the registration or call 315-339-3968.
- A message board will be available for incoming calls, (530) 541-1244. There are pay telephones for outgoing calls. There are no telephones in the rooms.

WHAT TO BRING

It may be cold or warm at 6000 feet in the Sierra in October. We recommend that you bring warm clothing and a coat. Comfortable, informal dress is encouraged. No suits, ties, or high heels please. You may want to bring hiking shoes. There are numerous outstanding hiking trails around the camp. A small flashlight would be helpful to find your cabin after dark.



From the intersection of 89 & 50

Take 89 North (Emerald Bay Rd.) for 3 miles. Just past Camp Richardson turn from left onto Fallen Leaf Lake Rd. Keep to the right for approximately 4.5 miles. At the Fallen Leaf Marina turn left up the hill; ¼ mile later take a right turn (over bridge) and on into Camp. Plan to arrive before dark.