1997 International

INTEGRATED RELIABILITY WORKSHOP

October 13-16, 1997

http://www.irps.org/irw/

Stanford Sierra Camp, S. Lake Tahoe, CA

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PROGRAM ANNOUNCEMENT!

WORKSHOP EXPERIENCE

You are cordially invited to participate in the 1997 Integrated Reliability Workshop. The Workshop provides a unique forum for sharing new approaches to achieve and maintain microelectronic component reliability. The Workshop features presentations, tutorials, open poster sessions, moderated discussion group sessions, and special interest group (SIG) meetings. All Workshop activities take place in a relaxed and rustic setting that promotes an atmosphere of interactive learningand knowledge sharing.

MAJOR TECHNICAL THEMES

As silicon technology continues aggressively to scale into the deep submicron regime, physical models for reliability need to be continually revised and expanded to include more complex device and materials behavior. Reflecting this need, the Contributors to Failure session includes several papers on thin oxide reliability modeling. The Reliability Test Structures session complements this focus with papers on area effect and antenna damage monitoring structures. Designing-in Reliability is a methodology that is being incorporated at earlier stages of the process development cycle. The balancing of technology requirements requires simultaneous assessment of device reliability and performance. This task is made easier with the help of modeling tools. The tools of Wafer Level Reliability continue to be crucial to the task of technology reliability development and monitoring. Techniques are constantly refined to meet the ever-changing behavior and test requirements.

- **Contributors to Failure** — failure mechanisms & reliability models (existing, new, anticipated); sensitivities to device geometry, materials, and manufacturing.
- **Reliability Test Structures** — design, characterization, uses and data analysis; integrated on-chip reliability test systems.
- **Designing-in Reliability (circuits, processes, products)** — methodologies and concepts, modeling, simulation tools, reliability-driven design rules and checkers.
- **Wafer Level Reliability** — test and analysis methodologies; in-line monitors; relation to circuit element and package tests; use and interpretation of WLR data; success stories.

'97 Workshop Features:

- ✶ 22+ Technical Presentations on:
  - Contributors to Failure
  - Reliability Test Structures
  - Designing In Reliability
  - Wafer Level Reliability
- ✶ Keynote Address: **Benchmarking Semiconductor Manufacturing**
  Professor David Hodges
  EECS Department
  University of California, Berkeley
- ✶ Tutorials
  - Physical Parameters & Reliability of Ultra Thin Oxides
  - Device Design Methodology & Reliability Strategy for Deep Subμm
- ✶ Group Discussions
  - Designing In Reliability
  - Wafer Level Reliability
  - Customer Reliability Requirements
  - Reliability Test Structures
- ✶ Open Poster Sessions
- ✶ Special Interest Groups

IEEE/Integrated Reliability Workshop
P.O. Box 308
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KEYNOTE: BENCHMARKING SEMICONDUCTOR MANUFACTURING

Professor David A. Hodges
University of California, Berkeley

Professor David Hodges is co-director of the Competitive Semiconductor Manufacturing Program at UC Berkeley. The CSM program brings together faculty and students from Berkeley's College of Engineering, Haas School of Business, and Department of Economics in a continuing program addressing key aspects of semiconductor manufacturing. The program has several elements:

- Comparative studies of the world's best semiconductor plants to identify world-class managerial, organizational, technical, and human resource practices.
- Specific research projects focused on improving key semiconductor manufacturing processes and related business and management practices.
- A dissemination program that has produced 33 research reports, a similar number of conference presentations and archival publications, and three professional short courses targeted at managers and engineers in the semiconductor industry.

The goal of the main comparative study, begun in 1992, is to develop a systematic account of the practices which explain best manufacturing performance in semiconductor production on a world-wide basis. The effort has established comparative benchmarks and performed comparative evaluation along dimensions of technology, business practices, and business environment.

DISCUSSION GROUPS

A highlight of the Workshop is the evening discussion group program. Attendees will have a choice of four topics on both Tuesday and Wednesday evenings. The same four topics will be discussed for 90 minutes each night. This year's topics are:

DESIGNING IN RELIABILITY

Leaders: Mark Poulter, National Semiconductor and Riko Radojcic, Cadence, Angora Room

The motto is: Process Qualification without Product Qualification. The traditional method of qualifying a new process comes late in the development cycle. It is achieved by running qualification on a few lots of a product which exercises the main features of the process. If there are failures, much time and money is wasted in implementing process improvements and performing requalification. In the constant push to reduce development cycle times, methods must be implemented to start qualification of the process well in advance of any product. Identifying and fixing reliability problems early avoids the need for costly requalification and the unacceptable delays it incurs.

In this discussion group we will consider how to perform process qualification without product qualification by asking:

- What needs to be done to ensure reliability?
- How do we sell this idea to our customers?
- What kinds of test structures are required?
- Design *degrees of freedom* to manage product reliability (i.e. what can be adjusted in the design to manage product reliability)
- Requirements to create a *standard* interface to process reliability (i.e. what information is required from the process arena to enable the design adjustments)
- Examples of specific experiences of design reliability

WAFER LEVEL RELIABILITY

Leader: Cleston Messick, National Semiconductor and Sally Yankee, IBM, Cathedral Room

The idea of Wafer Level Reliability (WLR) first appeared in the early 80's. After much discussion and many programs, the definition of WLR still eludes consensus. During this discussion session, several definitions will be presented and discussed. Attendees are invited to bring their own definitions and examples of successful implementations and/or examples of failures in implementation. The participants will gain a greater appreciation for the abilities and limitations of WLR along with a concrete understanding of the definition of WLR.

CUSTOMER RELIABILITY REQUIREMENTS

Leaders: Andreas Preussger, Siemens and Ian Wylie, Northern Telecom, Tallac Room

Suggested topics for discussion:

- Reliability evaluation methodologies:
  + What is needed to be preventive enough?
  + Can reliability investigations on test structures replace expensive and time consuming life tests?
- How can we prove reliability targets of 10 FIT and lower?
- Is BIR and DIR the accepted way to guarantee the required reliability?
- What type of reporting system is needed to prove the reliability of a production line?
- What are the future reliability targets: at the time of the qualification and during production?

RELIABILITY TEST STRUCTURES

Leaders: Tim Turner, Keithley Instruments and Jim Lloyd, Lloyd Technologies, Old Lodge

Test structures for reliability evaluations are taking an increasingly important position in reliability assurance programs for semiconductor products. The design of these test structures is not a trivial task. While the structures are generally fairly basic circuit elements, the restrictions imposed by anomalous failure mechanisms and stress limitations require a very detailed knowledge of the failure mechanism to be studied and the process used to build these structures. A few potential discussion topics associated with the use of these test structures are listed below.

- Process reliability control structures vs. lifetime prediction structures and test techniques.
- Test structure standardization
- Defect density vs. worst case structure design techniques
- Addressable test structures for silicon area reduction

TUTORIALS

In our continuing effort to enhance the value of the Workshop and to strengthen the Technical Program, we are again offering two tutorials on Monday afternoon.

Tutorial A: **DETERMINATION OF PHYSICAL PARAMETERS AND RELIABILITY OF ULTRA THIN GATE OXIDES**—E. Cartier, IBM Research Division, T.J. Watson Research Center, Yorktown Heights, NY

The aggressive down scaling of the device dimensions in CMOS technology will require the fabrication of gate oxides with thickness in the range of 2-3 nm in the near future and the fabrication of oxides with an equivalent thickness of less than 2 nm will eventually be required. To characterize such thin oxides, well established techniques may no longer provide accurate results or can not be used at all. In this tutorial, some issues related to the characterization of very thin oxides will be addressed.

Tutorial B: **DEVICE DESIGN METHODOLOGY AND RELIABILITY STRATEGY FOR DEEP SUBMICRON TECHNOLOGY—** Rama Divakaruni, Badih El-Kareh*, and William Tonti, IBM Microelectronics and *IBM Strategic Technologies

This tutorial will discuss device and process optimization techniques that may be employed in the design of present state of the art bulk Si DRAM technology. MOSFET performance and reliability issues are contrasted.

The topical issues to be discussed include:

- Time zero constraints for I_{on} and I_{off} considerations.
- A self consistent methodology for substrate hot carrier immunity.
- The hot carrier effects of box type isolation.
- Wafer level burn-in considerations.
- Module level burn-in and examples.

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(continued from page 2)

Open Poster Sessions

The Technical Program will include two open poster sessions. *All attendees have the opportunity to present a poster to communicate their ideas and results on a technical project or issue.* Please indicate your intention to bring a poster by reserving a poster display board (32" × 40" or 81 cm × 100 cm) in the space provided on the registration form. Your work should be in Landscape format on 8½ × 11" or A4 paper with a maximum of twelve pages. In addition, you are invited to submit a two-page abstract of your poster presentation for inclusion in the Workshop Final Report. This is a great opportunity for you to share your work with your peers.

Special Interest Groups (SIG)

The SIG program at the Workshop has been very successful in fostering collaborative work on important reliability issues and we look forward to continuing growth and renewal in our SIGs. The formation of SIGs is encouraged as a natural extension of the Discussion Group sessions. Anyone interested in more information about SIGs is encouraged to contact the 1997 SIG Coordinator, Jiang Tao at jtao@grape.amd.com.

JEDEC 14.2 Meeting

The JEDEC 14.2, Wafer Level Reliability Standards Committee, meeting will be held immediately after the Workshop at the Stanford Sierra Camp on Thursday afternoon and Friday morning. Members, alternates, and guests are welcome. The cost for the accommodations is $160.00, which includes Thursday night dinner and lodging *and* Friday breakfast and lunch. All attendees must leave the camp after lunch on Friday. If you have any questions or if you want to become a member of JC-14.2, please call the JEDEC office at (703) 907-7558 or call Mike Dion, JC-14.2 Chair, at (704) 724-7067.

More Information

We expect an exciting workshop again this year. We look forward to your active participation in the many Workshop activities and your valuable contribution to the technical program. If you have any questions, please contact the Technical Program Chair, Raif S. Hijab, by phone, 408-749-2250, or fax, ...5585, or e-mail: raif.hijab@amd.com, or the General Chair, James W. Miller, at 512-933-7297, fax...7662, email: rvkg60@email.sps.mot.com

REGISTER NOW!

Complete and mail the enclosed registration form. Please register early. We were nearly sold out last year. Space at the Camp limits the Workshop to roughly 120 attendees.

We look forward to seeing you at the '97 Workshop!

Sincerely,
Raif S. Hijab
Technical Program Chair

Tahoe Casino Express

The Tahoe Casino Express runs from Reno to Tahoe between 6 a.m. and midnight with departures from Reno at: 6:15 a.m., 8:15, 9:15, 10:15, 11:15, 12:15 p.m., 1:15, 2:15, 3:15, 5:30, 7:30, 9:30, 10:30 and 12:30 a.m.. The Express costs $17 each way ($30 round trip) and tickets can be purchased at the Express counter located in the baggage area in the Reno airport. Travel time is approximately 1½ hours. The Casino Express can be reached at 800-446-6128.

The Express leaves the Horizon Casino at Lake Tahoe and returns to Reno on the following schedule: 4:10 a.m., 6:10, 8:10, 9:10, 10:10, 11:10, 12:10 p.m., 1:10, 2:10, 3:10, 4:10, 5:10, 7:25, and 10:25 p.m. Tickets may be purchased in the Horizon Casino at the main cashier's cage.

Stanford Sierra Camp offers courtesy transportation for conference attendees from the Horizon Casino between 10 a.m. and 10 p.m. on Registration Day (Monday, Oct. 13). Return trips to the Casino are offered on the last day of the conference only. If you are planning on using the Casino Express, please notify Stanford Sierra Camp (916-541-1244) at least ONE WEEK prior to your arrival date. The IRW is offering emergency service to and from the casino. If you find yourself stranded, please call the camp at the same number.

1997 *International* INTEGRATED RELIABILITY WORKSHOP

PRELIMINARY PROGRAM

MONDAY, October 13

1:00–8:00 p.m.	Lodge check-in. Get room assignment (preassigned) & room key, with lodge area map and information. (ADA please notify desk of special needs)
1:00–2:30 p.m.	Registration: Pick up badges & handout (*Dining Room Lounge*) Sign up for Discussion Groups and SIG meeting
2:30–4:30 p.m.	Tutorial Sessions Tutorial A: Determination of Physical Parameters and Reliability of Ultra Thin Oxides— E. Cartier, IBM, Yorktown Heights, NY *Angora Room* Tutorial B: Device Design Methodology and Reliability Strategy for Deep Submicron Technology—Rama Divakaruni, Badih El Kareh*, and William R. Tonti, IBM Microelectronics and *IBM Strategic Technologies, *Cathedral Room*
4:30–6:00 p.m.	Registration: Pick up badges & handout (*Dining Room Lounge*) Sign up for Discussion Groups and SIG meeting
5:00–6:00 p.m.	Mixer & Poster Session, *Cathedral Room*
6:00–7:30 p.m.	DINNER, *Dining Room*
7:00–7:30 p.m.	Registration for late arrivals (*Dining Room Lounge*)
7:30–8:30 p.m.	Mixer & Poster Session, *Cathedral Room*
8:30–9:30 p.m.	SIG Meeting (all SIGs), *Angora Room*

TUESDAY, October 14

7:00 a.m.	BREAKFAST (until 8:00 a.m.)
8:15–8:30 a.m.	Welcome & Introduction: James W. Miller, General Chair, and Raif S. Hijab, Technical Program Chair, *Angora Room*
8:30–9:45 a.m.	Keynote: Benchmarking Semiconductor Manufacturing—Professor David Hodges, EECS Dept, University of California, Berkeley
9:45–10:15 a.m.	Break
10:15–11:30 a.m.	Session #1: Contributors to Failure (CTF), Paula O'Sullivan, NMRC, Chair, Harry Schafft, NIST, Vice Chair CTF-1 Resistance Transients in Thin-film Noise Data—Linda M. Head, SUNY at Binghamton CTF-2 Plasma-Induced Polarity Dependent Hot-Carrier Response of CMOS Devices Across a Wafer—B. Bhuva, V. Janapaty and S. Kerns, Vanderbilt University and Nguyen Bui, Advanced Micro Devices CTF-3 Acceleration Factors of PMOS Hot-Carrier Degradation—Hisao Katto, Science University of Tokyo
11:30 a.m.–noon.	Group Picture
noon–1:30 p.m.	LUNCH, *Dining Room*
2:00–3:15 p.m.	Session #2: Reliability Test Structures (RTS), Brian Langley, Hewlett-Packard, Chair RTS-1 Investigation of the Intrinsic SiO_2 Area Dependence using TDDB Testing—J. Prendergast, Nuala Finucane, Analog Devices, and John Suehle, NIST RTS-2 Antenna Damage from a Plasma TEOS Deposition Reactor: Relationship with Surface Charge and RF Sensor Measurements—Indira J. Gupta, Kelly Taylor, Dave Buck and Srikanth Krishnan, Texas Instruments RTS-3 Optimized Application of Antenna Structures in a WLR Monitoring Program—W. Asam, J. Fazekas and J. von Hagen, Siemens AG
3:15–3:45 p.m.	Break
3:45–5:00 p.m.	Session #3: Designing In Reliability (DIR), Bill Vigrass, Texas Instruments, Chair, Homi Nariman, AMD, Vice Chair DIR-1 CMOS Transistor Reliability and Performance Impacted by Gate Microstructure—Bin Yu, Dong-Huyk Ju*, Nick Kepler*, Tsu-Jae King, and Chenming Hu, University of California, Berkeley *Advanced Micro Devices DIR-2 Designing-in Device Reliability during the Development of High-Performance CMOS Logic Technology from 0.5 µm to 0.13 µm—Deepak K. Nayak, Ming-Yin Hao, and Raif Hijab, Advanced Micro Devices DIR-3 HCI Lifetime Enhancement by Double Implanted S/D of Nch MOSFET in 0.25 µm CMOS Technology—David Wu, Scott Luning, D. H. Ju, and Nick Kepler, Advanced Micro Devices
5:00–6:00 p.m.	Mixer & Poster Session
6:00–7:30 p.m.	DINNER, *Dining Room*
7:30–9:00 p.m.	Discussion Groups (90 minute parallel sessions for each topic) Attendees are to participate in one of the four groups
9:00–10:30 p.m.	Individual SIG Meetings

WEDNESDAY, October 15

7:00 a.m.	BREAKFAST (until 8:00 a.m.)
8:15–8:30 a.m.	Announcements, *Angora Room*
8:30–10:10 a.m.	Session #4: Contributors to Failure (CTF) CTF-4 Effect of Electronic Corrections on the Thickness Dependence of Thin Oxide Reliability—G. B. Alers, A.S. Oates, B. E. Weir, D. Monroe, and K. S. Krisch, Bell Labs, Lucent Technologies CTF-5 The Non-uniqueness of Breakdown Distributions in Silicon Oxides—J. C. Jackson, T. Robinson, O. Oralkan, D.J. Dumin, Clemson University and G. A. Brown, Texas Instruments CTF-6 Temperature Dependence of Gate Current in Ultra Thin SiO_2 in Direct-Tunneling Regime—A. Yassine and Raif Hijab, Advanced Micro Devices CTF-7 Charge-to-Breakdown and Trap Generation Process in Thin Oxides—Gennadi Bersuker, James Werking, and Sang Kim, SEMATECH
10:10–10:30 a.m.	Break
10:30 a.m.–12:10 p.m.	Session #5: Wafer Level Reliability (WLR), Prasad Chaparala, National Semiconductor, Chair, Sharad Prasad, LSI Logic, Vice Chair WLR-1 A New Technique to Extract TDDB Acceleration Parameters from Fast Qbd Tests—Y. Chen, John S. Suehle*, Bruce Shen, Joseph Bernstein, and Cleston Messick**, University of Maryland *NIST ** National Semiconductor WLR-2 Correlation of Charge to Breakdown Obtained from Constant Current Stresses and Ramped Current Stresses, and the Implications for Ultra-Thin Gate Oxides—Nels Dumin, Texas Instruments

	WLR-3	A Candid Comparison of the SWEAT Technique and the Conventional Test Procedure for Electromigration Study in Sub-Half Micron ULSI Interconnects—Satish S. Menon and Ratan K. Choudhury, LSI Logic
	WLR-4	High Resolution Electromigration Measurements for Reduction of the Test Time—Catherine de Keukeleire and Piet De Pauw, ALCATEL MIETEC and Luc Tielemans, DESTIN N.V.
12:15–1:30 p.m.	LUNCH, *Dining Room* (Take out Lunch bags available) The afternoon is free for discussion, hiking and other recreation	
1:30–6:00 p.m.	Open	
6:00–7:30 p.m.	DINNER, *Dining Room*	
7:30–9:00 p.m.	Discussion Groups (90 minute parallel sessions for each topic) Attendees are to participate in one of the four groups	
9:00–10:30 p.m.	Individual SIG Meetings	

THURSDAY, October 16

7:00 a.m.	BREAKFAST (until 8:00 a.m.)	
8:15–8:30 a.m.	Announcements, *Angora Room*	
8:30–10:10 a.m.	Session #6: Wafer Level Reliability	
	WLR-5	A Novel In-process Wafer-Level Screening Technique for CMOS Devices—I. Yoshii, H Hazama, H. Kamijo, Y. Ozawa, and K. Hama, Toshiba Corp.
	WLR-6	Pulsed BTS - an Accurate and Fast Technique to Determine Mobile Ion Concentrations and Kinetics in Gate and Field Oxides—Laszlo Gutai, Philips Electronics North American
	WLR-7	Charge Pumping for DRAM Retention Diagnostics—Rama Divakaruni and Jim Adkisson, IBM Microelectronics
9:45–10:00 a.m.	Break (checkout at this time if not staying for JEDEC meeting)	
10:00–10:50 a.m.	Session #7: Design-In Reliability	
	DIR-4	Automated Extraction of Parasitic BJTs for CMOS I/O Circuits Under ESD Stress—Tong Li, Y. J. Huh, and S. M. Kang, University of Illinois at Urbana-Champaign
	DIR-5	Evolution of BSIM3v3 Parameters During Hot-Carrier Stress—Sean Minehane, Paula O'Sullivan, Alan Mathewson, and Barry Mason*, National Microelectronics Research Centre (NMRC), and *GEC Plessey Semiconductors
10:50–11:05 a.m.	SIG Report	
11:05–11:35 a.m.	Discussion Group Summaries	
11:35 a.m. - noon	Wrap-Up	
noon–1:30 p.m.	LUNCH, *Dining Room* Workshop Ends—Leave the Stanford Sierra Camp unless attending JC14.2	
2:00 p.m.	JEDEC 14.2 Committee on Wafer Level Reliability Meeting	

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1997 IRW REGISTRATION FORM (Use also for reserving accommodations to EIA/JEDEC Committee JC14.2 meeting, Oct. 16-17)

(Please type, print clearly, or attach business card)

NAME: ______________ (Last / First / Initial) TITLE: ______________

COMPANY: ______________ (Mail Code)

ADDRESS: ______________

______________ (City / State/Country / Zip/Postal Code)

PHONE: (______) ______________ FAX: ______________

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❍ Address is HOME, Company not to be included on mailing label

❍ Please check here if you do not wish to receive mail other than from IRW & IRPS

❍ Please check here if under the Americans With Disabilities Act, you require any auxiliary aids or service. Please call (315) 339-3971.

For rooming assignments, please check one: male ❍ female ❍

REGISTRATION FEES (US$)

IEEE Member ________ ... **$900*** ________
(member No. Req'd)

NON-IEEE Member.................. **$950*** ________

** Includes meals, lodging, Handout, & Final Report. (Mon. eve., Oct. 13- Thur. noon, Oct. 16)*

EXTRA COPIES of Workshop Final Report ...... Qty: ______ x **$80** ________

JC14.2 accommodations .... **$160†** ________

TOTAL REMITTED $ ________

Meeting registration automatically includes a room reservation.

SORRY, WE DO NOT TAKE CREDIT CARDS

☐ MAKE CHECKS PAYABLE TO **"IEEE INTEGRATED RELIABILITY WORKSHOP"**

☐ **Wire Transfer:** Marine Midland Bank, 853 Black River Blvd., Rome, NY 13440; Acct. name: IEEE/IRW 1997; Acct. #: 192456083; ABA #: 021001088

Each Attendee will only attend one Discussion Group each night. Please Indicate your Discussion Group Preference

Tues	Wed	Discussion Group Topic
		Designing In Reliability
		Wafer Level Reliability
		Customer Reliability Requirements
		Reliability Test Structures

SEND PAYMENT & FORM TO:

IEEE IRW
P.O. Box 308
Westmoreland, NY 13490

For registration information:
phone: 315-339-3971
FAX: 315-336-9134
email: sar@ntcnet.com
http://www.irps.org/irw

❍ WILL ❍ WILL NOT ATTEND MONDAY TUTORIALS (3-5 p.m.). If you plan to attend, please indicate preference for topic below:

❍ **Phys. Parameters/Reliability of Ultra Thin Oxides** ❍ **Device Design Methodology & Reliability Strategy for Deep Submicron**

YOUR POSTER TITLE: ______________

You will be provided with a poster board for one of the poster sessions to share your ideas and your results on a technical topic or issue. Instructions will be sent to you if you register for a poster. You will be provided with a 32" x 40" poster board.

**The Workshop Registration Fee includes: your housing accommodations at the Stanford Sierra Camp cabins, all meals and refreshments (no-host bar), on-site recreation activities, parking for your car, the Presentation Viewgraph Booklet (at the workshop), and the Final Report (after the workshop).*

† The JEDEC Committee fee for accommodatons includes: housing on Thursday night, meals (from dinner on Thursday through buffet lunch on Friday), refreshments, and parking for your car.

CANCELLATION fees: $50 AFTER SEPTEMBER 19; FULL FEE AFTER OCTOBER 3

RESPONSIBILITIES OF ATTENDEES

You are expected to come prepared to participate actively in the discussions and meetings by sharing your experiences, concerns, questions, views, technical information, and test data, as appropriate. Your active involvement in the formal, as well as in the informal meetings and activities, is the key ingredient for maximizing the value of the workshop for you and your fellow attendees.

ARRANGEMENTS INFORMATION

AIR TRAVEL GROUP RATES: The IEEE/EDS has arranged for Group rates with **United Airlines**: 5% off the lowest available fare. Call 1-800-521-4041 to check restrictions and fares. Provide United with the Meeting ID Number: 500BX.

TRANSPORTATION NOTE: The Stanford Sierra Camp is located on Fallen Leaf Lake, a few miles from South Lake Tahoe. The nearest major airport is the Reno International Airport. Reno is approximately two hours from Stanford Sierra Camp. Currently no commercial flights are available to the South Lake Tahoe Airport.

- Transportation is available from Reno International Airport to the South Lake Tahoe terminus at Horizons Casino via the ***Tahoe Casino Express***. For ***Tahoe Casino Express*** schedule details see the other side of this page.

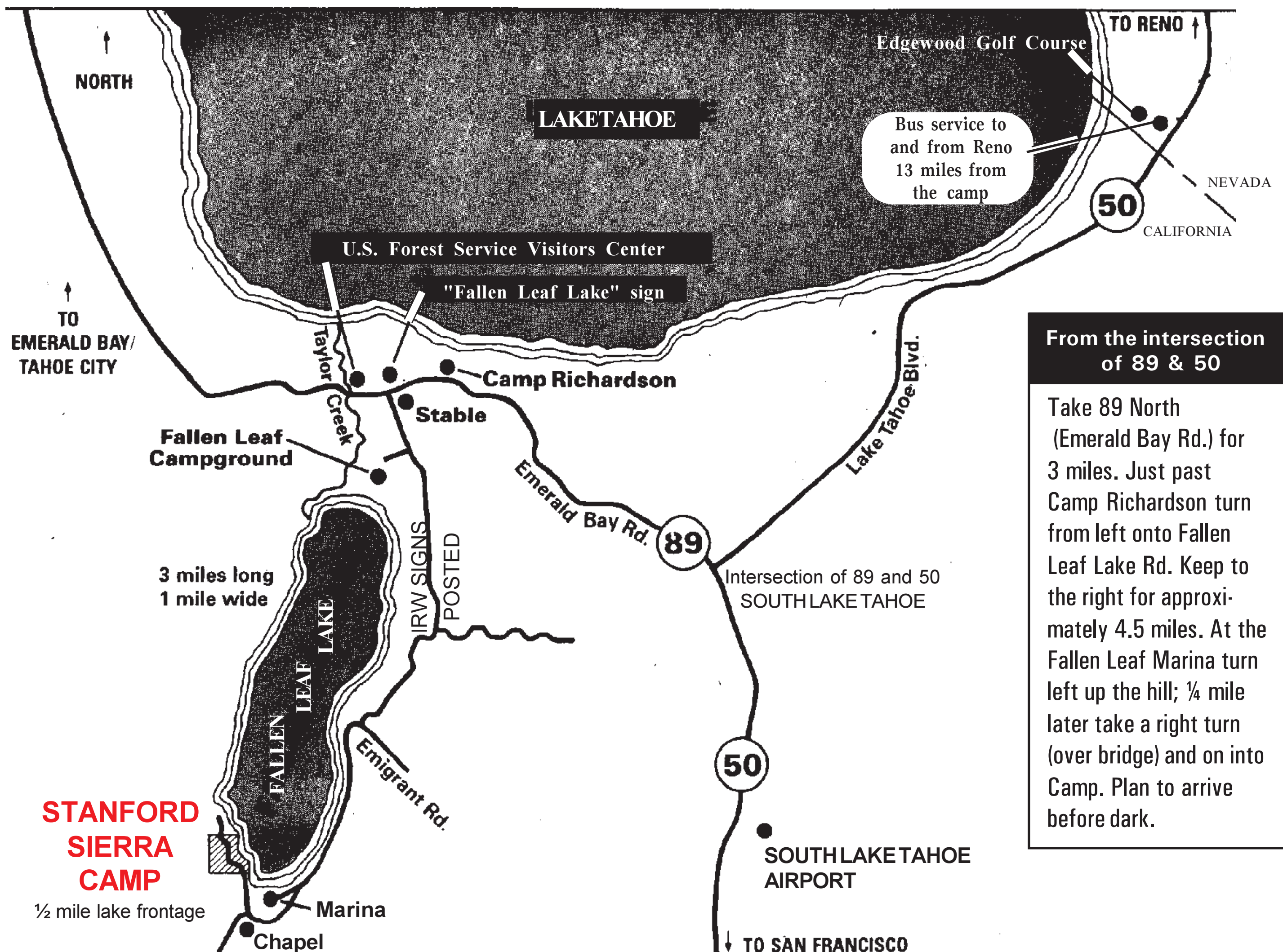
ACCOMMODATIONS

The Stanford Sierra Camp provides an ideal setting for the workshop. The isolated location and the absence of distractions, such as in-room phones and television sets, encourages extensive interaction among the Workshop attendees. Clusters of 2 and 3 bedroom cabins are nestled throughout the pines and cedars along the shoreline of Fallen Leaf Lake. Please note; while each attendee is assigned a bedroom, bathroom facilities within each cabin are shared. All rooms have decks with magnificent views of Fallen Leaf Lake and surrounding Sierra peaks.

- **All participants must stay at the camp during the workshop.**
- **We cannot accommodate spouses or any companions at the camp**.
- **Accommodations are *not* available at the Stanford Camp for any day before or after the workshop.**
- Smoking is permitted outdoors only. Smoking will not be permitted in the sleeping or meeting rooms.
- Arrangements can be made for those with special dietary or physical requirements. Please send your requirements with the registration or call 315-339-3971.
- A message board will be available for incoming calls, (916) 541-1244. There are pay telephones for outgoing calls. There are no telephones in the rooms.

WHAT TO BRING

It may be cold or warm at 6000 feet in the Sierra in October. We recommend that you bring warm clothing and a coat. Comfortable, informal dress is encouraged. No suits, ties, or high heels please. You may want to bring hiking shoes. There are numerous outstanding hiking trails around the camp. A small flashlight would be helpful to find your cabin after dark.



From the intersection of 89 & 50

Take 89 North (Emerald Bay Rd.) for 3 miles. Just past Camp Richardson turn from left onto Fallen Leaf Lake Rd. Keep to the right for approximately 4.5 miles. At the Fallen Leaf Marina turn left up the hill; ¼ mile later take a right turn (over bridge) and on into Camp. Plan to arrive before dark.