



2000 *International*

# INTEGRATED RELIABILITY WORKSHOP



**October 23-26, 2000**

<http://www.irps.org/irw/>

**Stanford Sierra Camp, Lake Tahoe, CA**

## CALL FOR PAPERS

The Integrated Reliability Workshop continues to focus on ensuring semiconductor reliability through component fabrication, design, characterization, and analysis tools. It provides a unique environment for envisioning, developing, and sharing reliability technology for present and future semiconductor applications.

Hot reliability topics of the workshop are: Cu interconnects, reliability of deep sub-micron, high speed, high frequency devices (e.g. SiGe), SOI devices, new dielectric systems, and reliability modeling & simulation.

We invite you to submit a presentation proposal that addresses one or more of the following topics:

- **WAFER LEVEL RELIABILITY TESTS AND TEST APPROACHES:**  
*fast stress tests and analysis methodologies, reduction in development time, in-line monitors, relation to circuit-element and package-level tests, use and interpretation of WLR data; success stories; the fine tuning of a WLR implementation.*
- **IDENTIFICATION OF RELIABILITY EFFECTS:**  
*failure mechanisms and sensitivities to materials and manufacturing; new reliability aspects of: novel dielectric systems, Cu interconnects, MOS and bipolar transistors.*
- **NEW OR EXISTING RELIABILITY CHARACTERIZATION AND PREDICTION MODELS TO SHOW:**  
*limits to accelerated stress, (non-) correlation of short- and long-duration stress results, applications for AC, pulsed, and DC conditions.*
- **RELIABILITY TEST STRUCTURES:**  
*design, characterization, uses, and data analysis; for chip or package level (including electrical and/or physical test/analysis).*
- **CUSTOMER PRODUCT RELIABILITY REQUIREMENTS/ MANUFACTURER RELIABILITY TASKS:**  
*limits to achieve future reliability targets, reliability evaluation methodologies; reporting systems; data bases.*
- **DESIGNING-IN RELIABILITY (CIRCUITS, PROCESSES, PRODUCTS):**  
*methodologies and concepts, modeling, simulation tools, reliability-driven design rules and checkers; use of WLR for design rule verification.*

**SUBMISSION DEADLINE: *Received no later than July 7, 2000.***

Your submission should state clearly and concisely the results of your work and why they are significant. Representative data and/or figures that support your proposal are REQUIRED. This year we are accepting both paper and poster submissions. Please state which submission category you prefer.

Preferably, please e-mail your maximum two-page abstract (incl. figures) or airmail (express mail preferred) it with 15 copies to either the Technical Program Chair or the Vice Technical Program Chair. If you send the proposal by e-mail, please send it as a MS Word document or pdf file. Your proposal must include the name, affiliation, complete return address, telephone and telefax numbers, and e-mail address for each author. Telefax submissions will NOT be accepted. All submissions will be acknowledged within three weeks. If you do not receive acknowledgment of your submission, please contact the Technical Program Chair.

Visual aids for the ACCEPTED paper proposals are required by September 8, 2000 for inclusion in the Presentation Handout available at the workshop. A written version of your presentation is due at the workshop for inclusion in the Final Report.

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## 2000 IRW ADVANCE REGISTRATION • October 23–26, 2000 • Stanford Sierra Lodge

Advance Registration should be made well before September 2000 to insure your space at the Workshop.

THE WORKSHOP HAS LIMITED SPACE (for approx. 140 attendees) and YOU ARE ENCOURAGED TO REGISTER EARLY.

The Registration fee is US\$925 for IEEE Members and US\$975 for non-members, which includes: meals, lodging, and refreshments at the Stanford Sierra Camp; Presentation View Graphs (provided at the Meeting); and the 2000 IRW Final Report (published after the Meeting).

### LODGING & FACILITIES

Nestled throughout the pines and cedars along the shoreline of Fallen Leaf Lake, a few miles from South Lake Tahoe, are clusters of 2 and 3 bedroom cabins furnished in the rustic style of an alpine resort. Each cabin cluster is equipped with shared bathroom facilities. All rooms have decks with magnificent views of Fallen Leaf Lake and surrounding Sierra peaks.

The physical isolation of the location and the absence of distractions, such as in-room phones and television sets, encourages extensive interaction among the Workshop attendees.

*Lodging is available for meeting attendees only.*

### JEDEC JC-14.2 MEETING

The JEDEC JC-14.2 Committee on Wafer Level Reliability meeting will be held immediately after the Workshop at the Stanford Sierra Camp on Thursday afternoon and Friday morning. Members, alternates, and guests are welcome. The cost for the accommodations is US \$160.00, which includes Thursday night dinner and lodging and Friday breakfast and lunch. All attendees must leave the camp after lunch on Friday. If you have any questions, please call Michael Dion at (407) 724-7067. If you want to become a member of JC-14.2, please call the JEDEC office at (703) 907-7558.

## INTEGRATED RELIABILITY WORKSHOP ADVANCE REGISTRATION FORM

(Please type, print or attach business card)

Meeting registration automatically includes a room reservation.

### ADVANCE REGISTRATION FEES

NAME: \_\_\_\_\_ TITLE: \_\_\_\_\_  
Last First Initial

COMPANY: \_\_\_\_\_ Mail Stop

ADDRESS: \_\_\_\_\_

City State/Country Zip/Postal Code

Phone: ( \_\_\_\_\_ ) \_\_\_\_\_ Fax: \_\_\_\_\_

Email: \_\_\_\_\_

☐ Address is HOME

☐ Please check here if you do not wish to receive mail other than from IRW & IRPS

☐ Please check here if physically challenged and you require any auxiliary aids or services. Please call (315) 339-3968.

For cabin assignments: ☐ male ☐ female

Method of Payment:

☐ Check: Make checks payable to: **2000 IEEE/IRW**

☐ Credit Card: ☐ AMEX ☐ MASTER CARD ☐ VISA ☐ Diners Club

IEEE Member \_\_\_\_\_ **\$925\*** \_\_\_\_\_  
(member No. Req'd)

NON-IEEE Member \_\_\_\_\_ **\$975\*** \_\_\_\_\_

\* Includes meals, lodging, Handout, & Final Report.  
(Mon. eve., Oct. 23–Thur. noon, Oct. 26)

EXTRA COPIES of Workshop

Final Report ..... Qty: \_\_\_\_\_ x **\$80** \_\_\_\_\_

JC-14.2 Mtg. accommodations **\$160** \_\_\_\_\_

**TOTAL REMITTED** \$ \_\_\_\_\_

Cancellation fees: \$50 after Sept. 29; full fee after Oct. 13

Send this completed form and payment to:  
IRW Registration; P.O. Box 308; Westmoreland, NY 13490

Paying by credit card... fax to 315-336-9134;  
Questions? sar@ntcnet.com or 315-339-3968

Card No.

Expiration Date

Signature

### HISTORY

The Wafer Level Reliability Workshop was initiated in 1982 through the efforts of O. D. "Bud" Trapp, of Technology Associates, and the active support and encouragement of DARPA (Defense Advanced Research Projects Agency). This support continued for the first eight years of the Workshop and included active support and involvement of the Stanford University Integrated Circuits Laboratory and the University of California, Berkeley, Dept. of Electrical Engineering and Computer Sciences. After DARPA sponsorship ended, Bud Trapp continued the direction of the Workshop until 1991 after which time he requested that sponsorship and management be assumed by an appropriate professional association. The IEEE accepted this responsibility in 1992. In 1993, the name of the Workshop was changed to the Integrated Reliability Workshop. This change reflects the enlarged scope of the Workshop, the integrated nature of reliability in the manufacture of semiconductor products, and the need for a broader and a more comprehensive approach to reliability engineering.



### SPONSORS

The International Integrated Reliability Workshop is sponsored and managed by the IEEE Electron Device Society and the IEEE Reliability Society through the Board of Directors of the International Reliability Physics Symposium.

<http://www.irps.org/irw>