2003 *INTERNATIONAL RELIABILITY PHYSICS SYMPOSIUM*

March 30–April 3, 2003 ● Hyatt Regency Dallas ● Dallas, Texas

CALL FOR PAPERS and CALL FOR POSTERS

The IRPS promotes the greater understanding of the reliability and performance of integrated circuits and microelectronic assemblies in the user's environment. IRPS accomplishes this by offering its attendees the opportunity to attend technical sessions, tutorials, workshops, and a poster session, all covering state-of-the-art developments in electronic reliability.

YOUR PAPER AND POSTERS ARE SOLICITED DESCRIBING ORIGINAL WORK IN THE FOLLOWING GENERAL CATEGORIES THAT:

A. Identifies new, or improves our understanding of, known mechanisms of failure in electronic and optoelectronic devices and materials;
B. Correlates the influence of fabrication processes with certain failure mechanisms;
C. Presents new, innovative, or improved failure analysis techniques or theoretical modeling and simulation of failure mechanisms;
D. Describes reliability testing, qualification, and screening methodologies for materials, devices, and processes;
E. Quantifies the impact of device and circuit design, material, and process selection on reliability;
F. Demonstrates techniques to build-in or extend reliability while meeting performance goals, especially as technologies are scaled.

For Silicon and Non-Silicon Devices in the following areas:

High-k gate dielectrics, dual gate devices, Low-k and Cu, NBTI, SOI, NVM

PRODUCT

Product Reliability and Burn-in – Case Histories of Product Reliability Issues, Wafer-Level Reliability Issues. New or Novel Failure Modes in Logic/Memory ICs, Burn-In Elimination Strategies, Correlation between Yield, Infant Mortality, Burn-In

Non-Volatile Memory – Unique Reliability Phenomena and Failure Mechanisms in Non-Volatile Memories, Reliability of Ferroelectric or Magnetic Memories

Qualification Strategies – New Techniques for Technology or Process Qualification, Case Histories or Best Practices to Reduce Time-to-Market, Fabless or Foundry Qualification

Circuits – Comprehending Reliability in Designs and Circuits, Soft Error Upsets, Analog Circuit Reliability Issues, Simulation/ Modeling Techniques

Assembly and Packaging – Package/Assembly Reliability, Stress Modeling, Cu and Low-K Issues, Chip Scale Integration, Bump Reliability Issues, Multi-Chip Packaging, Wafer Scale Packaging

Failure Analysis – New Failure Mechanisms and Failure Analysis Techniques, Case Histories

MEMS – Reliability of New Structures, Sensors, Actuators, Reliability Testing and Analysis of MEMS Systems, Design and Processing for Reliability

PROCESS

Device Dielectrics – New or Novel Dielectric Systems Reliability (high-k, dual dielectric), Oxide Breakdown Mechanisms, Processing Interactions, Wearout Models, Gate Dielectric Thickness Scaling

Interconnects – EM Phenomena in Cu and Al Systems, Low-k/Oxide Inter/Intra-Level Reliability, Mechanical Stress Related Reliability Issues, Joule Heating Effects, Modeling Mechanical and Thermal Behavior

Transistor – New Hot Carrier Phenomena, NBTI, Transistor Scaling Issues, Silicon on Insulator (SOI) Reliability Issues, High Performance Transistor Reliability, Issues Related to Back Bias Circuit Operation

Foundry Reliability – Reliability Methodologies at Foundries, Qualification and Process Monitoring Strategies, Case Histories

Process Induced Damage – Reliability Degradation Associated with Process Damage, Early Detection and Reliability Analysis, Correlation to Yield or Accelerated Testing Results

Device and Process – Reliability Driven Process Interactions, New Process-Related Reliability Issues including Si and Non-Si based, OptoElectronics, MEMS, WLR

ESD and Latch-Up – Novel Structures including SOI and Bipolar, Damage Interpretation, Circuit/Process Improvements, Scaling Issues

PAPER AND POSTER SUBMISSION GUIDELINES

Paper Submission: Your work must be original and unpublished. **The deadline for paper submission is October 1, 2002.** ***This year, you can submit a draft paper or an abstract.*** An on-line IRPS document template, located at http://www.irps.org/tpc is available for your use in abstract and paper submission. Using this template will save you time and preparation effort. Draft paper submissions are unrestricted in paper length and may represent the final camera-ready manuscript. Abstract submissions should include enough information to clearly indicate a path to develop the final paper. Whether abstract or paper draft, submission should clearly and concisely state the specific results, why they are important, and how they relate to prior work.

Late Paper Submission: This year, a limited number of late breaking news manuscripts will be considered on a space available basis. Completed camera-ready news manuscripts may be submitted up until December 10, 2002. These manuscripts are to follow the criteria for accepted papers above. Accepted late papers will be included in the normal proceedings and technical presentation sessions at the conference.

–over–

Poster Submission: We are continuing a poster session this year, extending upon last years success. You may submit original and unpublished work for consideration as a poster presentation. Posters are presented at a special reception specifically designed for display and discussion of this work on Tuesday evening at the symposium. Posters are limited to 2 pages and will be included in the symposium proceedings.

Electronic Submission Procedures: Please follow electronic submissions instructions on the IRPS Web page: http://www.irps.org/tpc. In addition to the paper or abstract submission, we also require a cover page with a 50-word abstract of your work, the category of submission from the above listing, as well as the authors' affiliation, addresses, phone & FAX numbers and e-mail addresses, and completed paper release forms. Send electronic submissions to Tim_Rost@irps.org. All submissions will be acknowledged within two weeks. If you do not receive acknowledgment of your submission, please contact the Technical Program Chair. If it is not possible to send your submission electronically, please contact the Technical Program Chair to make other arrangements.

Contact: Timothy A. Rost, Technical Program Chair, 2003 IRPS
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For general conference information, ***http://www.irps.org/*** or contact:

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