2002 *INTERNATIONAL RELIABILITY PHYSICS SYMPOSIUM*

April 8–11, 2002 • Hyatt Regency Dallas • Dallas, Texas

CALL FOR PAPERS and *New for 2002!* CALL FOR POSTERS

The IRPS promotes the greater understanding of the reliability and performance of integrated circuits and microelectronic assemblies in the user's environment. IRPS accomplishes this by offering its attendees the opportunity to attend technical sessions, tutorials, workshops, and a new poster session, all covering state-of-the-art developments in electronic reliability. **By adding the new poster session, IRPS provides an opportunity for more authors to present their work than had been possible under the prior format**.

YOUR PAPER AND POSTERS ARE SOLICITED DESCRIBING ORIGINAL WORK IN THE FOLLOWING GENERAL CATEGORIES THAT:

A. identifies new, or improves our understanding of, known mechanisms of failure in electronic devices and materials;
B. correlates the influence of fabrication processes with certain failure mechanisms;
C. presents new, innovative, or improved failure analysis techniques or theoretical modeling and simulation of failure mechanisms;
D. describes reliability testing, qualification, and screening methodologies for materials and devices;
E. quantifies the impact of device and circuit design, material, and process selection on reliability;
F. demonstrates techniques to build-in or extend reliability.

For Silicon (Integrated Circuits, Discrete Devices, MEMS) and Non-Silicon (GaAs, LEDs and Diode Lasers, Optical Fiber and Flat Panel Displays) Devices IN THE FOLLOWING SPECIFIC AREAS:

Non-Volatile Memory—Unique Reliability Phenomena and Failure Mechanisms in Non-Volatile Memories.

Product Reliability and Burn-in—Case Histories of Product Reliability Issues; Wafer-Level Reliability Issues. New or Novel Failure Modes in Logic/Memory ICs, Burn-In Elimination Strategies, Wafer-Level Burn-In

Yield Enhancement Effects on Reliability—Correlation between Yield, Infant Mortality, Burn-In

Assembly and Packaging—Package/Assembly Reliability, Stress Modeling, Cu and Low-K Issues, Chip Scale Integation.

Channel Hot Carriers—New Hot Carrier Phenomena; Reliability of Alternative Dielectrics; Oxide Degradation Mechanisms

Interconnects—EM Phenomena in Cu and AL Systems; Low-K/Oxide Inter/Intra-Level Reliability; Mechanical Stress Related Reliability Issues

Device and Process—Reliability Driven Process Interactions; New Process-Related Reliability Issues. Includes Si, and Non Si based, OptoElectronics, MEMS

Device Dielectrics—Oxide Breakdown Mechanisms; New or Novel Dielectric Systems Reliability; Processing Interactions, Non-Volatile Memory

ESD and Latch-Up—Novel Structures including SOI and Bipolar; Damage Interpretation

Process Induced Damage—Reliability Degradation Associated with Damage; Early Detection and Reliability Analysis

Failure Analysis—New Failure Mechanisms and Failure Analysis Techniques, Case Histories

Qualification Strategies—New Techniques for Technology or Process Qualification; Case Histories or Best Practices to Reducer Time-to-Market

Submission Deadline (Abstracts Must Be Received By): September 15, 2001

Abstract Preparation: Paper and poster acceptance is based entirely on summary submission. Your work must be ***original*** and ***unpublished***. Authors should declare whether the submission is for consideration as paper only, poster only, or either paper or poster. Your summary shall be a ***maximum of two pages long***, and shall clearly and concisely state the specific results of your work, why it is important, and how it relates to prior work. The summary should include graphs, drawings, photographs, and key references as necessary within the two-page limit. Separate from the two-page summary, we also require a cover page with a 50-word abstract of your work, the category of submission from the above listing, as well as the authors' affiliation, addresses, phone & FAX numbers and e-mail addresses.

Submission: Summaries and abstracts will be accepted in either electronic (preferred) or paper format. Please follow electronic instructions on the IRPS Web page http://www.irps.org/tpc. ***Send electronic submissions to Bernie_Pietrucha@irps.org***. Please limit summary file size to a maximum of 2MB. All submissions will be acknowledged within three weeks. If you do not receive acknowledgment of your submission, please contact the Technical Program Chair. For paper format, we require 1 copy of your one-page, 50-word abstract and 1 paper copy of your 2-page summary to be sent via ***express mail***.

Mail to:

Bernie M. Pietrucha, Technical Program Chair, 2002 IRPS
Lucent Technologies, Room 4E-230
67 Whippany Road PO Box 801
Whippany, NJ 07981 USA

Tel: (973)-386-4730
Fax: (973)-386-3806
e-mail: Bernie_Pietrucha@irps.org

–over–

Late Papers: A limited number of excellent late papers reflecting important breakthrough developments can be considered on a space-available basis. Abstract and summary must be received ***no later than December 1, 2001*** to be considered. Late papers must still meet the publication deadline stated below.

Presentation: Papers will be presented in both plenary and parallel technical sessions. Posters will be open for presentation during the Tuesday evening reception approximately one hour after the reception begins.

Proceedings Manuscript: Final, camera-ready manuscripts of the final paper must be received by February 4, 2002 so that the proceedings can be available at the Symposium. Submissions accepted as posters will have the 200-word summary published in the proceedings.

Sponsors:
The Electron Devices Society and the Reliability Society of The Institute of Electrical & Electronic Engineers, Inc. are the sponsors of the 2002 IRPS.

Mail list: Send requests, address changes, and/or if you don't want your address available to BoD approved renting of the IRPS mail list to pub_services@irps.org or IRPS, P.O. Box 308, Westmoreland, NY 13490.

For general conference information, *http://www.irps.org/* or contact:

USA
William R. Tonti
General Chair, 2002 IRPS
IBM Microelectronics
1000 River Street
Essex Junction, VT 05452 USA
Tel: (802)769-6561
Fax: (802) 769-6567
e-mail: wtonti@us.ibm.com

For registration and mailings
IRPS Publishing Services
P.O. Box 308
Westmoreland, NY 13490 USA
Tel: (315) 339-3968 / Fax: (315) 336-9134
e-mail: pub_services@irps.org

Asia
Dr. Eiji Takeda, IRPS Publicity Committee
Hitachi Ltd., Central Research Laboratory
Kokubunji, Tokyo 185-8601 Japan
Tel: (81) 423-23-1111 x2001
Fax: (81) 423-27-7687
e-mail: ETAKEDA@CRL.HITACHI.CO.JP

Prof. Daniel S.H. Chan
IRPS Publicity Committee
Dept. of Electrical and Computer Engineering
National University of Singapore
4 Engineering Drive 3
Singapore 117576
Tel: (65) 874-2117 / Fax: (65) 779-1103
e-mail: Daniel.Chan@ieee.org

Europe
Mauro Ciappa, IRPS Publicity Committee
Swiss Federal Institute of Technology (ETH)
Integrated Systems Laboratory
ETH-Zentrum
CH-8092 Zurich, Switzerland
Tel: (41) 1-632-2436
Fax: (41) 1-632-1194
e-mail: CIAPPA@IIS.EE.ETHZ.CH

Fred G. Kuper, IRPS Publicity Committee
Philips Semiconductors
MOS4YOU, Gerstweg 2
6534 AE Nijmegen
The Neitherlands
and MESA+ Research Institute of the University of Twente
Tel: (31) 24-353-22896 / Fax: (31) 24-353-5177
e-mail: Fred.Kuper@Philips.com