2001 INTERNATIONAL RELIABILITY PHYSICS SYMPOSIUM

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APRIL 30 – MAY 3, 2001 • WYNDHAM PALACE RESORT AT DISNEYWORLD • ORLANDO, FLORIDA

PRELIMINARY PROGRAM

• TUTORIALS • Monday, • April 30, • 8:00 a.m.-5:00 p.m. • Chair: T. Rost, TI • Vice Chair: P. Dixit, Sun Microsystems

Morning Session (8:00 a.m. – 11:30 a.m.)

1. Errors Made When Performing Reliability Experiments: Discussion, Consequences and Applications – L. Tielemanns, Destin N.V./K. Croes, Limburgs Universitair Centrum (8:00 – 11:30)
2. Silicon Amnesia: A Tutorial on Radiation Induced Soft Errors – R. Baumann, Texas Instruments (8:00 – 9:30)
3. Semiconductor Foundry Qualification Panel Discussion – Leaders in the semiconductor foundry business present their views on product qualification strategies (10:00 – 11:30)
4. New Phenomena in the Device Reliability Physics of Advanced Submicron CMOS Technologies - G. LaRosa/S.E. Rauch/F. Guarin, IBM (8:00 – 11:30)
5. ESD Reliability Physics, Devices, & Circuits – S. Voldman, IBM (8:00 – 11:30)

Afternoon Session (1:30 p.m. – 5:00 p.m.)

6. Aerosol Spray and the Cooling of Microelectronics – P. Boudreaux, Univ. of Maryland/D. Tilton, Isothermal Systems Research (1:30 – 3:00)
7. A Chip Designer's Perspective on Reliability – D. Overhauser, Simplex (1:30 – 3:00)
8. Thin Gate Oxide Reliability: Degradation, Statistics, and Breakdown Modes – J. Suñé, Universitat Autònoma de Barcelona /E. Miranda, Universidad de Buenos Aires (1:30 – 3:00)
9. Ferroelectric Material and Device Reliability – D. Hadnagy, Ramtron International (3:30 – 5:00)
10. Microstructure, Processing and Reliability of Cu-Based Interconnect Structures – J. Sanchez, AMD (3:30 – 5:00)
11. Qualification for Reliability in Time-to-Market Driven Product Creation Processes – W. Gerling, Infineon/F.-W. Wulfert, Motorola (1:30 – 5:00)

Tuesday, May 1, 8:00 a.m. — *Plenary Session*

SYMPOSIUM OPENING: • General Chair: Anthony S. Oates, Lucent Technologies • Technical Program Chair: Eric S. Snyder, Sandia Technologies

PRODUCT RELIABILITY I

1.1 Reliability Degradation of High Density DRAM Cell Transistor Junction Leakage Current Induced by Band-to-defect Tunneling Under the Off-state Bias-temperature Stress—Y.P. Kim/Y.W. Park/J.T. Moon/S.U. Kim, Samsung Electronics Co., Ltd.
1.2 A New Method for Predicting Distribution of DRAM Retention Time—Y. Mori/R. Yamada/S. Kamohara/M. Moniwa/K. Ohyu/T. Yamanaka, Hitachi, Ltd.
1.3 Is Product Screen Enough to Guarantee Low Failure Rate for the Customer?—M.W. Ruprecht, Infineon Technologies/G. La Rosa/R.G. Filippi, IBM Microelectronics
1.4 Analysis of Erratic Bits in FLASH Memories—A. Chimenton/P. Pellati/P. Olivo, Università di Ferrara
1.5 Individual Cell Measuring Method for FeRAM Retention Testing—N. Tanabe/H. Koike/T. Miwa/J. Yamada/A. Seike/N. Kasai/H. Toyoshima/H. Hada, NEC Corp.
1.6 Yield Enhancement and Yield Management of Silicon Foundries using Iddq "Stress Current Signature"—M. Rubin/S. Natan/D. Leary, Agilent Technologies
1.7 Dynamic Voltage Stressing Applying In the Reduction of The Early Failure Rate—C.-Y. Tsao/R.Y. Shiue/C.C. Ting/Y.S. Huang/Y.C. Lin/J. Yue, TSMC

Tuesday, May 1, 2:00 p.m. — *Parallel Session*

PROCESS & RELIABILITY INTERACTIONS

2A.1 A Study of Formation and Failure Mechanism of CMP Scratch Induced Defects on ILD in a W-damascene interconnect SRAM Cell—S.-M. Jung/H.S. Kang/W.S. Cho/J.S. Uom/Y.J. Bae/K.S. Ku/K.Y. Kim/K.T. Kim, Samsung Electronics Co., Ltd.
2A.2 The Effects of STI Process Parameters on the Integrity of Dual Gate Oxides—H. Lim/S.-J. Lee/J.-M. Youn/T.-H. Ha/J.-H. Kim/B.-H. Choi/K.-J. Kim/K.-T. Kim, Samsung Electronics Co., Ltd.
2A.3 Improvement in Retention Reliability of SONOS Nonvolatile Memory Devices by Two-step High Temperature Deuterium Anneals—J. Bu/M.H. White, Lehigh Univ.
2A.4 Data Retention Failure in NOR Flash Memory Cells—W.H. Lee/D.-K. Lee/Y.-M. Park/K.-S. Kim/K.-O. Ahn/K.-D. Suh, Samsung Electronics Co., Ltd.
2A.5 A New Conduction Mechanism for the Anomalous Bits in Thin Oxides Flash EEPROMs—A. Modelli, STMicroelectronics/F. Gilardoni/D. Ielmini, Politecnico di Milano/S. Spinelli, Università degli Studi dell'Insubria
2A.6 N-Channel Versus P-Channel Flash EEPROM-Which One has Better Reliabilities—S.S. Chung/S.T. Liaw/C.M. Yih/Z.H. Ho/, National Chiao Tung Univ./C.J. Lin/D.S. Kuo/M.S. Liang, TSMC
2A.7 New Technique for Fast Characterization of SILC Distribution in Flash Arrays—D. Ielmini, Politecnico di Milano/A.S. Spinelli, Università degli Studi dell'Insubria/A.L. Lacaita, Politecnico di Milano/L. Confalonieri/A. Visconti, STMicroelectronics

Tuesday, May 1, 2:00 p.m. — *Parallel Session*

MEMS RELIABILITY CHARACTERIZATION

2B.1 Reliability of a MEMS Torsional Ratcheting Actuator—D.M. Tanner/S.M Barnes/J.A Walraven/N.F. Smith, Sandia National Labs
2B.2 Full Three-Dimensional Motion Characterization of a Gimballed Electrostatic Microactuator—C. Rembe, Univ. of California/L. Muller, Network Photonics, Inc./R.S. Muller/A.P. Pisano/R.T. Howe, Univ. of California
2B.3 Non-Destructive Resonant Frequency Measurement on MEMS Actuators—N.F. Smith/D.M. Tanner/S.L. Miller, Sandia National Labs
2B.4 Size Effect on the Mechanical Properties and Reliability Analysis of Microfabricated Polysilicon Thin Films—J.N. Ding/Y.G. Meng/S.Z. Wen, Tsinghua Univ.

PACKAGING AND ASSEMBLY

2C.1 *(invited, ESREF best paper)* A Simple Model for the Mode I Popcorn Effect for IC Packages—P. Alpern/K.C. Lee, Infineon Technologies/R. Dudek, IZM/R. Tilgner, Infineon Technologies
2C.2 Improving Corrosion-Resistance of Silicon-Glass Micropackages Using Boron Doping and/or Self-Induced Galvanic Bias—B.H. Stark/M.R. Dokmeci/T.J. Harpster/K. Najafi, Univ. of Michigan
2C.3 A Fatigue Theory for Solders—S. Wen/L.M. Keer, Northwestern Univ.
2C.4 A New Mechanical Concept and Its Application in Reliability Evaluation of Solder Joint Connections Used in Electronic Packaging—X. Ma, CEPREI/Y. Qian, Harbin Institute of Technology/X. Zhang, CEPREI

Wednesday, May 2, 8:00 a.m. — *Parallel Session*

OXIDE I

3A.1 *(Invited)* Defect Generation and Reliability of Ultra-thin Silicon Dioxide at Low Voltage—J.H. Stathis/D.J. DiMaria, IBM
3A.2 *(Invited)* Identification of Atomic Scale Defects Involved in Oxide Leakage Currents—P.M. Lenahan/J.J. Mele/J. Campbell/A. Kang, Penn State Univ./R.K. Lowry/D. Woodbury, Intersil/S.T. Liu, Honeywell
3A.3 Nanoscale Observations of the Electrical Conduction of Ultra Thin SiO_2 Films with Conducting Atomic Force Microscopy—M. Porti/M. Nafría/X. Aymerich, Universitat Autònoma de Barcelona/A. Olbrich/B. Ebersberger, Infineon Technologies AG
3A.4 Softening of Breakdown in Ultra-thin Gate Oxide nMOSFETs at Low Inversion Layer Density—S. Lombardo, CNR-IMETEM/F. Crupi, Università di Messina/J.H. Stathis, IBM

(3A continued over)

Wednesday, May 2, 8:00 a.m. — *Parallel Session*

OPTOELECTRONICS & COMPOUND SEMICONDUCTOR

3C.1 Accelerated Stressing and Degradation Mechanisms for Si-based Photoemitters—A. Chatterjee/B.L. Bhuva, Vanderbilt Univ.
3C.2 Low-Temperature, High-Current Lifetests on InP-Based HBT's—B.M. Paine/S. Thomas III*/M.J. Delaney, Hughes Space & Comm. Co. *HRL Labs
3C.3 Degradation Characteristics of AlGaN/GaN High Electron Mobility Transistors (HEMTs)—H. Kim/B. Green/V. Tilak/H. Cha/ J.A. Smart/J.R. Shealy/L.F. Eastman, Cornell Univ.

ELECTROSTATIC DISCHARGE/LATCHUP

3D.1 Characterization & Investigation of the Interaction Between Hot Electron & Electrostatic Discharge Stresses Using NMOS Devices in 0.13µm CMOS Technology—A. Salman*/R. Gauthier**/S. Furkay**/M. Muhammad, GCI/C. Putnam**/D. Ioannou*/P. Nguyen**/W. Stadler, Infineon Technologies
*George Mason Univ. **IBM Microelectronics

(3D continued over)

Wednesday, May 2, 8:00 a.m. — *Parallel Session 3A continued*

3A.5 Calculating the Error in Long Term Oxide Reliability Estimates—B.P. Linder/J.H. Stathis/D.J. Frank, IBM

WLR FOR INTERCONNECTS

3B.1 Comparison of Isothermal, Constant Current and SWEAT Wafer Level EM Testing Methods—T. Lee/D. Tibel/T. Sullivan, IBM Microelectronics

3B.2 Real Case Study For Isothermal EM Test As A Process Control Methodology—S.-Y. Lee/J.B. Lai/S.C. Lee/L.H. Chu/R.Y. Shiue/J.Yue, TSMC

3B.3 Experimental Comparison of Wafer Level Reliability (WLR) and Packaged Electromigration Tests—C. Ryu/T.-L. Tsai/A. Rogers/C. Jesse/T. Brozek/D. Zarr/M. Adamson/S. Nayak/J. Walls, Motorola SPS

3B.4 Comparison of Via/Line Package Level vs. Wafer Level Results—D. Tibel/T. Sullivan, IBM Microelectronics

Wednesday, May 2, 8:00 a.m. — *Parallel Session 3D continued*

3D.2 Non-uniform Bipolar Conduction in Single Finger NMOS Transistors and Implications for Deep Submicron ESD Design—K.-H. Oh, Stanford Univ./C. Duvvury/C. Salling, Texas Instruments/K. Banerjee/R.W. Dutton, Stanford Univ.

3D.3 Advanced 2D Latch-up Device Simulation – a Powerful Tool During Development in the Pre-silicon Phase—S. Bargstädt-Franke/K. Oettinger, Infineon Technologies

3D.4 An Analysis of Bipolar Breakdown and its Application to the Design of ESD Protection Circuits—S. Joshi, Univ. of Illinois/R. Ida/P. Givelin, Motorola/E. Rosenbaum, Univ. of Illinois

3D.5 Parasitic Bipolar Transistor Model using Generated-Hole-Dependent Base Resistance—K. Suzuki/H. Anzai/T. Nomura/S. Satoh, Fujitsu Labs Ltd.

3D.6 Design and Analysis of New Protection Structures for Smart Power Technology with Controlled Trigger and Holding Voltage—V. De Heyn/G. Groeseneken/B. Keppens/N. Mahadeva Iyer, IMEC/L. Vacaresse/G. Gallopyn, Alcatel Microelectronic

Wednesday, May 2, 2:00 p.m.— *Parallel Session*

PRODUCT RELIABILITY II

4A.1 Historical Trend in Alpha-Particle induced Soft Error Rates of the Alpha Microprocessor—N. Seifert/D. Moyer/N. Leland, Compaq Comp.

4A.2 A Reliability Methodology for Low Temperature Data Retention in Floating Gate Non-Volatile Memories—P.J. Kuhn/A. Hoefler/T.S. Harp/B.E. Hornung/R.E. Paulsen/D. Burnett/J.M. Higman, Motorola

4A.3 High-Performance Chip Reliability from Short-Time-Tests: Statistical Models for Optical Interconnect and HCI/TDDB/NBTI Deep-Submicron Transistor Failures—A. Haggag/K. Hess/W. McMahon/K. Cheng/J. Lee/J. Lyding, Univ. of Illinois

4A.4 An Application-Specific Usage Model for Flash Memory Read Disturb Reliability—T.S. Harp/P.J. Kuhn/J.M. Higman/R.E. Paulsen/B.E. Hornung, Motorola

FAILURE ANALYSIS

4B.1 Case History: Novel FA Techniques Used to Recover EEPROM Data from the Swissair 111 Crash—R. Haythornthwaite/A. Earle/A. Rahal, Chipworks Inc.

4B.2 Novel Nondestructive and Non-electrical-contact Failure Analysis Technique - Scanning Laser-SQUID Microscopy—K. Nikawa/S. Inoue, NEC Corp.

4B.3 Analysis of Via-Void Generation Mechanism for Giga-bit-scale DRAM—D.H. Kim/J.S. Park/B.C. Kim/S.C. Lee/M.K. Bae/J.W. Nam/I.S. Park/H.Y. Kim/T.K. Kim/J.S. Kim/Y.J. Park/J.I. Hong/J.W. Park, Samsung Electronics Co., Ltd.

4B.4 Study of Metal Impurities Behavior Due to Difference in Isolation Structure on ULSI Devices—K. Matsukawa/Y. Kimura/H. Yamamoto/Y. Mashiko, Mitsubishi Electric Corp.

4B.5 High SRAM Standby Current Due to the Printing of Spurious Images—S.-Y. Tang/M. Mims/T. Cynkar/P.J. Marcoux/D.H. Eaton, Agilent Technologies, Inc.

Wednesday, May 2, 2:00 p.m.— *Parallel Session*

PROCESS INDUCED DAMAGE

4C.1 The Impact of Trench Geometry & Processing on the Performance & Reliability of Low Voltage Power UMOSFETs—S.A. Suliman/N. Gallogunta/L. Trabzon/J. Hao*/G. Dolny*/R. Ridley*/T. Greb*/J. Benjamin*/C. Kocon*/J. Zeng*/O.O. Awadelkarim/S.J. Fonash/M. Horn/J. Ruzyllo, Penn State Univ. *Intersil

4C.2 The Effects of Plasma Induced Damage on Transistor Degradation and the Relationship to Field Programmable Gate Array Performance—F.E. Pagaduan/J.K. Lee/V. Vedagarbha/K. Lui/M.J. Hart/D. Gitlin, Xilinx, Inc./T. Takaso/S. Kamiyama/K. Nakayama, Seiko Epson Corp.

4C.3 Improvement of MOSFET Subthreshold Leakage Current by its Irradiation with Hydrogen Radicals Generated in Microwave-Excited High-Density Inert Gas Plasma—Y. Saito/H. Takahashi/K. Ohtsubo/M. Hirayama/S. Sugawa, Tohoku Univ./H. Aharoni, Ben-Gurion Univ./T. Ohmi, Tohoku Univ.

INTERCONNECT RELIABILITY

4D.1 Reservoir Modeling for Electromigration Improvement of Metal Systems with Refractory Barriers—M.J. Dion, Intersil

4D.2 The Quantitative Assessment of Stress-induced Voiding in Process Qualification—A.H. Fischer/A.E. Zitzelsberger/M. Hommel, Infineon Technologies

4D.3 Statistics of Electromigration Early Failures in Cu/oxide Dual-damascene Structures—E.T. Ogawa/K.-D. Lee/H. Matsuhashi/A.J. Bierwag/P.R. Justison/A.N. Ramamurthi/P.S. Ho, Univ. of Texas Austin/V.A. Blaschke/R.H. Havemann, SEMATECH

4D.4 Trade-off Between Reliability and Post-CMP Defects with Recrystallization Anneal in Copper Damascene Interconnects—G.B. Alers, Novellus Systems/D. Dornisch, Conexant/J. Siri/K. Kattige/L. Tam/E. Broadbent/G. Ray, Novellus Systems

4D.5 Impact of Low-K Dielectrics and Barrier Metals on TDDB Lifetime of Cu Interconnects—J. Noguchi/T. Saitoh/N. Ohashi/H. Ahihara/H. Maruyama/M. Kubo/H. Yamaguchi/D. Ryuzaki, K.-I. Takeda/K. Hinode, Hitachi, Ltd.

Wednesday • May 2, • 7:30 p.m. — WORKSHOPS — Chair: S.D. Khandekar, Intel/Vice Chair: J. McDaniel, Lucent

Please sign-up for the workshop of your choice at www.irps.org/ws and on the registration form included with this program.

1. FIB User's group
2. Dielectric Reliability
3. Hot Carriers
4. Failure Analysis
5. Interconnect/Copper & Low K
6. MEMS
7. Package
8. ESD/Latchup

Thursday, May 3, 8:00 a.m. — **OXIDE II** — *Plenary Session*

5.1 Relation Between Breakdown Mode and Breakdown Location in Short Channel NMOSFETs and its Impact on Reliability Specifications—R. Degraeve/B. Kaczer/A. De Keersgieter/G. Groeseneken, IMEC

5.2 Analytic Modeling of Leakage Current Through Multiple Breakdown Paths in SiO_2 Films—E. Miranda, Univ. de Buenos Aires/J. Suñé, Univ. Autónoma de Barcelona

5.3 Experimental Study of Gate Voltage Scaling for TDDB under Direct Tunneling Regime—M. Takayanagi/S.-I. Takagi/Y. Toyoshima, Toshiba Corp.

5.4 Accurate and Robust Noise-based Trigger Algorithm for Soft Breakdown Detection in Ultra Thin Oxides—P. Roussel/R. Degraeve/B. Kaczer/G. Groeseneken, IMEC

5.5 Soft Breakdown Triggers for Large Area Capacitors Under Constant Voltage Stress—J. Schmitz/H.J. Kretschmann/H.P. Tuinhout/P.H. Woerlee, Philips Research Labs

PANEL DISCUSSION— "Is Burn-in Elimination Possible?"

Thursday, May 3, 2:00 p.m. — **HOT CARRIERS** — *Plenary Session*

6.1 Role of E-E Scattering in the Enhancement of Channel Hot Carrier Degradation of Deep Sub-Micron NMOSFETs at high V_{GS} Conditions—S.E. Rauch III/G. La Rosa/F.J. Guarin, IBM Microelectronics

6.2 Analysis of New Hot Carrier Degradation Phenomena: "W" or "S" Shape Evolution of LDD NMOSFET—J.R. Shih/L.H. Chu/R.Y. Shiue/J. Yue, TSMC

6.3 On the Dominant Interface Trap Generation Process During Hot-Carrier Stressing—D.S. Ang/C.H. Ling, The National Univ. of Singapore

6.4 A New Physical and Quantitative Width Dependent Hot Carrier Model for Shallow-Trench-Isolated CMOS Devices—S.S. Chung/S.-J. Chen/W.-J. Yang/J.-J. Yang, National Chiao Tung Univ.

6.5 Hot-Carrier Reliability of P-MOSFET with Ultra-Thin Silicon Nitride Gate Dielectric—I. Polishchuk/Y.-C. Yeo/Q. Lu/T.-J. King/C. Hu, Univ. of California

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INT'L RELIABILITY PHYSICS SYMPOSIUM
April 30 - May 3, 2001

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2001 RELIABILITY PHYSICS EQUIPMENT DEMONSTRATIONS ♦ April 30-May 3

Monday, noon – 7 p.m. ♦ Tuesday/Wednesday 7:30 a.m. – 6 p.m. ♦ Thursday, 7:30 a.m. – noon

Demonstrations by the following companies:

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- Alpha Innotech Corporation
- Barth Electronics
- Digital Instruments
- Hypervision, Inc.
- Karl Suss America, Inc.
- KeyTek
- Knights Technology, Inc.
- Micro Control Company
- Micro Instrument Company
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- SELA-USA, Inc.
- Semicaps, Inc.
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- ***Tuesday Evening** Attendees' Reception including a **Poster Session of all platform papers presented** at the Symposium.*
- *Participate in one of eight **WEDNESDAY NIGHT WORKSHOPS**—See who's moderating/signed-up to attend and send questions/data for posting at the web site http://www.irps.org/ws.*
- *SAVE through advance purchase of **your Disney PARK HOPPER®Meeting/Convention tickets**. These tickets are created just for you and are not available at front gates of the Theme Parks! Browse: https://secure.hes-services.com/WDWTicket/IEEE.asp*
- *After IRPS concludes, save on a **Kennedy Space Center excursion on Friday, May 4**, including: roundtrip bus transportation from the Wyndham Palace, a maximum accessbadge: including admission to the Visitor Complex, the Imax movie, NASA bus tour (approx. 4 h tour), & a half hour guided tour through the main Visitor Complex. Depart from Wyndham Palace at 9 a.m., returning 7 p.m. Price per adult: $32.00. Price per child (age 3-11): $29.00. Contact Margo Markvoort, Gator Tours, 800-537-0917 or 407-522-5911.*

IRPS COMPANIONS' PROGRAM

The IRPS, is again, pleased to offer a Companions' Program. In addition there will be a Hospitality Suite, for spouses and guests of IRPS attendees, open Monday through Thursday, 8:00 a.m. to 10:00 a.m. For more information on the Companions' Program please contact Sandy Barber, P.O. Box 2098, Banner Elk, NC 28604-2098, or phone 828-898-6375 (Monday through Friday, 10:00 a.m. to 4:30 p.m. EST)**, or send an Email to: sandyirps@aol.com.**

Delta Airlines — IRPS OFFICIAL AIRLINE

Delta Airlines is the official airline for the 2001 IRPS, offering five (5%) discount off Delta's published round-trip airfares, within the Continental US, Hawaii, Alaska, Canada, Mexico, Bermuda, San Juan, Nassau and the US Virgin Islands. A ten (10%) discount will be offered on Delta's domestic system, on published unrestricted round-trip coach (Y06) rates. An additional five (5%) discount, is available, for tickets purchased 60 days or more prior to departure date. Special round-trip zone fares, are also available. Call TOLL FREE: 1-800-241-6760, prompt number one (1), and reference file number 171134A, to obtain fares and make reservations.

Budget Rent A Car

IRPS OFFICIAL CAR RENTAL AGENCY

Budget Rent A Car is the official rental car agency for the 2001 IRPS. To receive the special rates listed below, call TOLL FREE: 1-800-772-3773, and refer to: BCD #U060828.

CAR	DAILY RATE	WEEKLY RATE
Economy	$29.00	$119.00
Compact	$33.00	$129.00
Intermediate	$35.00	$154.00
2-Door Full Size	$38.00	$174.00
4-Door Full Size	$39.00	$189.00
Premium	$46.00	$219.00
Sport Utility	$46.00	$239.00
Luxury	$49.00	$249.00
Mini Van	$49.00	$249.00
Convertible	$49.00	$249.00

All rentals include unlimited free miles. Rates are available one week prior to, and, one week after the official meeting dates, April 30 - May 3, 2001. International attendees may fax reservations to: 1-407-816-4434, or send by email to: Nmclarry@budgetgroup.com.