2000 INTERNATIONAL RELIABILITY PHYSICS SYMPOSIUM

FINAL PROGRAM

TUTORIALS

Monday, April 10, — Chair: Edward I. Cole, Jr. — Vice Chair: Thomas M. Moore

Morning Session (8:00 a.m. - 11:30 a.m.)

1. Thin Gate Oxide Reliability: Past & Present Trends in Characterization, Physical Modeling, & Assessment—J.S. Suehle/E.M. Vogel, NIST, ***Imperial Ballroom*** (8–11:30)
2. Low-k Constant Materials for Cu Interconnects - K. Taylor, TI, ***Regency Ballroom I*** (8-9:30)
3. Reliability Considerations for Cu Metallization Systems for ULSI Circuits— T.D. Sullivan/A.K. Stamper, IBM ***Regency Ballroom I*** (10–11:30)
4. Hot Carrier Reliability Fundamentals in Logic and Memory Technology—P. Fang, AMD , ***Crystal Room*** (8-9:30)
5. ASIC Design for Safety-Critical Applications—T. Ambler, Univ. of Texas, ***Crystal Room*** (10–11:30)
6. Focused Ion Beam Technology & Applications to Microelectronics—M.T. Abramo, IBM/A.N. Campbell, Sandia Nat'l. Labs, ***Regency Ballroom II*** (8–11:30)

Afternoon Session (8:00 a.m. - 11:30 a.m.)

7. Wet Etches for Si Semiconductor Failure Analysis—T.W. Lee, Varian, ***Regency Ballroom II*** (1:30-3)
8. Analytical Challenges in Packaging and Assembly—G. Samuelson/ R. Diaz/D. Goyal/S. Tandon, Intel/T.M. Moore, C. Hartfield, TI, ***Regency Ballroom II*** (3:30-5)
9. Analysis of Cu with Various Low K Dielectric Materials to Determine a Viable Cu-low K Dielectric Candidate for Advanced Interconnect Technology—S.U. Kim, Consultant, ***Regency Ballroom I*** (1:30-3)
10. Thermal Deformation & Interfacial Adhesion in Area-Array Packages for Cu/Low-k Chips - P.S. Ho, Univ. of Texas, ***Regency Ballroom I*** (3:30-5)
11. Product Reliability Assessment & Qual. Methodologies: Current Practices/Future Trends—N.E. Lycoudes, Motorola, ***Imperial Ballroom*** (1:30-5)

WORKSHOPS

Monday, April 10,
(7:30 p.m. -9:30 p.m.)
Chair: Art Rawers
Vice Chair: Marsha Abramo

1. New Packages Technologies
2. Focused Ion Beam
3. Standards for Product Qualification
4. Dielectrics
5. Hot Carrier
6. ESD/Latchup
7. Failure Analysis
8. Wafer Level Reliability
9. Interconnects/Copper/Low-K
10. MEMS

Tuesday, April 11, 8:00 a.m. — *Plenary Session—Imperial Ballroom*

SYMPOSIUM OPENING • KEYNOTE • DIELECTRICS I

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8:00 **SYMPOSIUM OPENING—General Chair: J.E. Klema** and **Technical Program Chair: W.R. Tonti**
8:20 **KEYNOTE:** Silicon Technology Directions in the New Millennium—T.H. Ning 1
9:05 1.1 Experimental Evidence for Voltage Driven Breakdown Models in Ultrathin Gate Oxides—P.E. Nicollian, W.R. Hunter, and J.C. Hu 7
9:30 1.2 Tunneling Current Characteristics and Oxide Breakdown in P+Poly Gate PFET Capacitors—J.M. McKenna, E.Y. Wu, and S.-H. Lo 16
9:55 *Coffee Break*
10:20 1.3 Field Acceleration for Oxide Breakdown - Can An Accurate Anode Hole Injection Model Resolve the E vs. 1/E Controversy?—M.A. Alam, J. Bude, and A. Ghetti 21
10:45 1.4 Anode Hole Injection versus Hydrogen Release: The Mechanism for Gate Oxide Breakdown—J.Wu et al. 27
11:10 1.5 Temperature Dependence of Soft Breakdown and Wear-Out in Sub-3nm SiO_2 Films—J.S. Suehle, E.M. Vogel , B. Wang, and J.B. Bernstein 33
11:35 1.6 Investigation of Ultra-Thin Gate Oxide Reliability Behavior by Separate Characterization of Soft Breakdown and Hard Breakdown—T. Pompl et al. 40
12:00 1.7 Quasi-breakdown in Ultra-Thin SiO_2 Films: Occurrence Characterization and Reliability Assessment Methodology—S. Bruyere, E. Vincent, and G. Ghibaudo 48

Tuesday, April 11, 2:00 p.m.

Parallel Session 2A & 2B — Imperial Ballroom

DIELECTRICS II

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2:00 2A.1 Evidence for Recombination at Oxide Defects and New SILC Model—D. Ielmini et al. 55
2:25 2A.2 Experimental Analysis of Gate Oxide Degradation -Existence of Neutral Trap Precursor, Single and Multiple Trap-assisted Tunneling for SILC Mechanism-—R.-I. Yamada, J.Yugami, and M. Ohkura 65
2:50 2A.3 Temperature Effect on the Reliability of ZrO_2 Gate Dielectric Deposited Directly on Silicon—W.-J. Qi et al. 72
3:15 *Coffee Break*

HOT CARRIERS

3:40 2B.1 Channel-Width Dependent Hot-Carrier Degradation of Thin-Gate pMOSFETs—Y.-H. Lee et al. 77
4:05 2B.2 The Role of the Spacer Oxide in Determining Worst-Case Hot-Carrier Stress Conditions for NMOS LDD Devices—E.E. King et al. 83
4:30 2B.3 Generation of Hot Carriers by Secondary Impact Ionization in Deep Submicron Devices: Model and Light Emission Characterization—B. Marchand *et al* 93
4:55 2B.4 Analysis of Hot-Carrier-Induced Degradation in MOSFETs by Gate-to-Drain and Gate-to-Substrate Capacitance Measurement—C.T. Hsu et al. 98
5:20 2B.5 Hot Carrier Induced Degradation in Deep Submicron MOSFETs at 100°C—E. Li et al. 103
5:45 2B.6 Early Stage Hot Carrier Degradation of State-of-the-Art LDD N-MOSFETs—S.K. Manhas et al. 108

Parallel Session 2C & 2D — Regency Ballroom

MEMS

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2:00 2C.1 Reliability Characterization of Thermal Micro-structures Implemented on 0.8 µm CMOS Chips—L.Y. Sheng et al. 112
2:25 2C.2 Reliability Studies of Bent-Beam Electro-Thermal Actuators—L. Que et al. 118
2:50 2C.3 Nontactile Reliability Testing of a Micro Optical Attenuator—C. Rembe et al. 123
3:15 *Coffee Break*
3:40 2C.4 MEMS Reliability in Shock Environments—D.M. Tanner et al. 129
4:05 2C.5 MEMS Reliability in a Vibration Environment—D.M. Tanner et al. 139
4:30 2C.6 Effect of W Coating on Microengine Performance—S.S. Mani et al. 146

DEVICE & PROCESS I

4:55 2D.1 Neutron-Induced Boron Fission as a Major Source of Soft Errors in Deep Submicron SRAM Devices—R.C. Baumann and E.B. Smith 152
5:20 2D.2 Multi Parameter Method for Yield Analysis and Reliability Assessment—Y. Mitnick et al. 158
5:45 2D.3 CMOSFET Characteristics Induced by Moisture Diffusion from Inter-Layer Dielectric in 0.23 µm DRAM Technology with Shallow Trench Isolation—S.-K. Park et al. 164

SYMPOSIUM RECEPTION — THE TECH MUSEUM OF INNOVATION .... 6:30 — 9:30 p.m.

Wednesday April 12, 8:15 a.m.

Parallel Session 3A — Imperial Ballroom

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8:40 3A.2 Hot-Carrier Reliability Of Lateral DMOS Transistors—V. O'Donovan et al. 174
9:05 3A.3 High Performance Deep-Submicron n-MOSFETs by Nitrogen Implantation and *In-situ* HF Vapor Clean—J.H. Chen et al. 180
9:30 3A.4 Role of Hydrogen Anneal in Thin Gate Oxide for Multi-Metal-Layer CMOS Process—Y.-H. Lee et al. 186
9:55 *Coffee Break*
10:20 3A.5 Analysis of Evolution To and Beyond Quasi-breakdown in Ultra-thin Oxide and Oxynitride—M. Okandan et al. ... 191
10:45 3A.6 A New Data Retention Mechanism After Endurance Stress on Flash Memory—H. Kameyama et al. 194
11:10 3A.7 Analysis of Detrap Current Due to Oxide Traps to Improve Flash Memory Retention—R.-I. Yamada et al. . 200
11:35 3A.8 Bias Temperature Degradation of pMOSFETs: Mechanism and Suppression—M. Makabe et al. 205

Parallel Session 3B & 3C — Regency Ballroom

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8:15 3B.1 Lifetime Prediction of IGBT Modules for Traction Applications—M. Ciappa and W. Fichtner 210
8:40 3B.2 Failure Analysis and Stress Simulation in Small Multichip BGAs—T.D. Moore and J.L. Jarvis 217
9:05 3B.3 Short and Long-Term Stability Problems of Hall Plates in Plastic Packages—D. Manic, J. Petr, and R.S. Popovic 225
9:30 3B.4 Improved Reliability Prediction Through Reduced-Stress Temperature Cycling—A.R. Cory 231
9:55 *Coffee Break*

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10:20 3C.1 Trends in Silicon Germanium BiCMOS Integration and Reliability—J. Dunn et al. 237
10:45 3C.2 Pulsed Measurements and Circuit Modeling of a New Breakdown Mechanism of MESFETs and HEMTs—E. Zanoni et al. 243
11:10 3C.3 Bias & Temperature Stress Reliability of InGaP/GaAs HBTs—A.A. Rezazadeh et al. 250
11:35 3C.4 Breakdown and Degradation Issues and the Choice of a Safe Load Line for Power HFET Operation—D. Dieci et al. 258
12:00 3C.5 Reliability of Optical Fiber Bragg Grating Sensors at Elevated Temperature—U. Sennhauser et al. 264

Wednesday April 12, 2:00 p.m.

Parallel Session 4A — Imperial Ballroom

ELECTROSTATIC DISCHARGE

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2:25 4A.2 Analysis of Oxide Breakdown Mechanism Occurring During ESD Pulses—C. Leroux, P. Andreucci, and G. Reimbold 276
2:50 4A.3 Microanalysis of VLSI Interconnect Failure Modes under Short-Pulse Stress Conditions—K. Banerjee et al. 283
3:15 *Coffee Break*
3:40 4A.4 Transmission Line Model Testing of Top-Gate Amorphous Silicon Thin-Film Transistors—N. Tosic, F.G. Kuper, and T. Mouthaan 289
4:05 4A.5 Process and Layout Dependent Substrate Resistance Modeling for Deep Sub-Micron ESD Protection Devices—X.Y. Zhang et al. 295
4:30 4A.6 Simulation and Experimental Study of Temperature Distribution During ESD Stress in Smart-Power Technology ESD Protection Structures—K. Esmark et al. 304
4:55 4A.7 Electrostatic Discharge and High Current Pulse Characterization of Epitaxial-Base Silicon-Germanium Heterojunction Bipolar Transistors—S. Voldman et al. 310

Parallel Session 4B — Regency Ballroom

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2:00 4B.1 The Role of Copper in Electromigration: The Effect of a Cu-Vacancy Binding Energy—M.J. Tammaro 317
2:25 4B.2 Electromigration Lifetime Enhancement for Lines With Multiple Branches—M.J. Dion 324
2:50 4B.3 Effect Of Ti Insertion Between Cu And TiN Layers On Electromigration Reliability In Cu/(Ti)/TiN/Ti Layered Damascene Interconnects—K. Abe et al. 333
3:15 *Coffee Break*
3:40 4B.4 TDDB Improvement in Cu Metallization under Biass Stress—J. Noguchi et al. 339
4:05 4B.5 Conduction Processes in Cu/Low-K Interconnection—G. Bersuker, V. Blaschke, S. Choi, and D. Wick 344
4:30 4B.6 Leakage and Breakdown Reliability Issues Associated with Low-k Dielectrics in a Dual-Damascene Cu Process—R. Tsu et al. 348
4:55 4B.7 Quantitative Projections of Reliability and Performance for Low-k/Cu Interconnect Systems—K. Banerjee et al. 354
5:20 4B.8 Experimental Data and Statistical Models for Bimodal EM Failures—A.H. Fischer, A. Abel et al. 359

Thursday April 13, 8:15 a.m. — *Plenary Session 5 and Panel Discussion— Imperial Ballroom*

PLASMA INDUCED DAMAGE

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8:15 5.1 A Model for Evaluationg Cumulative Oxide Damage from Multiple Plasma Processes—K. Noguchi, A. Matsumoto, and N. Oda. 364
8:40 5.2 On-Chip Probes for Silicon Defectivity Ranking and Mapping—A. Zanchi et al. 370
9:05 5.3 Detection of Thin Oxide (3.5 nm) Dielectric Degradation due to Charging Damage by Rapid-Ramp Breakdown—T.B. Hook, D. Harmon, and C. Lin 377
9:30 5.4 Charge Pumping Technique for the Evaluation of Plasma Induced Edge Damage in Shallow S/D Extension Thin Gate Oxide NMOSFET's—S.S. Chung et al. 389
9:55 *Coffee Break*

10:20 **OXIDE PANEL— "Is technology scaling limited by oxide reliability?"** *Panel:* J.W. McPherson, TI, D.J. Dumin, Clemson Univ., C. Hu, UC Berkeley, E.M. Vogel, NIST, J.S. Suehle, NIST, W.W. Abadeer, IBM, B.E. Weir, Lucent Technologies, R. Degraeve, IMEC, and S.A. Hareland, Intel; *Moderators:* W.R. Tonti and A.S. Oates

Thursday April 13, 2:00 p.m. *Plenary Session 6 — Imperial Ballroom*

FAILURE ANALYSIS

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2:25 6.2 Electrical Probing of Deep Sub-Micron ICs Using Scanning Probes—K. Krieg et al. 399
2:50 6.3 A Study of Implant Damage Induced Thin Oxide Film Expansion During Photoresist Dry Etching,—K.-P. Lin et al. 404
3:15 *Coffee Break*
3:40 6.4 Reliability Assessment Through Defect Based Testing—B. Lisenker and Y. Mitnick 407
4:05 6.5 Localizing Power to Ground Shorts in a Chips-First MCM by Scanning SQUID Microscopy—W.E. Vanderlinde et al. 413
4:30 6.6 Single Contact Optical Beam Induced Currents (SCOBIC) - A New Failure Analysis Technique—J.M. Chin et al. 420
4:55 Symposium Closing Ceremony—J.E. Klema//A.S. Oates

Don't forget to Vote for Best Paper & Pick up a Momento!