Projet 9 - H_2_PONT / Commande d'onduleur en demi–pont.

Projet : PROJETS-IUT1

Info : [DATA079]

Info : Sujet de formation de projet IUT 2ème année 1998/1999.

Révision : 5 du 18 octobre 1998.

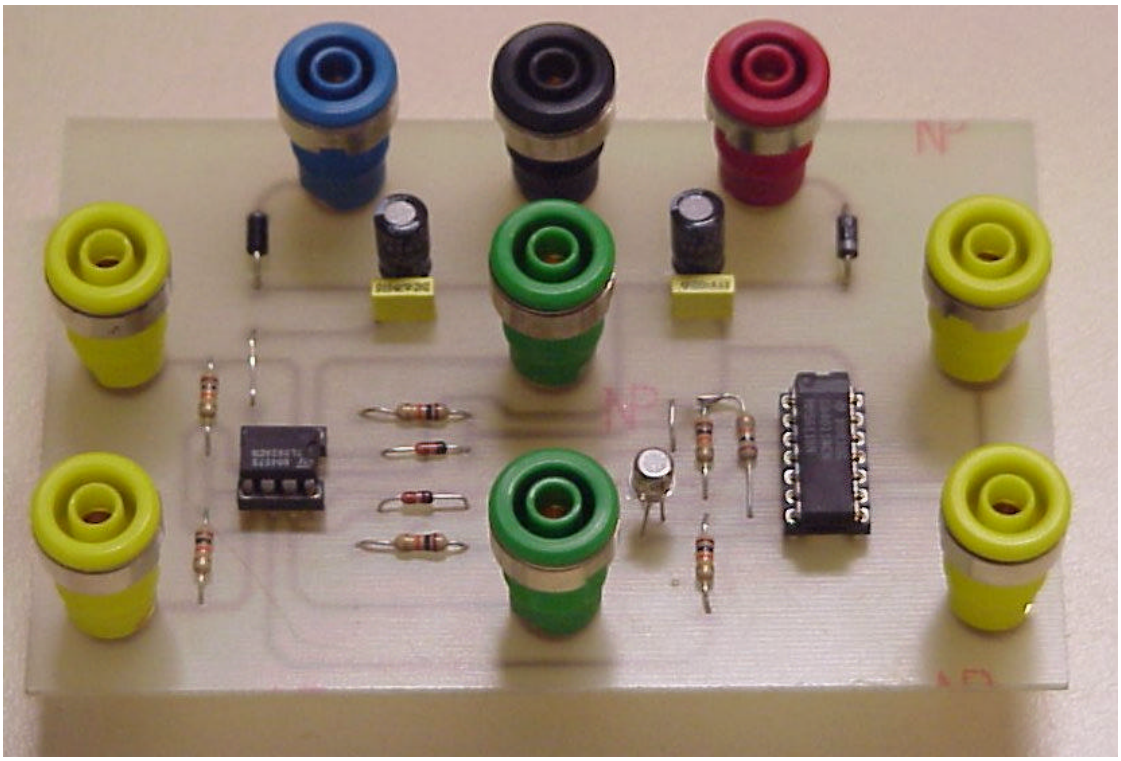


Figure 9.1. Vue du circuit imprimé (images-maquettes\command0.jpg).

9.1 Liste des documents

- Liste des composants.
- Schéma électronique.
- Implantation des composants
- Circuit imprimé coté cuivre.
- Documentations : CD4011D, TL082, 2N2222A.

Tableau 9.1. Liste des composants (projets-iut1.xls\H2PONT).

Item	Qu.	Référence :	Valeur	Tension / Puissance	Technologie / Fabricant	Empreinte
1	2	C3,C1	100nF	63V	MKT	CK06
2	2	C2,C4	47uF	25V	chimique	CK06
3	6	D1,D2,D3,D4,D5,D6	1N4148			DO35
4	2	D7,D8	1N4001			DO41
5	1	JP1	MLI	jaune		EMBASE
6	1	JP2	SINUS	jaune		EMBASE
7	1	JP3	BRAS 1	jaune		EMBASE
8	1	JP4	-SIGNE	verte		EMBASE
9	1	JP5	BRAS 2	verte		EMBASE
10	1	JP6	TRIANGLE	jaune		EMBASE
11	1	JP7	+15V	rouge		EMBASE
12	1	JP8	GND	noire		EMBASE
13	1	JP9	-15V	bleue		EMBASE
14	2	R1,R4	1K	1/4 W		RC05
15	4	R2,R3,R5,R6	10K	1/4 W		RC05
16	1	U1	TL082		ST	08DIP300L
17	1	U2	CD4011BE		ST	14DIP300

Réf.	Désignation	Qu.	Fournisseur	Date	Code Cde	Page	Prix U.H.T.	Prix T.H.T.
C1,C2	100 nF 63 V MKT	2					1.20 F	2.40 F
C3,C4	47 uF 10V chimique radial	2					3.50 F	7.00 F
D1,D2	1N4148	2					0.20 F	0.40 F
D3,D4	1N4001	2					0.50 F	1.00 F
Q1	2N2222	1					1.50 F	1.50 F
R1,... ,R5	10K	5					0.06 F	0.30 F
U1	TL082	1					6.00 F	6.00 F
U2	CD4011	1					4.00 F	4.00 F
U3,...,U10	Douille double isolation à visser	9					19.32 F	173.88 F
Divers	Support 8 broches tulipe	1					1.60 F	1.60 F
Divers	Support 14 broches tulipe	1					2.80 F	2.80 F
Divers	C.I. simple face 100x100 mm	100					0.15 F	15.00 F

TOTAL H.T. :		215.88 F
dont T.V.A.	20.60%	44.47 F
TOTAL T.T.C. :		260.35 F

Embases de sécurité à terminaison filetée

HCK

- Embases de sécurité 4 mm à raccordement par tige filetée M4.
- La fixation de l'embase sur la face avant est réalisée par un écrou à bague.

Spécifications techniques

Intensité: 32 A

Tension de service: 1000 V

Catégorie de surtension: III

Trou de fixation: 12,2 mm

U.D.V.=1

couleur	code commande	prix de l'U.D.V. 1-49	50-99	100+
Rouge	230-6344	**20.40** Fr	**18.36** Fr	**16.32** Fr
Noir	230-6350	**20.40** Fr	**18.36** Fr	**16.32** Fr
Bleu	230-6366	**20.40** Fr	**18.36** Fr	**16.32** Fr
Jaune	230-6372	**20.40** Fr	**18.36** Fr	**16.32** Fr
Vert	230-6388	**20.40** Fr	**18.36** Fr	**16.32** Fr

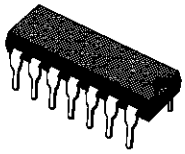
SGS-THOMSON MICROELECTRONICS

HCC4011B/12B/23B
HCF4011B/12B/23B

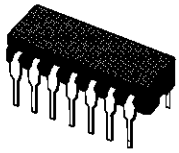
NAND GATES

QUAD 2 INPUT HCC/HCF 4011B
DUAL 4 INPUT HCC/HCF 4012B
TRIPLE 3 INPUT HCC/HCF 4023B

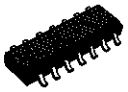
- PROPAGATION DELAY TIME = 60ns (typ.) AT C_L = 50pF, V_{DD} = 10V
- BUFFERED INPUTS AND OUTPUTS
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- 5V, 10V AND 15V PARAMETRIC RATINGS
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N°. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



EY
(Plastic Package)



F
(Ceramic Frit Seal Package)



M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

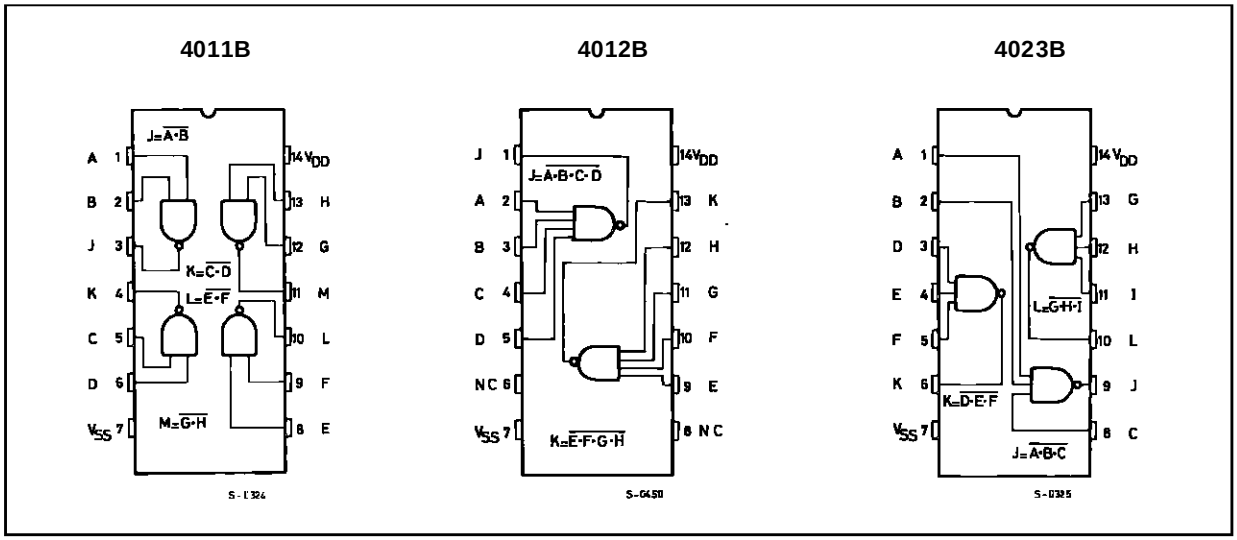
HCC40XXBF	HCF40XXBM1
HCF40XXBEY	HCF40XXBC1

DESCRIPTION

The **HCC4011B, HCC4012B** and **HCC4023B** (extended temperature range) and **HCF4011B, HCF4012B** and **HCF4023B** (intermediate temperature range) are monolithic, integrated circuit, available in 14-lead dual in-line plastic or ceramic package and plastic micropackage.

The **HCC/HCF4011B, HCC/HCF4012B** and **HCC/HCF4023B** NAND gates provide the system designer with direct implementation of the NAND function and supplement the existing family of COS/MOS gates. All inputs and outputs are buffered.

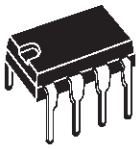
PIN CONNECTIONS



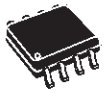
TL082
TL082A - TL082B

GENERAL PURPOSE J-FET DUAL OPERATIONAL AMPLIFIER

- WIDE COMMON-MODE (UP TO V_{CC}^+) AND DIFFERENTIAL VOLTAGE RANGE
- LOW INPUT BIAS AND OFFSET CURRENT
- OUTPUT SHORT-CIRCUIT PROTECTION
- HIGH INPUT IMPEDANCE J–FET INPUT STAGE
- INTERNAL FREQUENCY COMPENSATION
- LATCH UP FREE OPERATION
- HIGH SLEW RATE : 16V/µs (typ)



N
DIP8
(Plastic Package)



D
SO8
(Plastic Micropackage)

P
TSSOP8
(Thin Shrink Small Outline Package)

DESCRIPTION

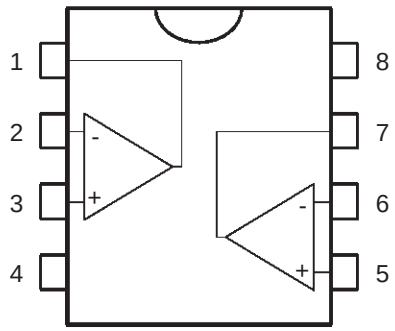
The TL082, TL082A and TL082B are high speed J–FET input dual operational amplifiers incorporating well matched, high voltage J–FET and bipolar transistors in a monolithic integrated circuit.

The devices feature high slew rates, low input bias and offset current, and low offset voltage temperature coefficient.

ORDER CODES

Part Number	Temperature Range	Package		
		N	D	P
TL082M/AM/BM	–55°C, +125°C	•	•	•
TL082I/AI/BI	–40°C, +105°C	•	•	•
TL082C/AC/BC	0°C, +70°C	•	•	•
Examples : TL082CD, TL082IN				

PIN CONNECTIONS (top view)



1 - Output 1
2 - Inverting input 1
3 - Non-inverting input 1
4 - V_{CC}^-
5 - Non-inverting input 2
6 - Inverting input 2
7 - Output 2
8 - V_{CC}^+

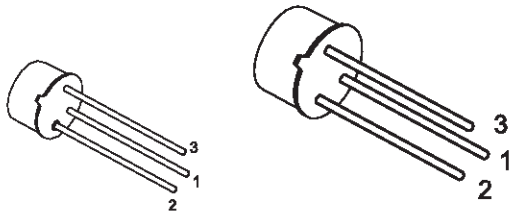
2N2219A
2N2222A

HIGH SPEED SWITCHES

DESCRIPTION

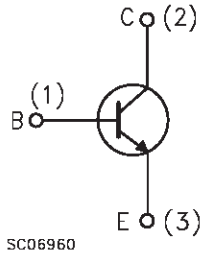
The 2N2219A and 2N2222A are silicon planar epitaxial NPN transistors in Jedec TO-39 (for 2N2219A) and in Jedec TO-18 (for 2N2222A) metal case. They are designed for high speed switching application at collector current up to 500mA, and feature useful current gain over a wide range of collector current, low leakage currents and low saturation voltage.

2N2219A approved to CECC 50002-100, 2N2222A approved to CECC 50002-101 available on request.



TO-18 **TO-39**

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CBO}	Collector-Base Voltage (I_E = 0)	75	V
V_{CEO}	Collector-Emitter Voltage (I_B = 0)	40	V
V_{EBO}	Emitter-Base Voltage (I_C = 0)	6	V
I_C	Collector Current	0.8	A
P_{tot}	Total Dissipation at $T_{amb} \leq 25\ ^oC$		
	for **2N2219A**	0.8	W
	for **2N2222A**	0.5	W
	at $T_{case} \leq 25\ ^oC$		
	for **2N2219A**	3	W
	for **2N2222A**	1.8	W
T_{stg}	Storage Temperature	-65 to 200	^oC
T_j	Max. Operating Junction Temperature	175	^oC