16-CHANNEL ANALOGUE MULTIPLEXER/DEMULTIPLEXER

The HEF4067B is a 16-channel analogue multiplexer/demultiplexer with four address inputs (A_0 to A_3), an active LOW enable input ($\overline{E}$), sixteen independent inputs/outputs (Y_0 to Y_{15}) and a common input/output (Z).

The device contains sixteen bidirectional analogue switches, each with one side connected to an independent input/output (Y_0 to Y_{15}) and the other side connected to the common input/output (Z).

With $\overline{E}$ LOW, one of the sixteen switches is selected (low impedance ON-state) by A_0 to A_3. All unselected switches are in the high impedance OFF-state. With $\overline{E}$ HIGH all switches are in the high impedance OFF-state, independent of A_0 to A_3.

The analogue inputs/outputs (Y_0 to Y_{15} and Z) can swing between V_{DD} as a positive limit and V_{SS} as a negative limit. V_{DD} to V_{SS} may not exceed 15 V.

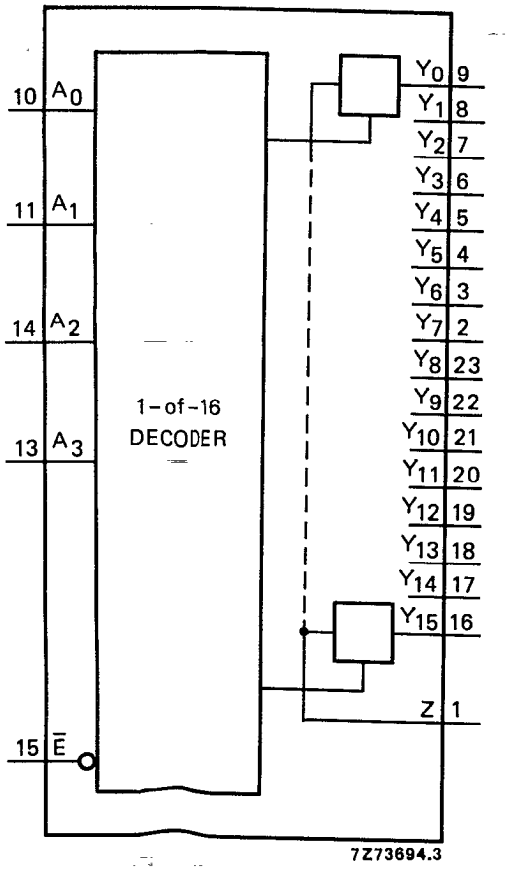

Fig. 1 Functional diagram.

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications

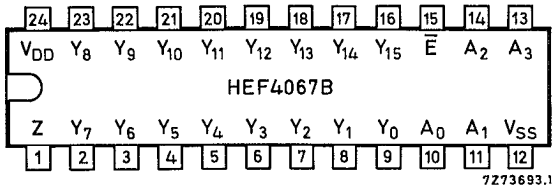

Fig. 2 Pinning diagram.

HEF4067BP(N): 24-lead DIL; plastic (SOT101-1)
HEF4067BD(F): 24-lead DIL; ceramic (cerdip) (SOT94)
HEF4067BT(D): 24-lead SO; plastic (SOT137-1)
( ): Package Designator North America

PINNING

Y_0 to Y_{15}	independent inputs/outputs
A_0 to A_3	address inputs
$\overline{E}$	enable input (active LOW)
Z	common input/output

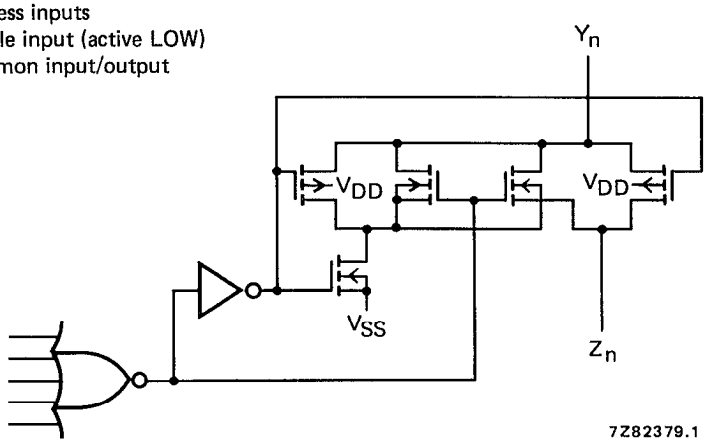

Fig. 3 Schematic diagram (one switch).

FUNCTION TABLE

inputs					channel
$\overline{E}$	A_3	A_2	A_1	A_0	ON
L	L	L	L	L	$Y_0 - Z$
L	L	L	L	H	$Y_1 - Z$
L	L	L	H	L	$Y_2 - Z$
L	L	L	H	H	$Y_3 - Z$
L	L	H	L	L	$Y_4 - Z$
L	L	H	L	H	$Y_5 - Z$
L	L	H	H	L	$Y_6 - Z$
L	L	H	H	H	$Y_7 - Z$
L	H	L	L	L	$Y_8 - Z$
L	H	L	L	H	$Y_9 - Z$
L	H	L	H	L	$Y_{10} - Z$
L	H	L	H	H	$Y_{11} - Z$
L	H	H	L	L	$Y_{12} - Z$
L	H	H	L	H	$Y_{13} - Z$
L	H	H	H	L	$Y_{14} - Z$
L	H	H	H	H	$Y_{15} - Z$
H	X	X	X	X	none

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

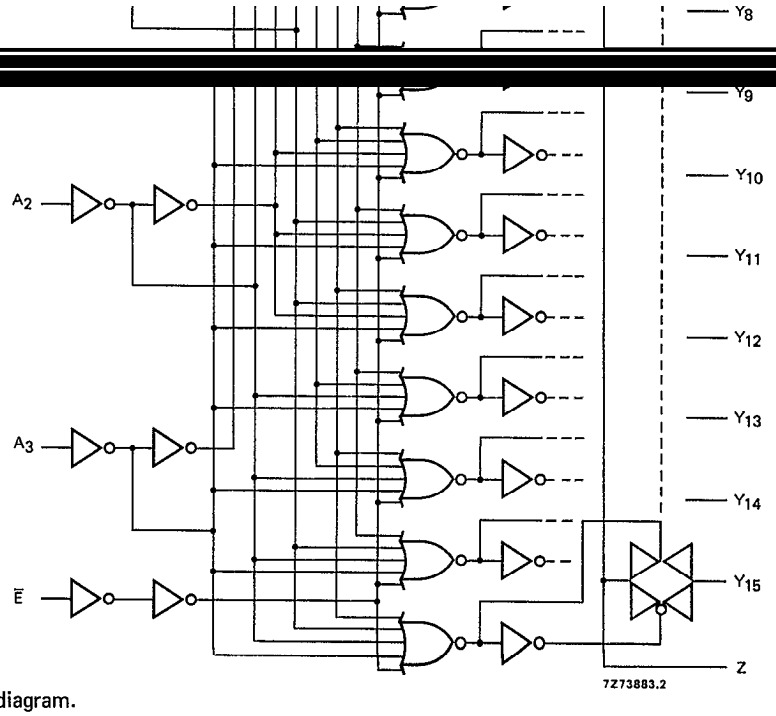

Fig. 4 Logic diagram.

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1\,100\ f_i + \Sigma(f_oC_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_oC_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$5\,000\ f_i + \Sigma(f_oC_L) \times V_{DD}^2$	
	15	$13\,300\ f_i + \Sigma(f_oC_L) \times V_{DD}^2$	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ.	max.		
Propagation delays						
$V_{is} \rightarrow V_{os}$ HIGH to LOW	5	t_{PHL}	30	60	ns	note 1
	10		15	25	ns	
	15		10	20	ns	
LOW to HIGH	5	t_{PLH}	25	50	ns	note 1
	10		10	20	ns	
	15		10	20	ns	
$A_n \rightarrow V_{os}$ HIGH to LOW	5	t_{PHL}	190	380	ns	note 2
	10		70	145	ns	
	15		50	100	ns	
LOW to HIGH	5	t_{PLH}	175	345	ns	note 2
	10		70	140	ns	
	15		50	100	ns	
Output disable times						
$\overline{E} \rightarrow V_{os}$ HIGH	5	t_{PHZ}	195	385	ns	note 3
	10		140	280	ns	
	15		130	260	ns	
LOW	5	t_{PLZ}	215	435	ns	note 3
	10		180	355	ns	
	15		170	340	ns	
Output enable times						
$\overline{E} \rightarrow V_{os}$ HIGH	5	t_{PZH}	155	315	ns	note 3
	10		70	135	ns	
	15		50	100	ns	
LOW	5	t_{PZL}	170	340	ns	note 3
	10		70	140	ns	
	15		50	100	ns	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ.	max.	
Distortion, sine-wave response	5		0,25	%	note 4
	10		0,04	%	
	15		0,04	%	
Crosstalk between any two channels	5		–	MHz	note 5
	10		1	MHz	
	15		–	MHz	
Crosstalk; enable or address input to output	5		–	mV	note 6
	10		50	mV	
	15		–	mV	
OFF-state feed-through	5		–	MHz	note 7
	10		1	MHz	
	15		–	MHz	
ON-state frequency response	5		13	MHz	note 8
	10		40	MHz	
	15		70	MHz	

NOTES

V_{is} is the input voltage at a Y or Z terminal, whichever is assigned as input.
V_{os} is the output voltage at a Y or Z terminal, whichever is assigned as output.

1. R_L = 10 kΩ to V_{SS}; C_L = 50 pF to V_{SS}; $\overline{E}$ = V_{SS}; V_{is} = V_{DD} (square-wave); see Fig. 7.
2. R_L = 10 kΩ; C_L = 50 pF to V_{SS}; $\overline{E}$ = V_{SS}; A_n = V_{DD} (square-wave); V_{is} = V_{DD} and R_L to V_{SS} for t_{PLH}; V_{is} = V_{SS} and R_L to V_{DD} for t_{PHL}; see Fig. 7.
3. R_L = 10 kΩ; C_L = 50 pF to V_{SS}; $\overline{E}$ = V_{DD} (square-wave);
   V_{is} = V_{DD} and R_L to V_{SS} for t_{PHZ} and t_{PZH};
   V_{is} = V_{SS} and R_L to V_{DD} for t_{PLZ} and t_{PZL}; see Fig. 7.
4. R_L = 10 kΩ; C_L = 15 pF; channel ON; V_{is} = ½ $V_{DD(p\text{-}p)}$ (sine-wave, symmetrical about ½ V_{DD}); f_{is} = 1 kHz; see Fig. 8.
5. R_L = 1 kΩ; V_{is} = ½ $V_{DD(p\text{-}p)}$ (sine-wave, symmetrical about ½ V_{DD}); $20 \log \frac{V_{os}}{V_{is}} = -50$ dB; see Fig. 9.
6. R_L = 10 kΩ to V_{SS}; C_L = 15 pF to V_{SS}; $\overline{E}$ or A_n = V_{DD} (square-wave); crosstalk is $|V_{os}|$ (peak value); see Fig. 7.
7. R_L = 1 kΩ; C_L = 5 pF; channel OFF; V_{is} = ½ $V_{DD(p\text{-}p)}$ (sine-wave, symmetrical about ½ V_{DD}); $20 \log \frac{V_{os}}{V_{is}} = -50$ dB; see Fig. 8.
8. R_L = 1 kΩ; C_L = 5 pF; channel ON; V_{is} = ½ $V_{DD(p\text{-}p)}$ (sine-wave, symmetrical about ½ V_{DD}); $20 \log \frac{V_{os}}{V_{is}} = -3$ dB; see Fig. 8.

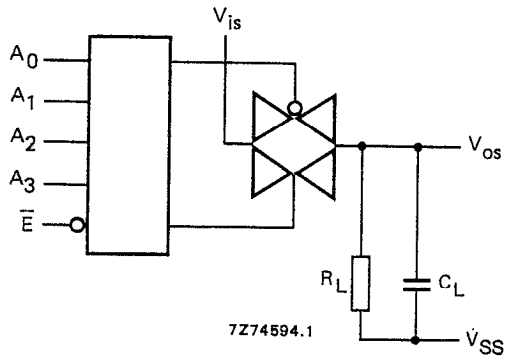

Fig. 7.

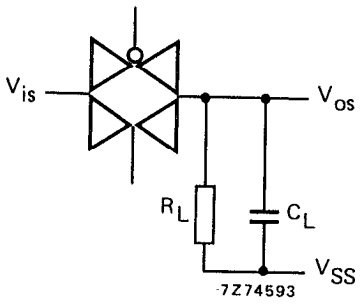

Fig. 8.

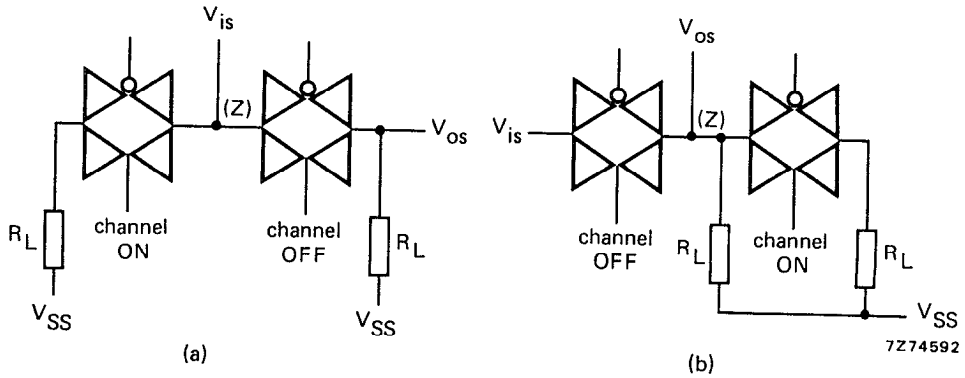

Fig. 9.

APPLICATION INFORMATION

Some examples of applications for the HEF4067B are:

- Analogue multiplexing and demultiplexing.
- Digital multiplexing and demultiplexing.
- Signal gating.

NOTE

If break before make is needed, then it is necessary to use the enable input.