Announcement

5th international conference on
thermal & mechanical simulation and experiments
in micro-electronics and micro-systems

EuroSimE 2004

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May 9 – May 12, 2004

Novotel Tour Noire
Brussels, Belgium

EuroSimE 2004 provides …
……7 courses given by professionals
……90 papers in 18 oral and 3 poster sessions
……exhibition and exhibitor presentations

Local organiser: Bart.Vandevelde@imec.be, Marion.Hegemann@imec.be (tel.: +32 16 281 849).

IEEE

IEEE COMPONENTS, PACKAGING AND MANUFACTURING TECHNOLOGY SOCIETY

Conference overview

Sunday	May 9, 2004	Short courses
8.30 – 9.00	Registration for short courses (IMEC-Leuven)	
9.00 – 12.30	C1: cancelled	
	C2: Application of static and dynamic compact thermal models for the thermal analysis of electronic parts (**M. Sabry**)	
	C4: Advanced optimization methods for design and qualification of microelectronics (**N. Tzannetakis, G.Q. Zhang**)	
	C6: Fundamentals of board-level assembly and solder joint reliability (**R. Lee**)	
	C8: Wafer level packaging technologies (**E. Beyne**)	
12.30 – 14.00	Lunch	
14.00 – 17.30	C1: cancelled	
	C3: Heat sink design and analysis for microelectronic equipment (**P. Rodgers**, **V. Eveloy**)	
	C5: Lead-free Solder Joints: Reliability Trends and Material Properties (**J-P. Clech**)	
	C7: Microvias and high density interconnects for advanced packaging (**R. Lee**)	
18.00	Bus to Novotel Brussels (conference location)	

Monday	May 10, 2004	Conference program, day 1
7.30 – 8.30	Registration	
8.30 – 10.40	Session 1: Industrial Trends	
10.40 – 11.10	Coffee break	
11.10 – 12.40	Session 2: Technology Developments	
12.40 – 14.20	Lunch	
14.20 – 15.50	Session 3: Virtual Thermal Mechanical Prototyping	
14.20 – 15.50	Session 4: Thermal Mechanical Behaviour on Wafer Level	
14.20 – 15.50	Session 5: Dynamic Compact Thermal and Electro-Thermal Models	
15.50 – 16.30	Coffee break	
16.30 – 18.00	Session 6: Experimental and Numerical Interaction	
16.30 – 18.00	Session 7: Modelling and Designing of Advanced Packaging	
16.30 – 18.00	Session 8: Thermal Behaviour Modelling and Characterization	
19.30 – 23.00	Gala dinner in “Roy d’Espagne”	

Tuesday	May 11, 2004	Conference program, day 2
8.30 – 10.20	Session 9: Advanced Numerical Simulation Methodologies	
8.30 – 10.20	Session 10: Small Scale Thermal and Fluid Aspects in Microsystems	
10.20 – 10.40	Coffee break	
10.40 – 11.30	Poster session 11, 12, 13.	
11.30 – 12.40	Session 14: Modelling of MEMS and Optical Devices	
11.30 – 12.40	Session 15: Simulation-Based Thermal Design Strategies	
12.40 – 14.10	Lunch	
14.20 – 16.10	Session 16: Solder Reliability Behaviour	
14.20 – 16.10	Session 17: CFD and FE Modelling of Thermal Performance	
16.10 – 16.30	Coffee break	
16.30 – 18.00	Special exhibitor session	
18.00 – 19.30	Cocktail party	

Wednesday	**May 12, 2004 Conference program, day 3**
8.30 – 10.00	Session 18: Micro- to Macro-Scale Thermal Design Challenges in Microelectronics
10.00 – 10.40	Coffee break
10.40 – 12.30	Session 19: Solder Fatigue
10.40 – 12.30	Session 20: Characterization and Modelling of Polymer behaviour
12.30 – 14.00	Lunch
14.00 – 16.00	Session 21: New Developments in Microelectronics Reliability
16.00	End of the conference

Sunday May 9, 2004: Short courses

Place and date : Leuven – (IMEC)

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14.00 – 17.30	C3: Heat sink design and analysis for microelectronic equipment (**P. Rodgers**, **V. Eveloy**)
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	C7: Microvias and high density interconnects for advanced packaging (**R. Lee**)
18.00	Bus to Novotel Brussels (conference location)

Attention!!! The location of the courses is different from the location of the conference.

Course description:

Course 1:	**Cancelled**

Course 2:	**Application of static and dynamic compact thermal models for the thermal analysis of electronic parts**
Instructor	**Mohamed-Nabil Sabry**, French University, Egypt
Introduction	The impact of thermal effects on both reliability and performance of electronic systems is no longer to be proved. Static and dynamic thermal effects in electronic circuits manifest themselves at all levels from device to system, with high impact on both reliability and performance of electronic systems, especially as the device feature size shrinks to the nano-scale. Progress in electronic systems has always been marked by a trend for smaller devices and hence larger systems in terms of number of devices. Breaking the barriers at both ends, small and large, is continuously creating new challenges for EDA industry. In fact, for small sizes, the electronic behaviour will be more affected by other physical phenomena such as thermal, electromagnetic and mechanical including quantum effects. This constitutes the first challenge. On the other hand, miniaturization enables us to construct systems containing millions, or perhaps billions, of different elements. Hence, modelling, simulating and moreover optimising these systems, is another challenge. It is evident that analysing a thermal problem in its full details, involving fluid dynamics, heat transfer by all modes (conduction, convection and radiation) including non-linear effects together with all the electronic details of the system is simply a fiction. Yet, electronic and thermal problems interfere at all levels, and we need to predict system performance and reliability before fabrication. Hence, new design methodologies have to be adopted based on top - down design approach. This is a “divide and conquer” approach, heavily relying on hierarchical sets of compact models at different levels of abstraction. Recent advances have been made to extend the relatively more mature understanding of static compact thermal models to the dynamic case. The wealth of knowledge accumulated has largely deserved a structured presentation in order to correctly grasp underlying physics as well as adequate methodologies to handle different problems according to their inherent nature as well as design needs and constraints.
Objectives	The course aims at giving attendees a rational and structured understanding of the nature of both compact models as well as physical problems they are intended to address, whether in static or dynamic regimes, in order to adequately build and use these compact models for the design and analysis of electro-thermal problems arising in electronic systems.

Course Outline	1. Introduction • When and why should we care about electro-thermal effects • Why should we use compact models • Place of compact models in simulation and design flow 2. Properties of a compact model • General forms for static and dynamic models • Constraints that must be satisfied by compact models, validity checks • Precision of a compact model 3. When should we use a dynamic compact model? • Slow dynamics • Fast dynamics 4. How compact models are constructed and used (static & dynamic) • Preliminary notes about lumping a distributed system • Structural assembly approach • Integral approach • The structure function • Modal approach 5. Special problems • Nonlinear problems, Radiation • Convection
Who should attend?	The course addresses the needs of engineers, scientists as well as technical strategic decision makers, involved in thermal management of electronic systems. Although the course presents most recent advances in the field of static and dynamic compact models with sufficient details to let this knowledge be operational in concrete applications, it does not assume prior knowledge of these issues and hence is of interest for both experts and new actors in this area..
About the instructor	Prof. Mohamed-Nabil Sabry is the dean of engineering faculty in the French University in Egypt. He holds a Doctorat es Sciences Degree from the National Polytechnic Institute in Grenoble, France 1984, about modeling and simulation of 3D convective problems and has been involved since then in thermal and electro-thermal issues at different levels both in academic and industrial context. He was formerly with Mentor Graphics where he was the engineering manager of analog simulation activities worldwide, as well as the French Nuclear Research Center. He also worked with different universities in France (INP-Grenoble) and in Egypt (Mansoura U., American U. and finally the French U.). For his publications on compact models, he was awarded the Harvey Rosten award of excellence in 2002. He is also member of the program committee of THERMINIC, a panel member in many international conferences (THERMINIC, VLSI Test Symposium) and a reviewer in many international scientific journals dealing with this subject (IEEE/CPT, IEEE/Electron Device letters, Microelectronics Journal, ASME/Journal of Electronic Packaging). His published works cover the whole spectrum of electro-thermal analysis from transistor level to system level.

Course 3:	**Heat sink design and analysis for microelectronic equipment**
Instructor	**Peter Rodgers**, CALCE Electronic Products and Systems Center, University of Maryland, USA **Valérie Eveloy**, Electronics Thermal Management Ltd., Ireland
Introduction	Heat sinks are the most common, cost-effective hardware employed for the thermal management of microelectronic equipment, with applications spanning from microchannel cooling to component- and circuit board thermal control. Heat sinks function by extending the surface area of heat dissipating surfaces through the use of fins. Their design and analysis is one of the most extensive research areas in electronics cooling. Ever-rising electronic component power dissipation, combined with both the demand for more compact and lighter equipment, and manufacturing constraints, place increasing challenges on the optimisation of heat sink thermal performance today. This is compounded by shortening product design cycle times, which heighten the requirement for innovative thermal design methods enabling accurate heat sink designs to be generated and quickly assessed. An efficient thermal design process involves the use of analytical and semi-empirical calculations to establish an initial heat sink design, which is refined by numerical analysis to account for the impact of the application environment on thermal performance. The effectiveness of the heat sink design ultimately needs to be verified by experimentation. The course provides an overview of the state-of-the-art and general trends in heat sink design. Apart from convective and radiative heat transfer optimisation, the course addresses key issues in advancing heat sink thermal performance, including contact thermal resistance, integration of heat spreading technologies and entropy minimisation. Practical case studies dealing with heat sink design optimisation are presented.
Objectives	This course provides a comprehensive treatment of the design and analysis of heat sinks. It combines theoretical and practical information to successfully design or select cost-effective heat sinks for microelectronic equipment. The attendee will gain an appreciation of both the fundamental performance limits of heat sinks, and current state-of-the-art in heat sink technology.

Course Outline	1. Introduction • Fundamentals of heat transfer: conductive, convective and radiative heat transfer processes • Thermal analysis and design process: Application of analytical, experimental and numerical analyses, overview of the latest commercial thermal design software packages • Heat dissipation trends in electronic systems: heat transfer chain, limits of air-cooling: passive versus active 2. Evolution of Heat Sink Design and Analysis • Analytical analysis: Fin efficiency, Radiative heat transfer models • Experimentation: derivation of correlations for the convective heat transfer coefficient as a function of heat sink geometry and convective environment; friction factor correlations • Numerical analysis: Investigation of thermofluid phenomena: Use of Computational Fluid Dynamics (CFD) methods to predict heat sink performance in application environment • Heat sink design optimisation Fin geometry: fin spacing and thickness as a function of heat sink rectilinear volume and given convective environment Manufacturability: fin aspect ratio, production cost Entropy minimisation methodology: energy and material consumed in the fabrication and operation of heat sink • Key observations from past work 3. Heat Sink Technologies • Types of heat sink designs Straight, staggered, pin and amorphous fin designs Porous designs: foams, weave-screen laminates Passive and active heat sinks Forced-air cooling: side entrance inlet flow versus impingement flow • High-performance heat sink designs Augmented, bonded, folded, forged and cast designs • Survey of future trends on heat sink performance Limits of air-cooling; Manufacturability constraints 4. Current Design and Analysis Methods for Air-Cooled Heat Sinks • Heat sink characterisation Vendor characterisation methods of heat sink performance and their limitations Heat sink selection: how to select a heat sink from manufacturer catalogues • Customised heat sink design Environmental and physical conditions; Initial feasibility study Preliminary heat sink design Heat sink optimisation: Convective and radiative performance; Conductive performance (Fin efficiency, heat spreading: heat pipes, vapour chambers, improved thermal conductivity materials), design for manufacturability, least-energy optimisation 5. Current Design and Analysis Methods for Air-Cooled Heat Sinks (Cont'd) • Heat sink attachment: contact thermal resistance and interface materials, properties of interface materials; Types of interface materials • Airflow management Fan performance Fan/blower/impeller selection; Assessment of vendor specified fan curve performance Change in fan curve characteristics due to application environment Effect of grille and filter open area on system impedance • Compact modelling of heat sink thermofluid characteristics for system-level numerical analysis 6. Case studies: heat sink design and application • Microprocessor cooling • Telecommunication cabinet unit cooling 7. Summary
Who should attend?	The course will benefit engineers, managers and scientists involved in the thermal management or reliability of electronic systems. It is aimed at participants with varying expertise levels in thermal management, from novice to advanced.

About the instructor	**Dr. Peter Rodgers** is an Assistant Research Professor at the University of Maryland, College Park, where he supports the thermofluid research of the CALCE Electronic Products and Systems Center. He holds a Ph.D. degree in mechanical engineering from the University of Limerick, Ireland and has extensive experience of electronic equipment thermal design and characterisation. He was formerly with Electronics Thermal Management Ltd., Ireland, and the Nokia Research Center, Finland, where he consulted on electronics cooling. He is recipient of the 1999 Harvey Rosten Award for Excellence, awarded for his publications on the application of CFD analysis to electronics thermal design. Other research interests include the design of high-performance heat sinks, and the development of advanced experimental techniques to characterise thermofluid phenomena in electronic systems. He is a participant in the JSME Project, "Design and Manufacture of High-Performance Heat Sinks for Microelectronic Equipment". He is a member of several international conference program committees and has authored or co-authored approximately forty conference and journal publications on a broad range of topics related to electronics cooling. He has been an invited lecturer, track- and session chair and panelist at international conferences. **Dr. Valérie Eveloy** is with Electronics Thermal Management Ltd., a research and consulting firm specialized in electronics cooling. She has been involved in electronics cooling for nine years, and was previously a Research Engineer with the Nokia Research Center, Finland, where her activities focused on the thermal management of telecommunication products and the selection of RF IC packaging solutions. She has authored or co-authored over twenty five conference and journal publications, holds an M.Sc. degree in physical engineering from the National Institute of Applied Science (INSA), France, and a Ph.D. degree in mechanical engineering from Dublin City University, Ireland.

Course 4:	**Advanced optimisation methods for design and qualification of microelectronics**
Instructor	**Nick Tzannetakis**, NOESIS, Belgium **Kouchi Zhang**, Philips, The Netherlands
Background & relevancy	The rapid technological development trends of microelectronics and microsystems are mainly characterized by miniaturization down to nano-scale, increasing levels of technology/function integration and eco-design, while the business trends are mainly characterized by cost reduction, shorter time-to-market and outsourcing. These trends lead to increased chances and consequences of failures, increased design complexity, decreased product development and qualification times, dramatically decreased design margins and increased difficulties to meet quality, robustness and reliability requirements. To achieve competitive product/process development and manufacturing excellence, it is vital to know and to apply the advanced optimization methods for design and qualification of microelectronics.
Course Outline	1. Development trends of Microelectronics and Microsystems 2. The state-of-the-art of design and qualification of microelectronics 3. Basic theories of advanced optimization methods and tools 4. Exposure to Process Integration Techniques supporting the application of the advanced optimization on industrial problems 5. Case studies including software demonstrations 6. Challenges and future development and perspectives
What You Will Learn	This half-day course provides the participants with a unique chance to learn both the overview on the state-of-the-art methodologies, and the detailed ways of working & applications via both basic theory and case studies. The added business values will also be demonstrated.
Who should attend?	Microelectronics design engineers, reliability engineers, product/process developers and managers, thermal and mechanical analysts, researchers, graduates, PhD students and postdoc.
About the instructor	**Nikolas Tzannetakis** (1960) acquired an MSc. degree in Mechanical Engineering (1985) and an MSc. In Aerospace Engineering (1991) from the University of Michigan (USA). From 1985 to 1990 he worked in various positions in the area of structural analysis and optimization. From 1990 to 1996 he worked exclusively in the area of application of design optimization methods to industrial design applications. From 1996 to 1999 he served as the Product Manager of LMS OPTIMUS, at LMS International, working in the development, promotion and management of the software package. From 1999 until 2003 he managed the development of LMS Virtual.Lab Integrated Simulation software package. He is now the Chief Technical Officer of NOESIS Solutions a company focusing in the area of Process Integration and Design Optimization. He has published over 20 papers in the area of Process Integration and Design Optimization with emphasis in design optimization and robustness and reliability approaches in design. Beside his responsibilities in Technical University of Eindhoven, **Prof. Dr. G.Q. Zhang** is a principal scientist and technology domain leader at Philips (CFT) Centre For Industrial Technology, The Netherlands. Prof. Zhang is author and co-author for more than 100 scientific publications, including journal and conference papers, book and invited keynote lectures. His scientific interests include virtual prototyping and virtual qualification, development of fundamental and application knowledge of computational & experimental mechanics, advanced optimization methods and reliability engineering, and especially their applications in microelectronics, Microsystems and nanotechnology.

Course 5:	**Lead-free Solder Joints: Reliability Trends and Material Properties**
Instructor	**Jean-Paul Clech**, EPSI Inc., USA
Course Outline	○ Material properties (incl. physical properties, creep data in tension and shear…): Sn-Ag, Sn-Ag-Cu. ○ Creep deformations and creep rupture: temperature-dependent activation energy, effect of alloy composition on mechanical properties. ○ Fatigue curves, failure modes. ○ Thermal cycling reliability data: 100% lead-free data (Sn-Ag-Cu), mixed assemblies (SnPb balls + lead-free paste; SAC balls + HASL); data for leadless components (LCCC, discretes), leaded packages, BGA (PBGA, CCGA, CBGA), CSPs, Flip-Chip with & without underfill. ○ Impact of components and test conditions on the relative reliability of lead-free versus SnPb assemblies. ○ Effect of component and board finish on lead-free solder joint life (thermal cycling & drop test). ○ On-going developments: acceleration factors, constitutive modeling, life prediction models.
What You Will Learn	Solder joint reliability issues, which are well understood for SnPb assemblies, have been compounded by the introduction of lead-free and mixed (lead-free + SnPb) assemblies, limited field experience with lead-free solders, and ever more demanding end-use reliability requirements. The thermo-mechanical properties of Sn-Ag-Cu based alloys are also quite different from those of conventional SnPb. It is thus critical to understand what factors affect both the properties and the long term reliability of lead-free solders. This workshop provides an analysis and synthesis of the latest reliability information for popular lead-free alloys such as Sn-Ag-Cu (SAC). The performance of lead-free assemblies is put in perspective with that of SnPb assemblies. Material properties and fatigue curves are presented in an attempt to explain differences in the reliability of, and in the acceleration factors for SnPb and lead-free assemblies. The significance and the effect of alloy composition on thermo-mechanical properties is also discussed. Accelerated test results are presented for common components assembled onto circuit-boards using lead-free solder: leadless ceramic chip carriers, resistors, leaded packages, CBGA, CCGA, PBGA, flip-chip (with and without underfill), chip scale and wafer scale packages. Reliability risks are quantified for mixed assembly circuit-boards (lead-free + SnPb). Effects of common board (HASL, Ni/Au, OSP) and component finish are also discussed. The surveyed data indicates a strong dependence of lead-free solder joint reliability on component type, CTE mismatch as well as test conditions. In addition to the workshop slides, the hand-outs include an extensive list of references on lead-free solder mechanical properties and joint reliability.
Who should attend?	Circuit board designers, packaging engineers, design, manufacturing, quality or reliability professionals and managers who are responsible for, or plan to implement lead-free assembly technologies in their companies' products. Engineers and scientists involved in solder alloy development and characterization.
About the instructor	**Jean-Paul Clech** has over 18 years of practical experience in SMT quality and reliability assurance. He maintains one of the largest databases of solder joint reliability failures in the industry and is constantly challenged by problems brought about by new and emerging technologies. His current research interests are in BGA, CSP, flip-chip and lead-free assembly reliability. Jean-Paul is the founder of EPSI Inc. in Montclair, NJ. His responsibilities include technical consultation and problem solving for clients across the electronics industry and the development of engineering tools and training programs to prevent or solve reliability problems in electronics packaging and assembly. He is the principal developer of the "Solder Reliability Solutions" model and application software. He previously was Manager of Electronic Packaging at a European super-computer start-up, a Member of the Technical Staff and then consultant at AT&T Bell Labs. Jean-Paul received the Diplôme d' Ingénieur from Ecole Centrale de Paris, France (Materials Science major), and the M.S. and Ph.D. degrees in Mechanical Engineering from Northwestern University, Evanston, IL. His technical interests include thermal, mechanical, structural and fatigue behavior of electronic materials, packages and assemblies, and the application of engineering principles to the physical design and manufacturing of electronic systems. He is the author of over thirty-five technical papers, a frequent speaker at technical conferences, and has been an invited lecturer and workshop instructor at universities and corporations in Asia, Europe and North America. He is an active member of ASME, IEEE, IMAPS, TMS and SMTA.

Course 6:	Fundamentals of board-level assembly and solder joint reliability
Instructor	**Ricky Lee**, Hong Kong University of Science and Technology, Hong Kong
Outline	Introduction to soldering and surface mount technology (SMT); materials and processes for solder bumping; solder ball shear strength tests and analyses; printed circuit board (PCB) assemblies; destructive and non-destructive inspection methods; board level reliability under thermo-mechanical loading; accelerated temperature cycling tests; mechanical drop tests; computational and experimental mechanics for solder joint reliability; lead-free solder issues; design for reliability and environment.
Description	One of the major tasks of microelectronic packaging is to provide the ICs and components with passages for I/O signals, power, and ground. The interconnections between the chip and the substrate, and between the package and the printed circuit board are very critical to the electronics manufacturing industries. This workshop is aimed at providing comprehensive information on the most significant development and latest technologies for SMT solder joint interconnections in microelectronic packaging. During the course of this workshop, the topics listed in the outline will be discussed in great details. Emphases will be placed on the materials, processes, inspection, testing, analysis, and reliability issues. From this workshop, the attendees will acquire a profound understanding in the most significant issues for board level assemblies and solder joint reliability.
About the instructor	Ricky Lee received his Ph.D. degree from Purdue University in 1992. Currently, he is Associate Professor of Mechanical Engineering and Director of EPACK Lab at HKUST. He also sits on the Editorial Advisory Board of two international journals and is serving as Associate Editor for IEEE Transactions on Components & Packaging Technologies and IEEE Transactions on Advanced Packaging. Ricky is an ASME Fellow and a senior member of IEEE. He was Vice-Chair of Hong Kong Section, ASME International (1997 & 1998) and Chair of Hong Kong Chapter, IEEE-CPMT Society (2001 & 2002). Currently he is an Executive Committee Member of ASME-EPPD and a member of Board of Governors, IEEE-CPMT. Ricky has served as Track Organizer and Session Chair for many international conferences and he is a member of Program Committee (Interconnections) of ECTC. Besides, he has been invited to deliver short courses and seminars around the world (including ECTC, NEPCON-West and SEMICON-Singapore/Taiwan). Ricky has published numerous technical papers in international journals and conference proceedings, and is the co-author of three books- Chip Scale Packages (CSP): Design, Materials, Process, Reliability, and Applications; Microvias for Low-Cost High Density Interconnects; and Electronics Manufacturing with Lead-Free, Halogen-Free, and Conductive-Adhesive Materials. Furthermore, he is the two-time recipient (2000 & 2001) of JEP Best Paper Award, ASME Transactions: Journal of Electronic Packaging.

Course 7:	Microvias and high density interconnects for advanced packaging
Instructor	**Ricky Lee**, Hong Kong University of Science and Technology, Hong Kong
Objectives	This course will introduce the cutting-edge information on the most important development and latest research results in applying microvias and high density interconnect technologies to advanced packaging. For professionals active in microelectronic packaging research and development, those who wish to master high density interconnect technologies, and those who need to choose a cost effective design and highyield manufacturing process for their electronic systems, this is a timely summary of progress in all aspects of this fascinating field. The lecture contents are based on the instructor's books on electronic packaging, his recent research results, and interactions with the packaging and assembly industries. The scope of course covers flip chip and CSP technologies, wafer-level packaging, microvias and build-up substrates, and emerging high-density interconnect technologies. With the information provided in this lecture, the attendees will acquire a practical understanding in the design, materials, processes, analysis, and reliability issues of high-density interconnection technologies.
Course Outline	• Overview of area array and high density interconnect technologies • Solder-bumped flip chip & wafer level chip scale packages • Formation of microvias on silicon wafer • Formation of microvias on organic substrate • Copper-plated and conductive paste/ink-filled microvias • Special high density interconnect technologies • PCB/substrate with sequential build-up layers • Reliability Issues of High Density Interconnects
Who should attend?	This short course is intended for research scientists, professional engineers and technical managers who are involved in IC packaging, component assembly, materials and processing, contract manufacturing and marketing

About the instructor	**Ricky Lee** received his Ph.D. degree from Purdue University in 1992. Currently, he is Associate Professor of Mechanical Engineering and Director of EPACK Lab at HKUST. He also sits on the Editorial Advisory Board of two international journals and is serving as Associate Editor for IEEE Transactions on Components & Packaging Technologies and IEEE Transactions on Advanced Packaging. Ricky is an ASME Fellow and a senior member of IEEE. He was Vice-Chair of Hong Kong Section, ASME International (1997 & 1998) and Chair of Hong Kong Chapter, IEEE-CPMT Society (2001 & 2002). Currently he is an Executive Committee Member of ASME-EPPD and a member of Board of Governors, IEEE-CPMT. Ricky has served as Track Organizer and Session Chair for many international conferences and he is a member of Program Committee (Interconnections) of ECTC. Besides, he has been invited to deliver short courses and seminars around the world (including ECTC, NEPCON-West and SEMICON-Singapore/Taiwan). Ricky has published numerous technical papers in international journals and conference proceedings, and is the co-author of three books- Chip Scale Packages (CSP): Design, Materials, Process, Reliability, and Applications; Microvias for Low-Cost High Density Interconnects; and Electronics Manufacturing with Lead-Free, Halogen-Free, and Conductive-Adhesive Materials. Furthermore, he is the two-time recipient (2000 & 2001) of JEP Best Paper Award, ASME Transactions: Journal of Electronic Packaging.

Course 8:	**Wafer level packaging technologies**
Instructor	**Eric Beyne**, IMEC, Belgium
Course Outline	1. Introduction Impact of the IC-roadmaps on interconnection and packaging technologies Traditional packaging approaches System-in-a-package technology Wafer-level packaging (WLP) techniques - definitions 2. Wafer level packaging technologies Flip chip technology Wafer level redistribution technologies Chip-sized package technologies with overview of different industrial appoaches 3. Electrical considerations in WLP Electrcial parasitics package level interconnects 4. Thermo-mechanical considerations Impact on reliability solder joints Impact on reliability redistribution metallisation Technology & FEM co-design for improved reliability 5. Thermal considerations 6. Economic aspects 7. Summary

Monday May 10, 2004: Technical programme day 1

7.30	**60**	**Registration**

8.30		**Start Monday Morning Sessions**

		Opening Session
8.30	**10**	**Opening**

Session 1:		**Keynote session: Industrial Trends**
8.40	**30**	**Keynote: Roadmap Challenges – There is More than Moore** ***A. J. van Roosmalen*** *Philips Semiconductors, Eindhoven, the Netherlands*
9.10	**30**	**Keynote: Opportunities and Challenges for Telecommunications Technology** ***J. Rantala*** *Nokia Research Center, Helsinki, Finland*
9.40	**30**	**Keynote: Trends in automotive electronics** ***H. Casier*** *AMI Semiconductor Belgium BVBA, Oudenaarde, Belgium*
10.10	**30**	**Keynote: Trends & Challenges in Microsystems Packaging** ***M. K. Iyer*** *Microsystems, Modules & Components Lab, Institute of Microelectronics (IME), Singapore*

10.40	**30**	**Break**

Session 2:		**Keynote session: Technology Developments**
11.10	**30**	**Keynote: Nano-electronics in Biological Applications** ***G. Borghs*** *IMEC, Leuven, Belgium*
11.40	**30**	**Keynote: Reliability Challenges and Recent Advances for Cu Interconnects** ***Paul S. Ho[a*], Ki-Don Lee[b], Sean Yoon[a], Guotao Wang[a]*** *[a]Laboratory for Interconnect and Packaging, University of Texas at Austin, USA* *[b]Silicon Technology Development, Texas Instruments, Inc., Dallas, USA*
12.10	**30**	**Keynote: From Macro-Cooling to Micro-Reliability** ***M.R.D. Davies*** *Stokes Research Institute, University of Limerick, Ireland*

12.40	**100**	**Lunch**

14.20		Monday Afternoon Sessions

	Parallel sessions				
14.20-15.50	Session 3		Session 4		Session 5
	Virtual Thermal Mechanical Prototyping		Thermal Mechanical Behavior on Wafer Level		Dynamic Compact Thermal and Electro-Thermal Models

Session 3:		Virtual Thermal Mechanical Prototyping
14.20	30	Keynote: **Modeling of Cure-Induced Warpage of Plastic IC Packages** ***D.G. Yang[1], K.M.B. Jansen[1], L.J. Ernst[1], G.Q. Zhang[2], W.D. van Driel, H.J.L. Bressers[3]*** *[1)]Delft University of Technology, The Netherlands,* *[2)]Philips-CFT, Eindhoven, The Netherlands* *[3)]Philips Semiconductors, Nijmegen, The Netherlands*
14.50	20	**Thermo-Mechanical Stress Modelling of MOS Device with Electro- thermal Considerations** ***P. Tounsi[*], J.P. Fradin[***], X. Chauffleur[***], Ph. Dupuy[**], J.M. Dorkel[*], A. Marty*,A. Deram[**]*** *[*)] LAAS/CNRS, Toulouse Cedex, France* *[**)] MOTOROLA Semiconducteurs SA, Toulouse Cedex, France* *[***)] EPSILON Ingénierie, California, Labège Cedex, France*
15.10	20	**FEM-based Method to Determinate Mechanical Stress Evolution during Process Flow in Microelectronics – Application to Stress-Voiding** ***S. Orain[1], J.C Barbé[2], X. Federspiel[1], P. Legallo[3], H. Jaouen[4]*** *[1)] PHILIPS semiconductors, Crolles cedex ; France* *[2)] CEA-DRT-LETI/DTS, Grenoble Cedex, France* *[3)] CEA-DRT/DTEN, Grenoble Cedex, France* *[4)] STMicroelectronics, Crolles Cedex, France*
15.30	20	**On Wire Failures in Micro-electronic Packages** ***W.D. van Driel[1], J.H.J. Jansen , G.Q. Zhang[2],M.A.J. van Gils[2], R.B.R. van Silfhout[2], L.J. Ernst[3]*** *[1)] ATO Innovation/Philips Semiconductors, Nijmegen, The Netherlands* *[2)] Center for Industrial Technology/Philips, Eindhoven, The Netherlands* *[3)] Delft University of Technology, 2628 CD Delft, The Netherlands*

Session 4:		Thermal Mechanical Behavior on Wafer Level
14.20	30	Keynote: **A Finite Element Study of Process Induced Stress in the Transistor Channel: Effects of Silicide Contact and Gate Stack** ***C.Torregiani[1,2], J. Liu[3], B.Vandevelde[1], D.Degryse[1], M.J.Van Dal[4], A. Benedetti, A.Lauwers[1], K.Maex[1,2].*** *[1)] IMEC, Leuven, Belgium; [2)] E.E. Dept. K.U.Leuven, Leuven, Belgium* *[3)] E.E. Dept. Stanford University, Stanford, California, USA* *[4)] Philips Research Leuven, Leuven, Belgium*
14.50	20	**Effect of Metal Layout Design on Passivation Crack Occurrence using both Experimental and Simulation Techniques** ***R.B.R van Silfhout[1)], W.D. van Driel[2)], Y.Li[2)], M.A.J. van Gils[1)], J.H.J. Janssen[2)], G.Q. Zhang[1)], G. Tao[2)], J. Bisschop[2)], L.J. Ernst[3)]*** *[1)] Philips Centre for Industrial Technology, Eindhoven, The Netherlands* *[2)] Philips Semiconductors, ATO Innovation, Nijmegen, The Netherlands* *[3)]Delft University of Technology, The Netherlands*
15.10	20	**Probability of Silicon Fracture in Molded Packages** ***C. Bohm*, T. Hauck*, W. H. Müller**, A. Juritza*** *[*)] Motorola GmbH, Schatzbogen 7, 81829 München* *[**)] Technische Universität Berlin, Einsteinufer 5, 10587 Berlin*
15.30	20	**Interfacial Sliding and Plasticity in Back-end Interconnect Structures of Microelectronic devices** ***I. Dutta[1], D. Pan, C. Park[1], J. Vella[2]*** *[1)] Center for Materials Science and Engineering, Department of Mechanical Engineering, Naval Postgraduate School, Monterey, CA, USA* *[2)] Process and Materials Characterization Laboratory, Motorola, Tempe, AZ, USA*

Session 5:		Dynamic Compact Thermal and Electro-Thermal Models
14.20	30	**Keynote: Empirical Validation of Thermal Dynamics in a Silicon Microthruster: Influence of the Boundary Conditions** ***M. Salleras, I. García, J. Palacín, M. Puig, J. Samitier, S. Marco*** *Sistemes d'Instrumentació i Communicacions, Departament d'Electrònica, Universitat de Barcelona, Spain*
14.50	20	**Compact Electro-thermal Models of Semiconductor Devices with Multiple Heat Sources** ***C. Bohm, T. Hauck, E.B. Rudnyi, J. G. Korvink*** *Motorola, Germany IMTEK, University of Freiburg, Germany*
15.10	20	**Electro-Thermal Transistor Models in the SISSI Electro-Thermal IC Simulator** *V.Székely, A.Poppe, G.Hajas* *Budapest University of Technology and Economics, Hungary*

15.50	40	Break

	Parallel sessions				
16.30-18.00	Session 6		Session 7		Session 8
	Experimental and Numerical Interaction		Modeling and Designing of Advanced Packaging		Thermal Behavior Modeling and Characterization

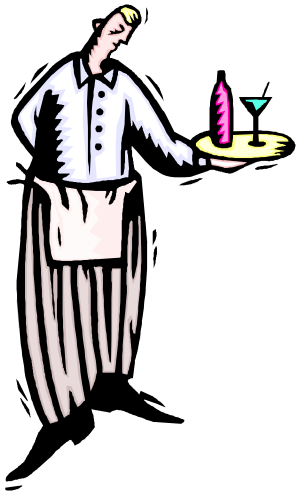
Session 6:		Experimental and Numerical Interaction
16.30	30	**Keynote: Computational Model Validation with Experimental Data from Temperature Cycling Tests of PBGA Assemblies for the Analysis of Board Level Solder Joint Reliability** ***R. Lee, D. Lau*** *Electronic Packaging Laboratory, Department of Mechanical Engineering* *Hong Kong University of Science & Technology, Hong Kong*
17.00	20	**PWB Warpage Analysis and Verification using an AP210 Standards-based Engineering Framework and Shadow Moiré** ***D. Zwemer[1], S. McCarron[1], A. Spradling[1],R. Peak[2], M. Bajaj[2],T. Thurman[3],*** ***M. Dickerson[4], L. Klein[5], G. Liutkis[5],K. Brady[6], J. Messina[6]*** *[1)] AkroMetrix LLC, USA* *[2)] Georgia Institute of Technology, USA* *[3)] Rockwell Collins, USA* *[4)] InterCAX LLC, USA* *[5)] LKSoft, USA* *[6)] NIST, USA*
17.20	20	**Novel Numerical and Experimental Analysis of Dynamic Responses under Board Level Drop Test** ***Tong Yan Tee [a], Jing-en Luan [a], Eric Pek [b], Chwee Teck Lim [b], Zhaowei Zhong [c]*** *[a] STMicroelectronics, Singapore* *[b] National University of Singapore, ME Dept, Singapore.* *[c] Nanyang Technological University, School of MPE, Singapore.*
17.40	20	**Finite Element Modelling of Crack Detection Tests** ***S Ridout[1] , M Dusek[2] , C Bailey[1], C Hunt[2]*** *[1)] Centre for Numerical Modelling and Process Analysis, University of Greenwich, Greenwich, UK* *[2)] NPL Materials Centre, National Physical Laboratory,, Teddington, UK*

Session 7:		Modeling and Designing of Advanced Packaging
16.30	**30**	**Keynote: Design, Fabrication and Comparison of Lead-Free/Eutectic Solder Joint Reliability of FlipChip Package** ***Chih-Tang Peng, Kuo-Ning Chiang, Terry Ku, Kenny Chang*** *National Tsing Hua University, Taiwan*
17.00	**20**	**Virtual Qualification of Moisture Induced Failures of Advanced Packages** ***M.A.J. van Gils[1], W.D. van Driel[2], G.Q. Zhang[3], H.J.L. Bressers[2], R.B.R. van Silfhout[1], X.J. Fan[4], J.H.J. Janssen[2]*** *[1)] Philips Center for Industrial Technology, Eindhoven, The Netherlands* *[2)] ATO Innovation/Philips Semiconductors, Nijmegen, The Netherlands* *[3)] Technical University of Eindhoven, Eindhoven, The Netherlands* *[4)] Philips Research-USA, Briarcliff Manor, New York, USA*
17.20	**20**	**Finite Element Analysis of an Improved Wafer Level Package using Silicone Under Bump (SUB) Layers** ***M. Gonzalez[1], M. Vanden Bulcke[1], B. Vandevelde[1], E. Beyne[1], Y. Lee[2], B. Harkness[2], H. Meynen[2]*** *[1]IMEC, Leuven, Belgium* *[2]Dow Corning Corporation*
17.40	**20**	**Crack and Delamination Risk Evaluation of Thin Silicon Applications based on Fracture Mechanics Approaches** ***J. Auersperg [1,2], D. Vogel[1], B. Michel[1]*** *[1)] Fraunhofer Institute for Reliability and Microintegration Berlin (IZM), Dept. Mechanical Reliability and Micro Materials, Berlin, Germany* *[2)] AMIC Angewandte Micro-Messtechnik GmbH, Berlin, Germany*

Session 8:		Thermal Behavior Modeling and Characterization
16.30	30	Keynote: **Numerical Simulation and Experimental Verification of the Thermal Contact Properties of the Polymers Bonds** ***T. Fałat, A. Wymysłowski, K. Friedel, J.Felba*** *Wrocław University of Technology, Poland*
17.00	20	**Experiments on Behaviour of Power Silicon PN Junctions under Reverse Bias Voltage at High Temperature** ***V.V.N. Obreja[1], C. Codreanu[1], K. Nuttall[2], O. Buiu[2]*** *[1)] National R&D Institute for Microtechnology, Romania* *[2)] Liverpool University, UK*
17.20	20	**Parameter Calibration on Post-ion-implantation Dopant Diffusions** ***J. Fu , W.Crans[2], W.J. Eijsenga[2]*** *[1)] X-FAB Semiconductor Foundries, Erfurt, Germany* *[2)] TU Delft, ITS-Faculty/DIMES, Electronic Components, Technology and Materials (ECTM)-Lab, Delft, The Netherlands*

18.00		End of 1st day Technical Sessions

19.30		Gala dinner in Roy d'Espagne (Great Market place in heart of Brussels)



Tuesday May 11, 2004: Technical programme day 2

8.30		Start Tuesday Morning Sessions

	Parallel sessions		
8.30-10.20	Session 9		Session 10
	Advanced Numerical Simulation Methodologies		Small Scale Thermal and Fluid Aspects in Microsystems

Session 9:		Advanced Numerical Simulation Methodologies
8.30	30	Keynote: **Automated FEM Mesh Optimization for Nonlinear Problems Based on Error Estimation** ***S. Rzepka*** *Infineon Technologies SC 300 Dresden, MDC RM, Dresden, Germany*
9.00	20	**Advanced Numerical Prototyping Methods in Modern Engineering Applications** ***W.D. van Driel[1], J. van de Peer[3], N. Tzannetakis[3], A. Wymysłowski[4], G.Q. Zhang[2]*** *[1)] ATO Innovation/Philips Semiconductors, Nijmegen, The Netherlands* *[2)] Center for Industrial Technology/Philips, Eindhoven, The Netherlands* *[3)] Noesis, Leuven, Belgium* *[4)] Wroclaw University of Technology, Wroclaw, Poland*
9.20	20	**Reliability-Based Design Optimization for Land Grid Array Solder Joints Under Thermo-Mechanical Load** ***Zhenxue Han[1], Bo Wang[1], Leon Xu[2], Tommi Reinikainen[2],Ren Wei[2]*** *[1)] University of Texas at Arlington, USA* *[2)] Nokia, USA*
9.40	20	**Finite Element Analysis of Ultra Thin BGA Package: First and Second Level Reliability** ***P. Limaye[1], B. Vandevelde[1], H. deVries[2], D. Degryse[1], K. Slob[2], C. van Veen[2], R. Labie[1]*** *[1)] IMEC, Leuven, Belgium* *[2)] Philips CFT (Eindhoven), The Netherlands*
10.00	20	**Application of Simulation-based Decision Making in Product Development of an RF Module** ***M. Lindgren[1,2], I. Belov[2], M. Törnvall[1], P. Leisner[2,3],*** *[1)] Kitron Development AB, Jönköping, Sweden* *[2)] School of Engineering, Jönköping university, Sweden* *[3)] Acreo AB, Jönköping, Sweden*

Session 10:		Small Scale Thermal and Fluid Aspects in Microsystems
8.30	30	Keynote: **Data on the Velocity Slip and Temperature Jump Coefficients** *F. Sharipov* *Universidade Federal do Paran´a, Brazil*
9.00	20	**Shear Driven Micro-Flows of Gaseous Mixtures** *D. Valougeorgis, S. Naris* *University of Thessaly, Greece*
9.20	20	**Effect of Slip on Transient Liquid Flow Development in Micro-Channels** *M.N. Sabry[1], A.R. Abdel-Rahim[2], M.H. Mansour[2]* *[1]) Université Française d'Egypte, Egypt* *[2]) Mansoura University, Egypt*
9.40	20	**Model Order Reduction of 3D Electro-Thermal Model for a Novel Micromachined Hotplate Gas Sensor** ***T. Bechtold[1], J. Hildenbrand[1], J. G. Korvink[1], J. Wollenstein[2]*** *[1)] IMTEK, University of Freiburg, Germany* *[2)] Institute for Physical Measurement Techniques, Germany*
10.00	20	**Non-contact Thermal Conductivity Measurements of P-doped and N-doped Gold Covered Natural and Isotopically-Pure Silicon and their Oxides** *M. G. Burzo, P. L. Komarov, P. E. Raad* *Southern Methodist University, Dallas*

10.20	20	Break

	Parallel poster sessions				
10.40-11.30	**Session 11**		**Session 12**		**Session 13**
	Modeling in Micro Technology		**Designing for Reliability**		**Material Characterization and Modeling**

Session 11:		**Poster session: Modeling in Micro Technology**
10.40	**50**	**Design and analysis of novel glass WLCSP structure** ***Chang-Ann Yuan , Cheng Nan Han, Kou-Ning Chiang*** *Department of Power Mechanical Engineering, National Tsing Hua University, HsinChu, Taiwan* **State of the Art in Prediction of Mechanical Behaviour of Microsystems** ***M. Lishchynska, N. Cordero, O. Slattery*** *NMRC, Lee Maltings, Prospect Row, Cork, Ireland* **Behavioral VHDL-AMS Modeling of Nuclear Magnetic Resonance Sensor** ***S. Megherbi[1], J.-C. Ginefri[2], L. Darrasse[2], G. Raynaud[1], J.-F. Pône[1]*** *[1)] Institut d'Electronique Fondamentale, France* *[2)] Unité de Recherche en Résonance Magnétique Médicale, University of Paris-Sud, france* **3D-FEM Modelling of an Electro-Optical Micro-Shutter** ***P. Roux[1], E. Woirgard[1], M. Pizzi[2]*** *[1)]IXL Laboratory, University of Bordeaux, Talence, France* *[2)]Centro Ricerche Fiat (CRF), Orbassano, Italia*
		Novel 2D Micronib Ionization Sources for Nano Electrospray-Mass Spectrometry (ESI-MS) ***S. Le Gac,[1] S. Arscott[1,2], C. Rolando[1]*** *[1)] USTL, UPRESA CNRS 8009, Villeneuve d'Ascq Cedex, France* *[2)] IEMN, UMR CNRS 8520, Villeneuve d'Ascq Cedex, France.*

Session 12:		**Poster session: Designing for Reliability**
10.40	**50**	**A Study of Cyclic Bending Reliability of Bare-die-type Chip-scale Packages** ***Yi-Shao Lai1, Tong Hong Wang, Han-Hui Tsai, Jenq-Dah Wu*** *Stress Characterization Laboratory, Advanced Semiconductor Engineering, Inc., Nantze, Kaohsiung, Taiwan*
		Three-Dimensional Stress Analysis of Ink Marking Process ***Chang-Lin Yeh1, Yi-Hsien Lin, Yi-Shao Lai, Hsiao-Chuang Chang, Jenq-Dah Wu*** *Advanced Semiconductor Engineering, Inc., Nantze, Kaohsiung, Taiwan*
		Microprocessor Packaging Strategy: Reliability of various Flip Chip BGA Packages on different Printed Circuit Boards *A. Guilhaume[1], C. Munier[1], C. Allégret[2], M. Michaud[2]* *[1)] EADS CCR, Service DCR/EP/EO, SURESNES Cedex, France* *[2)] MBDA, Vélizy Villacoublay, France* **Mechanism-Based Delamination Prediction During Reflow with Moisture Preconditioning** ***X.J. Fan[4], L.J. Ernst[1], G.Q.Zhang[2], W. van Driel[3]*** *[1)]Delft University of Technology, Delft, The Netherlands* *[2)]Philips Cft, Eindhoven* *[3)]ATO Innovation/Philips Semiconductors, Nijmegen, The Netherlands* *[4)]Philips Research USA, New York, USA*
		Microstructural Stability and Failure Modes in Eutectic Sn-Ag-Cu Solder ***M. A. Matin, W. P. Vellinga, and M. G. D. Geers*** *Division of Materials Technology, Department of Mechanical Engineering, Eindhoven University of Technology, Eindhoven, The Netherlands* **Analysis of Thermal-Moisture Induced Failure of Pb-free Soldered IC Packages in SMT Reflow Soldering Process** ***Ning Sun[1], Dachuan Lin[1], Daoguo Yang[1,2]*** *[1)] Guilin University of Electronic Technology, Guilin, China* *[2)] Delft University of Technology, The Netherlands*

Session 13:		Poster session: Material Characterization and Modeling
10.40	50	**Rupture Test on Polysilicon Films Through Electrostatic Actuation** ***F. Cacchione[1], B. De Masi[2], A. Corigliano[1], M. Ferrera[2]*** *[1)] Department of Structural Engineering. Politecnico di Milano, Milano, Italy* *[2)] MEMS Business Unit. STMicroelectronics, Cornaredo, (Milano), Italy*
		Evaluation of the Primary and Secondary Creep of SnPb Solder Joint Using a Modified Grooved-lap Test Specimen. ***S. Déplanque[1], W. Nüchter[1], B. Wunderle[2], H. Walter[2], B. Michel[2]*** *[1)] Robert BOSCH GmbH, Stuttgart, Germany* *[2)] IZM Fraunhofer Institut Zuverlässigkeit und Mikrointegration, Berlin, Germany*
		Numerical Simulation and Experimental Verification of the Piezoresistivity Phenomenon for the Printed Thick-Film Piezoresitors ***A. Wymysłowski[1], M. Santo – Zarnik[2,3], K. Friedel[1], D. Belavič[2,3]*** *[1)] Wrocław University of Technology, Wrocław, Poland* *[2)] Jožef Stefan Institute, Ljubljana, Slovenia* *[3)] HIPOT-R&D, Šentjernej, Slovenia*
		Void Formation in a Copper-Via-Structure Depending on the Stress Free Temperature and Metallization Geometry ***K. Weide[1], D. Dalleau[1], Y. Danto[2], H. Fremont[2]*** *[1)] Laboratorium für Informationstechnologie, University of Hannover,, Germany* *[2)] IXL, Universite Bordeaux I, Talence, France*
		Mechanical Characterisation of SiLK by Nanoindentation and Substrate Curvature Techniques ***V. Gonda[1], K.M.B. Jansen[1], L.J. Ernst[1], Jaap den Toonder [1], G.Q. Zhang[3]*** *[1)] Delft University of Technology, Delft, The Netherlands* *[2)] Philips Research Laboratories, Eindhoven, The Netherlands* *[3)] Center for Industrial Technology/Philips, Eindhoven, The Netherlands*
		Cantilever Microbeams: Modelling of the Dynamical Behaviour and Material Characterization ***R. Yahiaoui, A. Bosseboeuf*** *Institut d'Electronique fondamentale, University of Paris-sud Orsay, Orsay, France*
		A Novel Tool for Cure Dependent Viscoelastic Characterization of Packaging Polymers ***C. van 't Hof[1], L.J. Ernst[1], K.M.B. Jansen[1], D.G. Yang[1], H.J.L. Bressers[2], G.Q. Zhang[3]*** *[1)]Delft University of Technology, Delft, The Netherlands* *[2)]Philips Semiconductors, Nijmegen, The Netherlands* *[3)] Center for Industrial Technology/Philips, Eindhoven, The Netherlands*

	Parallel sessions		
11.30-12.40	Session 14		Session 15
	Modeling of MEMS and Optical Devices		Simulation-Based Thermal Design Strategies

Session 14:		Modeling of MEMS and Optical Devices
11.30	30	Keynote: **Hardware Description Language Modeling of an Electrostatically Actuated bi-axial Micromirror** ***F. Parrain[1], S. Megherbi[1], G. Raynaud[1], H. Mathias[1], J. Gilles[1], A. Bosseboeuf[1], G. Schröpfer[2], P. Cusin[3], N. Faure[3]*** *[1)] Institute d'Electronic Fondamentale UMR8622 – Université Paris-Sud, Orsay Cedex, France* *[2)] Coventor Sarl, Villebon, France* *[3)] Colibris SA, Neuchâtel, Switserland*
12.00	20	**Polymer Waveguide and VCSEL Array Multi-Physics Modelling for OECB Based Optical Backplanes** ***D. Gwyer[1], P. Missebrook[2,3], C. Bailey[1], P.P. Conway[3], K. Williams[3]*** *[1)] Centre for Numerical Modelling and Process Analysis, University of Greenwich, London, UK* *[2)] Celista, Stoke-on-Trent, UK* *[3)] Interconnection Group, Loughborough University, Loughborough, UK*
12.20	20	**Determination of Residual Stress in Glass Frit Bonded MEMS by Finite Element Analysis** ***M. Ebert, J. Bagdahn*** *Fraunhofer- Institute for Mechanics of Materials Halle, Germany*

Session 15:		Simulation-Based Thermal Design Strategies
11.30	30	**Keynote: A Computer-Architecture Approach to Thermal Management in Computer Systems: Opportunities and Challenges** ***K. Skadron, M.R. Stan, W. Huang, Zhijian Lu, K. Sankaranarayanan, J. Lach*** *University of Virginia, USA*
12.00	20	**Tri-dimensional reduced-order Thermal Model of Stacked Electronic Structures** ***V. Feuillet[1], V. Gatto[1], Y. Scudeller[2], Y. Jarny[1]*** *1) Laboratoire de Thermocinétique* *2) Laboratoire de Génie des Matériaux* *Ecole polytechnique de l'université de Nantes, Nantes, France*
12.20	20	**Thermal Modeling for Power MOSFETs in DC-DC Applications** ***Y. Bulut, K. Pandya*** *Vishay Siliconix, USA*

12.40	100	Lunch

14.20		Start Tuesday Afternoon Sessions

	Parallel sessions		
14.20-16.10	Session 16		Session 17
	Solder Reliability Behavior		CFD and FE Modelling of Thermal Performance

Session 16:		Solder Reliability Behavior
14.20	30	**Keynote: Reliability of SnPb and Pb-Free Flip-Chips under Different Test Conditions** ***M. Sprau[1], W. Nüchter[1], A. Möller[1], B. Wunderle[2], B. Michel[2]*** *[1)] Robert Bosch GmbH, Germany* *[2)] Fraunhofer-IZM, Berlin, Germany*
14.50	20	**Microstructural and Mechanical Characterization of 95.5Sn-4Ag-0.5Cu Solder Balls by Nano-Indentation** ***M. Erinç[1], P. Schreurs[1], G.Q. Zhang[1], W. D. van Driel[2], M. Geers[1]*** *[1)] Technical University of Eindhoven, Eindhoven, The Netherlands* *[2)] ATO Innovation/Philips Semiconductors, 6534 AE Nijmegen, The Netherlands*
15.10	20	**Modeling Stress Strain Curves For Lead Free 95.5Sn-3.8Ag-0.7Cu Solder** ***J.H.L. Pang, B.S. Xiong and T.H. Low*** *Nanyang Technological University, School of Mechanical and Production Engineering, Singapore*
15.30	20	**Effect of Different Temperature Cycle Profiles on the Crack Propagation and Microstructural Evolution of Real Lead Free Joints of Different Electronic Components** ***C. Andersson[1,2], D. Andersson[1,3], P-E Tegehall[1,3], Johan Liu[1,2,3]*** *[1)] Swedish Microsystem Integration Technology (SMIT) Center* *[2)] Division of Electronics Production, Chalmers University of Technology, Mölndal, Sweden* *[3)] IVF Industrial Research and Development Corporation, Sweden*
15.50	20	**A Review of Creep Fatigue Failure Models in Solder Material - Simplified Use of a Continuous Damage Mechanical Approach** ***G. Massiot, C. Munier*** *EADS Corporate Research Center, Suresnes cedex, France*

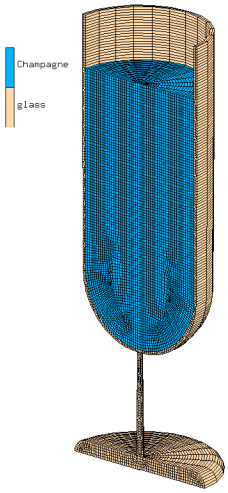
Session 17:		CFD and FE Modeling of Thermal Performance
14.20	**30**	**Keynote: Thermal and Flow Analysis of SiC-Based Gas Sensors for Automotive Applications** *I. Below[1], P. Leisner[1], H. Wingbran[2], A.L. Spetz[2], H. Sundgren[2], B. Thuner[2], H. Svenningstorp[3], P. Leisner[4]* *[1)] Jönköping University, Sweden* *[2)] Linköping University, Sweden* *[3)] Volvo Technology Corporation, Sweden* *[4)] Acreo, Sweden*
14.50	**20**	**Low Reynolds Number Turbulence Models for Accurate Thermal Simulations of Electronic Components** *K Dhinsa, C Bailey, K Pericleous* *University of Greenwich, UK*
15.10	**20**	**Thermal Testing of a 3-Die Stacked Chip Scale Package Including Evaluation of Simplified and Complex Package Geometry Finite Element Models** *B.A. Zahn* *ChipPAC, USA*
15.30	**20**	**Thermal Analysis of QFN Packages Using Finite Element Method** ***C.L. Chang, Y.Y. Hsieh*** *National Yunlin University of Science and Technology, Taiwan*
15.50	**20**	**Experimental Study on Visualization of a Longitudinal Heat Sink with Top-mounted Fan by Particle Tracking** *J.H. Jang* *Kuang-Wu Institute of Technology, Taiwan*

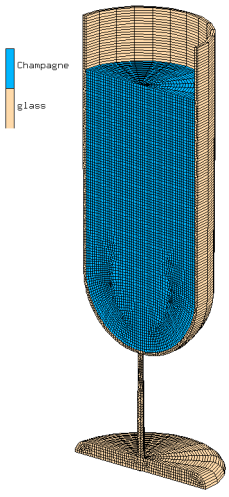
16.10	**20**	**Break**

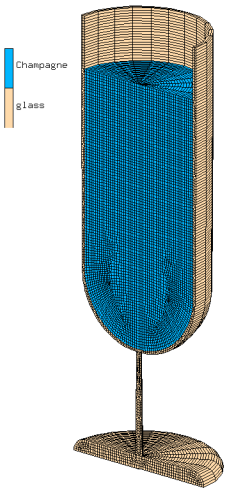
		Special Exhibitor session
16.30		

18.00		**End of 2nd day Technical Sessions**

18.10		Cocktail reception







Wednesday May 12, 2004: Technical programme day 3

8.30		**Start Wednesday Morning Sessions**

Session 18:		**Keynote session: Micro- to Macro-Scale Thermal Design Challenges in Microelectronics**
8.30	**30**	**Keynote: Modeling Heat Transfer and Liquid Flow in Micro-Channels** ***M.N. Sabry[1]***, *B.O. Djebedjian[2], S.H. Saleh[2], M.M. Mahgoub[2]* *[1]) Université Francaise d'Egypte, Egypt* *[2]) Mansoura University, Egypt*
9.00	**30**	**Keynote: Cooling Problems and Thermal Issues in High Power Electronics: a Multi-Faceted Design Approach** ***M. Behnia[1]***, *L. Maguire[2]* ***,G. Morrison[2]*** *[1]) The University of Sidney, Australia* *[2]) University of New South Wales, Australia*
9.30	**30**	**Keynote: Design Challenges for High-Performance Heat Sinks used in Microelectronic Equipment: Evolution and Future Requirements** ***P. Rodgers[1], V. Eveloy[2]*** *[1]) CALCE Electronic Products and Systems Center, University of Maryland, USA* *[2]) Electronics Thermal Management, Ltd., Ireland*

10.00	**40**	**Break**

	Parallel sessions		
10.40-12.30	**Session 19**		**Session 20**
	Solder Fatigue		**Characterization and Modeling of Polymer behavior**

Session 19:		**Solder Fatigue**
10.40	**30**	**Keynote: A Mechanics-Based Strain Gage Methodology for Direct Solder Joint Reliability Assessment** ***L.L. Mercado, S. Girouard, G. Hsieh*** *Intel, Chandler, USA*
11.10	**20**	**Microstructural Behaviour of Solder Alloys** ***R.L.J.M. Ubachs, P.J.G. Schreurs, M.G.D. Geers*** *Eindhoven University of Technology, Departement of Materials Technology, Eindhoven, The Netherlands.*
11.30	**20**	**Flip Chip Solder Joint Fatigue Analysis Using 2D and 3D FE Models** ***A. Yeo[1], C. Lee[1], J. H.L. Pang[2]*** *[1)] Infineon Technologies Asia Pacific Pte Ltd, Assembly & Interconnect Technology, Singapore* *[2)] *School of Mechanical and Production Engineering, Nanyang Technological University, Singapore*
11.50	**20**	**Thermal Fatigue Modelling for SnAgCu and SnPb Solder Joints** ***R. Dudek, H. Walter, R. Doering, B. Michel*** *Fraunhofer IZM, Berlin, Germany*
12.10	**20**	**Thermal Cycling Reliability of SnAgCu and SnPb Solder Joints: A Comparison for Several IC-Packages** ***B. Vandevelde, M. Gonzalez, P. Limaye, P. Ratchev, E. Beyne*** *IMEC, Leuven, Belgium*

Session 20:		Characterization and Modeling of Polymer behavior
10.40	30	Keynote: **Molecular Modeling Studies of IC Barrier Concerns.** ***N. Iwamoto,*** *Honeywell Specialty Materials, Morristown, USA*
11.10	20	**Molecular Simulation of Cu-SAM Adhesion Force** ***H. Fan, C.K. Wong, M.M.F. Yuen*** *Department of Mechanical Engineering, Hong Kong University of Science and Technology, Kowloon, Hong Kong*
11.30	20	**Cure, Temperature and Time dependent Constitutive Modeling of Moulding Compounds** ***K.M.B. Jansen[1], L. Wang[1], D.G. Yang[1], C. van 't Hof[1], L.J. Ernst[1], H.J.L. Bressers[2], G.Q. Zhang[3]*** *[1)]Delft University of Technology, Delft, The Netherlands* *[2)]Philips Semiconductors, Nijmegen, The Netherlands* *[3)]Philips CFT, Eindhoven, The Netherlands*
11.50	20	**Simulation of No-Flow Underfill Process for Flip-Chip Assembly** ***A. Kolbeck[1], T. Hauck[1], J. Jendrny[2], O. Hahn[2], S. Lang[3]*** *[1)] Motorola GmbH, Deutschland* *[2)] LWF, Universität Paderborn, Deutschland* *[3)] CADFEM Gmbh, Grafing, Germany*
12.10	20	**Mechanical Properties of Molding Compounds (MCs) under Different Moisture Conditions and in a Wide Temperature Range** ***W.H. Zhu, S. L. Gan, C.L. Toh*** *Assembly and Interconnect Technologies, Infineon Technologies Asia Pacific Pte Ltd, Singapore*

12.30	90	Lunch

14.00		Start Wednesday Afternoon Sessions

Session 21:		Keynote session: New Developments in Microelectronics Reliability
14.00	30	Keynote: **Challenges of Thermomechanical Design and Modeling of Ultra Fine-Pitch Wafer Level Packages** ***A. A. O. Tay*** *Department of Mechanical Engineering, Nano/Microsystems Integration Laboratory, National University of Singapore, Singapore*
14.30	30	Keynote: **Topography and Deformation Measurement under Thermomechanical Stress** ***R. Fayolle, J. Lecomte*** *Insidix, Seyssins, France*
15.00	30	Keynote: **Reliability of Interfaces for Lead-Free Solder Bumps** ***R.L.H. Shih[1], D.Y.K. Lau[2], R.W.M. Kwok[2*], M. Li[3], M.K.W. Sun[4]*** *[1)] Department of Chemistry, The Chinese University of Hong Kong, Shatin, N.T., Hong Kong* *[2)] Rohm and Haas Electronic Materials Asia Limited, 15 On Lok Mun Street, Fanling, N.T., Hong Kong* *[3)] Department of Electronic Engineering, The Chinese University of Hong Kong, Shatin, N.T., Hong Kong* *[4)] Department of Physics, The Chinese University of Hong Kong, Shatin, N.T., Hong Kong*
15.30	30	Keynote: **From Chemical Building Blocks of Polymers to Microelectronics Reliability** **H.J.L. Bressers[2], W.D. van Driel[3], K.M.B. Jansen[1], L.J. Ernst[1] and G.Q. Zhang[3]** *[1)]Delft University of Technology, Delft, The Netherlands* *[2)]Philips Semiconductors, Nijmegen, The Netherlands* *[3)]Philips CFT, Eindhoven, The Netherlands*

16.00	End of Conference

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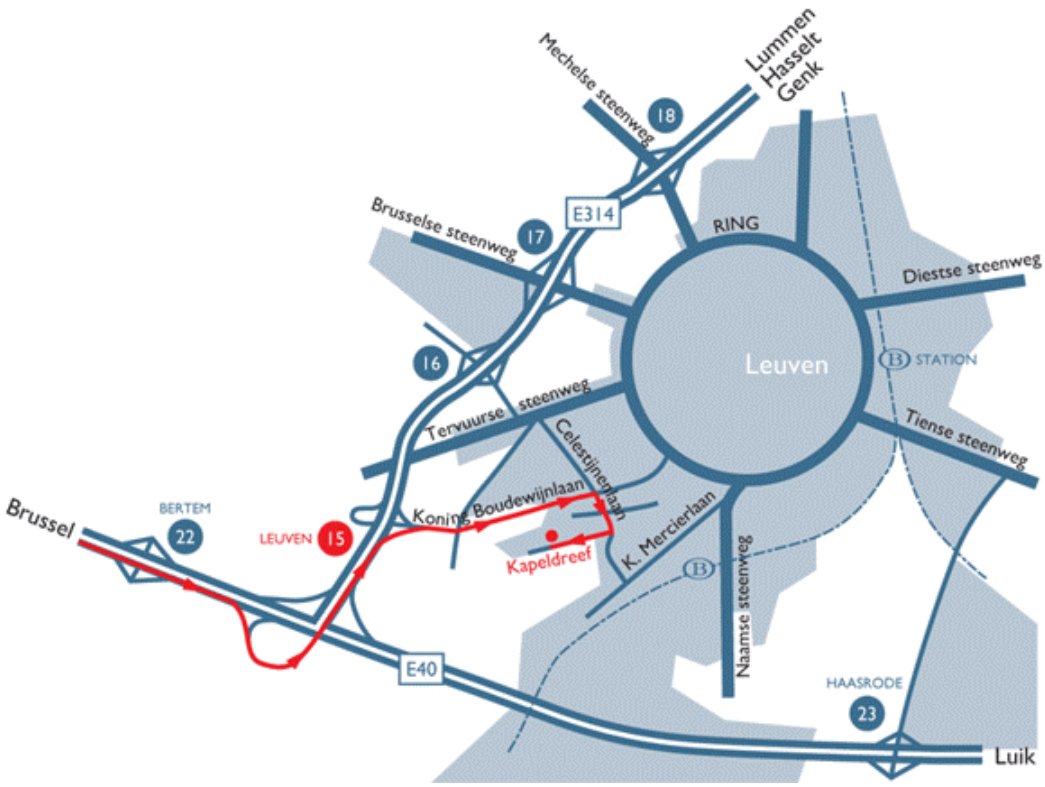
Location of courses + hotel info

IMEC
Kapeldreef 75, 3001 Leuven, Belgium

How to reach IMEC:
By car: IMEC is located in Heverlee, Leuven, approximately 25 km from both Brussels and International Airport "Zaventem". It takes half an hour drive by car to reach IMEC from Brussels, capital of Belgium. Leuven lies at the intersection of two highways, the E40 highway London (GB) - Brussels - Liège - Köln (Germany) and the E314 highway Leuven-Hasselt-Aachen (Germany). For a visual representation, see our map. Taxi fare from Brussels city centre to IMEC is approximately 50 Euro.
By train: Leuven is situated along the international rail line serving London (GB) - Brussels - Liège - Köln (Germany). If you are travelling from another direction then the ones mentioned above, a changeover at Brussels' North, Central or South Station is needed to reach Leuven. If you are coming from Brussels airport, take the underground station located in the airport building to reach Brussels Station North (Noord). From this station you can take the train to Leuven. For more information about the Belgian Railroad company "NMBS" and its trains go to www.nmbs.be. Taxi fare from Leuven station to IMEC is approximately 10 Euro.
By Bus: From Leuven station or downtown Leuven city, bus 2 - CAMPUS will bring you to the Kapeldreef in Heverlee (terminus). The bus stop is situated just opposite of the IMEC building. For more information about the Flemish bus company "De Lijn" go to www.delijn.be



Hotels in Leuven (to stay from May 8th to May 9th): http://www.book-a-hotel-in-leuven.com/
(closest hotel to IMEC: The Lodge in Heverlee: http://www.lodge-hotels.be/)

Conference location

EUROSIME 2004

NOVOTEL Tour Noire
Rue de la Vierge Noire 32, B-1000 Brussels, Belgium
Phone +32(0) 2 505 50 50, Fax +32(0) 2 505 50 00
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Hotel information form

EUROSIME 2004

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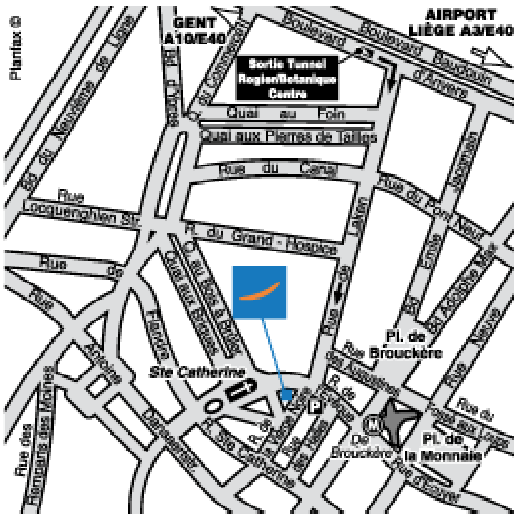

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EuroSimE 2004

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I shall attend (please tick boxes) :

Sunday May 9 : 9.00 to 12.30, in Leuven (IMEC)	**Sunday May 9 : 13.30 to 17.00, in Leuven (IMEC)**
☐ C2: Application of static and dynamic compact thermal models	☐ C3: Heat sink design and analysis for microelectronic equipment
☐ C4: Advanced optimization methods for design and qualification	☐ C5: Lead-free solder joints: Reliability trends and material Properties
☐ C6: Fundamentals of board-level assembly and solder joint reliability	☐ C7: µ-vias and high density interconnects for advanced packaging
☐ C8: Wafer level packaging technologies	

☐ **The conference on May 10-12, in Brussels**	☐ Vegetarian lunches ☐ Vegetarian dinner (Monday May 10)
☐ The dinner on Monday May10 (free for participants)	☐ Other food requirements: ……..

Participation to the conference includes access to exhibition, lunches, social event, cocktail party, proceedings of the conference (bound + CD)

Price calculation:

Item	***Price early registration (before April 24th)***	***IEEE member Number: _____***	***Supplement for late registration (after April 24th)***	***Your price***
Conference	550 €	495 €	+ 100 €	
One course (C2 – C8)	250 €	225 €	+ 100 €	
Two courses (or C1)	400 €	360 €	+ 100 €	
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