ESSCIRC'2000

26th European
Solid-State Circuits Conference

19 – 21 September 2000
Stockholm, Sweden

Organised by:

KUNGL TEKNISKA HÖGSKOLAN
Royal Institute of Technology

with sponsorship of

SSF, NUTEK, TFR and ACREO

Conference Venue

The conference place is located in the Electrum building, Kista Science Park. Kista is located in the north-west part of Stockholm 32 kilometres from Arlanda airport and about 20 min by subway to the centre of Stockholm.

Address: Kungl. Tekniska Högskolan (KTH)
Electrum
Isafjordsgatan 22/Kistagången 19
KISTA, Stockholm

Stockholm - in particular the industrial region in the northern part around Kista - is one of the most dynamically expanding areas in Europe in the field of mobile communication systems and devices. Kista is often referred to as "Wireless Valley" and is rapidly developing as one of the world's leading science parks. ELECTRUM in Kista, is a major European Center for Information Technology. It is the result of a unique co-operation between the Government, the City of Stockholm and Swedish computer and electronics industry. It is built on active co-operation between education, research and industry.

In ELECTRUM the competence areas range from material physics and components to systems design and applications. There is a close co-operation between education, research and industry.

Kungl. Tekniska Högskolan (KTH) is the largest technical university in Sweden and has recently established a new faculty of information technology in Kista with the objective of becoming one of the leading European universities in research and education in information technology area.

Today more than 3500 people work in ELECTRUM, 500 teachers and researchers, thirty professors and more than 3000 students from KTH and Stockholm University.
A great proportion of Swedish Industry is concentrated to Kista next to ELECTRUM, as well as software houses, telecommunication systems manufacturers and microelectronics manufacturers. Most computer manufacturers are represented in the area.

Conference Secretariat

Kungl. Tekniska Högskolan (KTH)
Zandra Lundberg
ELE/EKT
Electrum 229
SE-164 40 KISTA
Phone: +46-8 7521348
Fax: +46-8 7527850
E-mail: zandra@ele.kth.se

Registration and Information

The registration desk is located in the Electrum hall.
During ESSCIRC the conference desk will be open:

Monday, 18 September	09:00 - 19:00
Tuesday to Thursday, 19-21 September	08:00 until the end of the conference sessions
Friday, 22 September	09:00 - 13:00

FOREWORD

With great pleasure we welcome you to the ESSCIRC 2000 in Kista, Stockholm, Sweden.

Sweden is one of the leading Nordic countries in both the mobile phones industry and in the number of active handset users. During the last decade this rapid movement towards a wireless society has become one of the striving forces for the development of the new microelectronics technologies. The new wireless applications require broadband data transmission and this will push circuit design development as well into a rapid growth.

This conference is focused on wireless and telecommunication circuits and systems, data-converters, sensor-systems, digital systems, memories and signalling techniques. There are invited papers on wireless systems, presenting topics on the future wireless telecommunications, on basestation design techniques and on the Bluetooth, all introducing very demanding new aspects. Invited papers are contributed also on analogue circuit design with deep submicron CMOS technology, on circuit designing with SOI CMOS technology and on the 3-D integration technologies, striving at the future IC-technologies. To continue, challenging system integration aspects are brought up also in the invited papers concentrating on the VDSL and on automotive electronics and sensor applications.

The technical programme of the ESSCIRC'2000 includes 8 invited papers, 66 oral presentations and 50 posters, which have been carefully selected by renowned experts out of 217 submitted contributions from all over the world. In addition 4 workshops will be devoted on up-to date topics. For your interest and pleasure, social events are organised to complement the technical programme by offering the possibility for informal meetings. We hope that you enjoy your stay in Stockholm!

Prof. Hannu Tenhunen
Conference Chairman

Prof. Kari Halonen
Technical Programme Chairman

ESSCIRC ON INTERNET

http://www.esscirc.org

Workshop	
Monday	
08:300	Registration
09:00	Workshops
12:00	Lunch
13:00	Workshops
16:00	End of Workshops

Conference			
Tuesday			
08:00	Registration		
09:00	Opening		
	Best Paper '99		
09:20	Keynote		
10:10	Coffee Break		
10:40	S1.1	S1.4	S1.7
12:20	Lunch		
14:00	Invited		
14:50	S1.2	S1.5	S1.8
15:40	Coffee Break		
16:10	S1.3	S1.6	S1.9
18:00	Reception		

Wednesday			
08:30	Invited		
09:20	S2.1	S2.4	S2.7
10:10	Coffee Break		
10:40	Invited		
11:30	S2.2	S2.5	S2.8
12:20	Lunch		
14:00	Invited		
14:50	S2.3	S2.6	S2.9
15:40	Coffee Break		
16:00	Posters		
20:00	Conference Banquet		

Thursday			
08:30	Invited		
09:20	ESSCIRC 2001		
09:25	S3.1	S3.4	S3.7
10:15	Coffee Break		
10:45	Invited		
11:35	S3.2	S3.3	S3.4
12:25	Lunch		
14:00	Invited		
14:50	S3.3	S3.6	S3.9
16:05	Young Sc. Award		
	Closing Session		

Workshop	
Friday	
08:00	Registration
09:00	Workshops
15:00	End of Workshops

TECHNICAL PROGRAMME

Workshops

Four workshops will be given:
Monday, 18 September 2000
Design Techniques for Mobile Equipments
Organiser: Philippe.Garcin@st.com / STMicroelectronics, France
presented by the project partners from MEDEA-A451/LIBERTY and MEDEA-A453
CAD for Mixed Analogue-Digital and RF ICs: the Current State of the Art
Organiser: George Gielen / K.U. Leuven, Belgium

Friday, 22 September 2000
RF-Circuits
Organiser: Christer Svensson / Linköping Technical University, Sweden
Ton Wagemans / Philips RF Business Development Center Mansfield MA, USA

Systematic Analogue Design: Hope or Hype
Organiser: Peter Jores / Robert Bosch GmbH, Germany

Conference (Tuesday, Wednesday, Thursday)

Invited: 8 speakers and one keynote speaker have been invited.
Regular: 65 papers will be orally presented.
Posters: 43 posters will be presented on Wednesday afternoon during which time the authors will be present to answer questions. The posters will be displayed throughout the three conference days.

Awards

Best Paper Award '99
The Best Paper Award'99 will be presented by the last year's Programme Chairman, Mr. B. Hosticka, Fraunhofer IMS, Germany, at the opening of this year's conference.
Best Paper Award '00
The participants will be invited to select the Best Paper from the contributed papers presented this year. The Award will be presented at ESSCIRC'2001.
Best Poster Award '00
The Best Poster Award '00 will be presented during the closing session of the conference.

Poster Session

Poster Session on Wednesday, 22 September 2000, from 16:00 – 19:30.

PROCEEDINGS

Conference Proceedings

Each registered participant will receive a copy of the conference proceedings. Additional copies may be purchased during the conference. After the conference, please contact:

Editions Frontières
20, Rue d'Armenonville
F-92200 NEUILLY/SEINE
Phone: +33-1-47 22 59 09
Fax: +33-1-47 47 07 57
E-Mail: frontier@club-internet.fr

Workshop Proceedings

Each registered participant of the workshop will receive a copy of proceedings of the workshop he or she registered for.

SOCIAL PROGRAMME

Welcome Reception at the Stockholm City Hall

The reception will take place at the City Hall in the centre of Stockholm on Tuesday evening. The City Hall building was finished in 1923 and has been designed by the Swedish architect Ragnar Östberg. The reception is hosted by the mayor of Stockholm. http://www.stockholm.se/cityhall/

Conference Banquet

The conference banquet on Wednesday evening will be held in the Vasa Museum. The dinner will be served in the shiphall next to the restored Vasa ship originally built in 1628 and salvaged in 1961. http://www.vasamuseet.se

REGISTRATION AND ACCOMMODATION BOOKING

Registration

Registration to the conference and workshops should be made by returning the completed registration form by fax or by mail. This form can be found in this programme or printed from our Internet site.

Full registration fee includes attendance to the conference (Tuesday, Wednesday and Thursday), lunches and coffee breaks, welcome reception, conference banquet and conference proceedings (hardcopy+CD-ROM).

The student registration fee (only for B.sc. and M.Sc. students) includes all of the above except the conference proceedings hardcopy and the conference dinner. It is possible to register for the conference banquet and/or proceedings hardcopy separately.

Registration is final when full payment has been received by the Conference Secretariat. Substitutions can be accepted at any time before the start of the conference. Payment should be made in advance. Payment for early registration should be received **no later than August 1, 2000**.

Accommodation

The participants of the ESSCIRC 2000 have to book their own accommodation directly with the hotel. Hotels listed below are located in Kista, or in the Stockholm City, which is about 20 minutes from Kista. A limited number of rooms have been reserved for the conference participants. Early reservation is highly recommended.

Hotel reservation deadline is August 1. After this date we cannot guarantee any hotel accommodation. Arrival on Saturday, 16 September enables special prices during weekend.

Memory Hotel
Borgarfjordsgatan 3, SE-164 25 Kista
Phone: +46-8-793 07 00
Fax: +46-8-793 08 00 *"walking distance*
Bookingref: DW248 *ca 2 minutes"*
Single room – SEK 1280:-
http://www.memoryhotel.se
hotel@ memoryhotel.se

Mr Chip Hotel
Färögatan 9, SE-164 26 Kista
Phone: +46-8-750 56 00
Fax: +46-8-751 85 80 *"walking distance*
Bookingref: DO291 *ca 2 minutes"*
Single room – SEK 1170:-
http://www.mrchip.kistahotel.se
hotel@mrchip.kistahotel.se

Hotel Adlon
Vasagatan 42, SE-111 20 Stockholm
Phone: +46-8-402 65 00
Fax: +46-8-20 86 10
Bookingref: G138766
Single room – SEK 1495:-
http://www.adlon.se

Hotel Esplanade
Strandvägen 7A, SE-114 56 Stockholm
Phone: +46-8-663 07 40
Fax: +46-8-662 59 92
Bookingref: MS 1405
Single room – 1 225:-
http://www.hotelesplanade.se/
hotel@hotelesplanade.se

Hotel Oden
Karlbergsvägen 24, 102 34 Stockholm
Phone: +46-8-457 97 00
Fax: +46-8-457 97 10
Bookingref: FE259
Single room – SEK 945:-
http://www.hoteloden.se
hotel@hoteloden.se

Hotel Stockholm
Norrmalmstorg 1, 111 46 Stockholm
Phone: +46-8-678 1320
Fax: +46-8-611 2103
Bookingref: 53408
Single room – SEK 1050:-
http://www.hotelstockholm.aos.se
info.stockholm@swedenhotels.se

If you have any further questions concerning the accommodation (e.g. double occupancy rates etc.) please contact the hotel.

Information about other hotels can be found on
http://rival.spray.se/hotell/english.asp

Payment

Payment of the conference and workshop fees should be made by credit card (Visa, Eurocard/MasterCard). On-site payment by credit card or cash.

Cancellation policy

The registration fee is not refundable.

Liability

The conference organisation accepts no responsibility for accidents to conference delegates or for damage or loss of personal property during the conference.

TRAVEL INFORMATION

By air arriving at Arlanda airport

Bus:	Take the airbus line Arlanda-Brommaplan to Kista Centrum, approx 30 min. A 5 minutes walk will take you to the Electrum building.
Taxi:	Use "Taxi Stockholm" or "Taxi - 020" to address Electrum, Kista. Agree on price with the driver before leaving Arlanda, should be approx. SEK 300-350.- 30 minutes drive.
Car:	After approx 30 km on the E4 take the Kista exit. Turn right toward Kista Centrum. Turn right in the traffic circle and then left at the OK Q8 gas station to Isafjordsgatan.
Parking:	We do not recommend to arrive by car as the parking possibilities are very limited in Kista.

Subway (T-Tunnelbana) to Kista Centrum

Take the blue Line 11 Kungsträdgården-Akalla to Kista Centrum subway station. Travel time from Stockholm city to Kista approx. 20 minutes.
Follow the signs to Electrum through the shopping centre. Use the exit close to the post office, follow Kistagången to #16 and enter into Electrum. The walk will take you less than 5 minutes.

Commuter Train (J-Pendeltåg) Helenelunds station

Line Södertälje-Märsta from Stockholm Central to Helenelunds station - 15 minutes. Walking from Helenelund to Electrum approx 15 min.

INVITED PAPERS

Future is in Wireless

Key-Note: Yrjö Neuvo / Nokia Mobile Phones, Finland

The wireless Internet will introduce revolutionary new applications that pave the way toward a mobile information society.

Third generation mobile communication systems and broadband wireless access systems will play the key role in enabling wireless Internet. Because of rapidly increasing system complexity, wireless terminal manufacturers face huge challenges in ensuring fast product creation. In the radio frequency section, the main challenge is to achieve high overall linearity with low power consumption and low implementation complexity. In the baseband section, managing complexity remains the key challenge; it requires a paradigm shift in system and IC design practices, the design re-use of circuit blocks.

Bluetooth™: From Antenna to Silicon

Jaap Haartsen / Ericsson Radio Systems, The Netherlands

Recently, a new universal radio interface called Bluetooth™ was developed enabling electronic devices to connect and communicate via short-range radio links.

The Bluetooth technology is regarded as a complement and an extension to existing wireless technologies, addressing the short-range and inter-device connectivity. The technology allows the design of low-power, small-sized, and low-cost radios that can be embedded in a wide range of future products, which will eventually lead towards ubiquitous connectivity between these products.

The paper addresses the implementation aspects of the Bluetooth transceiver. It also discusses the trade-offs made in the air interface specification to achieve single-chip implementations.

SOI CMOS Circuit Design Exposed -
Another Dirty Tricks Campaign?

William Redman-White / Philips Semiconductors, United Kingdom
Kerry Bernstein / IBM Essex Junction, USA

SOI CMOS is finally shaking off the double-edge epithet of the "technology of tomorrow" and is emerging as a viable mainstream process.

Much has been written about the device physics, but rather little definitive material has addressed circuit designers' questions. What have gained attention have been arguments over achievable benefits, and scary stories of strange behaviour, with great difficulties in design and simulation.

In this paper we aim to put the technology issues in perspective for both digital and analogue designers, and to show where the opportunities as well as the problems lie. To exploit the features and to solve the problems we focus not on technology tweaks, but on the circuit designer's stock in trade - (dirty) tricks.....

Software-Radio Base-Stations, a Challenge For Analog IC-Design

Arne Rydin / Ericsson Radio Systems, Sweden

The paper discusses the impact and aspects on analog IC for wideband radio systems and in particular software defined radio.

The strong evolution of digital ASIC's and signal processing cause analog IC and dataconverters to be bottlenecks of future radio systems. Signal dynamic range and linearity of dataconverters, frequency converters and power amplifiers are already today a great challenge.

The handling of this challenge is discussed in terms of process evolution, the importance of understanding technology limitations, the impact of design experience and the advantage of understanding the RF-design language. To exemplify the challenge, solutions of converter circuits and complex control circuitry for RF-frequencies are presented.

VDSL, From concept to chips

Paul Spruyt / Alcatel Research, Belgium

VDSL (Very high-speed Digital Subscriber Line) can transport data at tens of Megabits-per-second (Mbit/s) over conventional copper twisted pairs that have been used for more than a century to carry only voice calls or low-speed data.

Following, in the last decades, a gradual increase of transmission speeds over the telephone access network by means of successive DSL technologies, VDSL puts the copper loop in a higher gear. Whereas ADSL (Asymmetric DSL) brings you Internet downloads at warp speeds and good video, VDSL can deliver several films simultaneously. To enable such super-fast traffic, the frequency band over which the system operates has to be increased, from about 1 MHz for ADSL to over 10 MHz for VDSL. This requires faster digital signal processing and analog (integrated) components with higher bandwidths. In addition the system has to withstand loop impairments that were inexistent or less stringent for other DSL variants.

Once again (as for ADSL) Discrete MultiTone (DMT) transmission turns out to deliver the required performance. If carefully implemented, DMT can be combined with frequency division duplexing (FDD) without requiring filters for up- and downstream frequency band separation, resulting in extreme flexibility for spectral shaping and band allocation. This paper takes you in a couple of pages from the concepts up to the implementation of a system-on-chip. It shows how a very performant and flexible FDD-DMT VDSL system can be integrated while meeting the requirements on power and size.

Analog Design in Deep Submicron CMOS Technology

Klaas Bult / Broadcom Netherlands, The Netherlands

Analog integration in deep sub-micron CMOS has become an economic necessity. This paper discusses problems and design challenges of analog circuits integrated in purely digital deep sub-micron CMOS technologies.

The discussion will touch upon process related issues, like the scaling of the supply voltage, increasing 1/f-noise, and the use of process options like thick-oxide or low-Vt transistors, circuit related issues, like OpAmps, gain stages and the use of switches, system related issues like system partitioning, power dissipation

and cross-talk, as well as business related topics, like the shortened life-cycle of process technologies, time-to-market and design-time. Emphasis will be on circuit-level aspects, mainly focussed on front-end circuits like Amplifiers, Track & Hold Circuits, and ADC's.

Future Trends in Automotive Electronics, Sensors and Communication Systems

Karl-Thomas Neumann / Volkswagen AG, Germany

90% of all future innovations in the automotive world are mainly driven by electronics.

This lecture will give an overview on actual and future applications of electronics in cars. The major areas are powertrain, comfort functions, passive and active safety and the emerging fields of entertainment, communication and information. Examples of current research projects such as autonomous driving, where test vehicles are driven by a robot which has video and laser sensors as well as a high precision GPS system will be given. The convergence of telecommunication, consumer and computer technology with in-vehicle electronics will be shown using examples from the field of multimedia within the car.

3-D ICs: Motivation, Performance Analysis, and Technology

Krishna Saraswat / Stanford University, USA

Continuous scaling of VLSI circuits is reducing gate delays but rapidly increasing interconnect delays. Semiconductor industry roadmap predicts, that beyond the 130 nm technology node, performance improvement of advanced VLSI is likely to begin to saturate unless a paradigm shift from present IC architecture is introduced.

The paper presents a comprehensive analytical treatment of ICs with multiple Si layers (3-D ICs). It is shown that significant improvement in performance (more than 145%) and reduction in wire-limited chip area can be achieved with 3-D ICs with vertical inter-layer interconnects. This analysis is based on dividing a chip into separate blocks, each occupying a physical level. A scheme to optimize interconnect distribution among different interconnect tiers is presented and the effect of transferring the repeaters to upper Si layers has been quantified in this analysis.

Furthermore, thermal analysis of ICs with two Si layers is presented. It is demonstrated that below 110 nm technology node die temperatures for ICs with two Si layers can be lower than the corresponding projected values for ICs with single Si layer. This is attributed to decrease in overall interconnect capacitance for the 3-D case. Finally, various technologies being investigated for 3-D fabrication are reviewed.

Monday, 18.09.2000

Design Techniques for Mobile Equipments
Organiser: Philippe Garcin
STMicroelectronics, France

Registration - 08:30

Morning session - 09:00 – 12:00

LIBERTY – MEDEA Project A-451

LIBrary Enhancement for Radio Transceivers

ACCO – MATRA NORTEL COMMUNICATIONS (MNC)
ST MICROELECTRONICS (STM) – LABORATORI FONDAZIONE GUGLIELMO MARCONI (LABS) – UNITED MONOLITHIC SEMICONDUCTORS (UMS) – THOMSON MICROSONICS (TMX)

The surge of information technologies is rapidly pulling up the ever-growing market of components for wireless communication. The driving forces in the design of new generations of equipment are cost reduction and economic improvement. The latter can be translated in terms of weight/size reduction on the one hand and autonomy increase on the other hand. These stringent requirements directly lead to a higher level of integration and low power oriented designs for architectures and components.
At the same time, new standards are emerging to obtain higher data transmission rate like GSM-EDGE and UMTS. Then, the new generation of components is expected to achieve versatile use in existing standards and in future ones.
In that context, Liberty is one of these dedicated MEDEA Programs which has been launched to explore technology and architecture opportunities to reduce the bill of hardware, the part count and the power consumption.
In order to fulfil the market expectations here above targeted, some technical challenges, as innovative architectures definition and high performance-level functions design (ADDA, PA, SAW filters, multi-mode synthesiser), remain to be overcome while multi-mode design guidelines and multi-mode oriented macro-cells are lacking.
This new Liberty program focuses on those blocks with the aim to develop the design guidelines and the macro libraries for multi-mode purpose, which in turn will enable quick development of this type of blocks, necessary for versatile multi-mode transceivers.
The identified demonstrators are developed using state of the art well suited technologies such as LDDMOS and GaAs HBT for Power Amplifiers, Bi(SiGe)CMOS for fast ADDA, CMOS for synthesiser and SAW filters technology.
This half-a-day workshop will be dedicated to the presentation of the performed works in the frame of the program, with design techniques oriented contents. Program goals, consortium skills, description of tasks and results, master milestones and further developments will be addressed.

Monday, 18.09.2000

Afternoon session - 13:00 – 16:00

MEDEA Project A-453

Low-Power Digital Design Techniques

NOKIA – STMicroelectronics – ANACAD
HTMicroelektronik – University of Saarland – X-Fab

Under the co-ordination of Nokia, key-players in European IC Manufacturing and EDA (STMicroelectronics, X-Fab and ANACAD), HT Microelektronik design house for low power, and University of Saarland are involved in a 2-year co-operative program (1999-2000) *Low-Power Digital Design Techniques*. As density increases, new design for Low-Power challenges regularly appear, concerning both System-on-Chip complexity and physical-level details.
A set of innovative design and process techniques resulting from the MEDEA A-453 Program are now available for industrial use - thus contributing to solve the above issues. The most outstanding techniques will be presented in a half-a-day public Workshop at ESSCIRC 2000.

Main topics:

- Project Overview
- Low Power architectures for telecommunication applications
- Low Power architectures for hearing aid applications
- Architectures, circuit concepts and low voltage research
- Static power optimisation through process and design techniques
- Cell-level and circuit-level estimation concepts

For pre-booking, please write to Organiser :
Philippe.Garcin@st.com

For further contacts, please write to Project Manager:
Mohsen.Darianian@nokia.com

Monday, 18.09.2000

CAD for Mixed Analogue-Digital and RF ICs: the Current State of the Art

Organiser: George Gielen / K.U. Leuven, Belgium

Speakers:

Georges Gielen, Katholieke University of Leuven, Leuven, Belgium
Rob Rutenbar, Carnegie Mellon University, Pittsburgh, U.S.A
Jaijeet Roychowdhury, Lucent Bell Labs, Murray Hill, U.S.A.
Francois Clement, Snaketech, Grenoble, France

Overview:

The growth of wireless services and other telecom applications increases the need for low-cost highly integrated solutions with very demanding performance specifications. This requires the development of intelligent front-end architectures that circumvent the physical limitations posed by the technology. In addition, with the evolution towards ultra deep submicro CMOS technologies, the design of complex systems on a chip (SoC) will emerge which are increasingly mixed-signal designs. The desire to do hand-crafted, one-transistor-at-a-time analogue design is increasingly at odds with the current time-to-market constraints and hence the need for more analogue design productivity, practical circuit and layout synthesis, and reliable verification at all levels of the mixed-signal hierarchy.

This tutorial will present the recent progress and current state of the art in design tools and methodologies for complex mixed analogue-digital designs as well as for RF design. Different aspects will be covered by the different presenters, ranging from techniques and methodologies for analogue synthesis both at architectural, circuit and layout level, as well as the recent progress in simulation and modelling for RF designs, as well as methods to analysis substrate noise couplings in mixed-signal ICs.

The techniques will be addressed from a designer point of view, so that the attendees can assess how the techniques could be integrated to improve their current design practice.

Targeted audience:

Practising analogue, RF and mixed-signal designers who want to learn about the new techniques and methodologies that could boost their design
quality and productivity.
CAD professionals responsible for implementing or maintaining analogue, RF or mixed-signal tools or flows.

Monday, 18.09.2000

Registration - 08:30
Morning Session - 09:00 – 12:00
CAD AND METHODOLOGY FOR ANALOGUE AND MIXED-SIGNAL IC DESIGN

Tools for designing analogue building block
Rob Rutenbar, CMU
Digital designs gain tremendous leverage from the existence of robust libraries of reusable building blocks, from gates to cores. Analogue designs are mostly designed from scratch, and rarely reused without significant manual intervention. Recent work on circuit and physical synthesis for cell-level and subsystem-level analogue designs will be covered, with several industrial examples.

High-level design and simulation of mixed-signal telecom system
Georges Gielen, K.U.Leuven
The design of complex mixed-signal systems-on-a-chip requires new design methodologies and design tools to boost the design productivity needed to meet present time-to-market constraints. New methods and flows for high-level architectural design will be revised, as well as the necessary simulation and modelling tools, with emphasis on efficient simulation of telecom frontends, analogue behavioural modelling and power/area/noise estimation.

Afternoon Session - 13:00 – 16:00
MODELING AND ANALYSIS FOR RF AND MIXED-SIGNAL ICs

Modeling and simulation for RF design
Jaijeet Roychowdhury, Lucent Bell Labs
This presentation will focus on the recent progress in modelling and simulation techniques for RF circuits. Present RF simulation methods will be reviewed, including dedicated techniques for phase noise analysis. Also macro-modelling will be covered. In addition, current progress in device modelling for RF applications will be described.

Substrate noise coupling analysis in mixed-signal IC
Francois Clement, Snaketech/Simplex
This presentation will describe the current techniques that are used to analyse the coupling of substrate noise in mixed analogue/digital ICs. Both the sources of noise generation, the mechanisms of propagation in different technologies and the methods to analyse the effect will be described. Techniques to reduce the noise coupling will be assessed.

Friday, 22 September 2000

RF-Circuits

Organiser: Ton Wagemans
Philips RF Business Development Center
Mansfield MA, USA
Christer Svensson
Linköping Technical University, Sweden

The aim of this workshop is to discuss contemporary trends in RF Circuit Techniques, driven by market needs which can be translated into higher demands on linearity for both transmitter and receiver circuits in 2nd and 3rd generation mobile telephony systems. Emerging applications, such as WLAN's, are becoming increasingly popular, creating demands for bandwidth at higher frequencies. Due to semiconductor improvements, new frequency bands in the mm-wave region can be used to build commercial communication systems at reasonable costs. Novel technologies, like Silicon on Anything, have been developed to improve linearity and increase bandwidth of silicon based technologies.

8.00 **Registration**

8.30 **Low power, highly linear RF techniques**
Quiting Huang, ETH, Switzerland

9.15 **Linearisation techniques for RF Power Amplifiers**
Lars Sundström, Lund University, Sweden

10.00 **Coffe break**

10.30 **Bluetooth – a Radio Design Overview**
Sven Mattisson, Ericsson Communication Systems, Sweden

11.15 **60 GHz Wireless – Applications and Research Activities**
Arne Alping, Ericsson Microwave Systems, Sweden

12.00 **Lunch**

13.00 **Novel technologies for future RF communication systems**
Peter Baltus, Philips Semiconductors, The Netherlands

13.45 **Future directions of wireless communications systems**
Panel discussion with all speakers.

14.45 **Concluding remarks**

15:00 **End of Workshop**

Friday, 22.09.2000

Systematic Analogue Design: Hope or Hype?

Organiser: P. Jores
Robert Bosch GmbH, Reutlingen, Germany

The workshop focuses on the results achieved within the MEDEA project SADE (Systematic Analogue Design Environment) in the area of top-down design, modelling, sizing, characterisation and design environments. Three overview presentations will introduce the results of the project partners and be a guided tour to the poster and demonstration session following. There the results will be shown in detail and there will be the opportunity for discussion with the developers.

08:00 **Registration**

08:30 **Welcome and Introduction**

08:45 **Computer-aided Symbolic Analysis and Behavioural Modelling for Systematic Analogue Circuit Design**
R. Sommer
Infineon Technologies AG, Munich, Germany

The presentation gives an overview of the application of symbolic circuit modelling, analysis, and design techniques developed within the research activities of the project. Firstly a top-down design guideline will be presented on an industrial application example and secondly two key problems in systematic circuit design will be addressed: the transfer of specifications between different levels of abstraction and knowledge acquisition for redesign and optimisation.

09:15 **Application of Sizing and Characterisation to Analogue Circuits**
T. Ifström
Robert Bosch GmbH, Reutlingen, Germany

Both sizing and characterisation of analogue circuits have usually been carried out manually and have been very time-consuming. Thus both offer a great potential for efficiency improvement. Different sizing approaches that support either an interactive procedure or a more automated one have been developed in the project will be presented. In addition present tool for automatic characterisation will be introduced.

09:45 **Design Environments Supporting Technology and Reusability**
A. Stürmer
TEMIC Semiconductor GmbH, Ulm, Germany

A well supported and reliable design flow is indispensable for successful work in circuit design. The design flow has to be very general in the basic concept but it has to consider also company specific requirements. This applies for the handling of technology information and data for reusability in particular. The presentation gives a short introduction to two environments.

10:00 **Poster Session and Computer Demonstrations**
incl. Coffee Break

12:00 **Summary, Outlook and Final Discussion**

12:30 **End of Workshop**

Conference Organisation

Chairman:
Hannu Tenhunen, KTH, Sweden
Vice-Chairman:
Mikael Östling, KTH, Sweden
Technical Programme:
Kari Halonen, HUT, Finland
Christer Svensson, LiTH, Sweden
Conference Secretary:
Zandra Lundberg, KTH, Sweden
Local Arrangements:
Elena Dubrova, KTH, Sweden

TECHNICAL PROGRAMME COMMITTEE

Members:

P. Alinikula, Nokia Research Center, Finland
W. Brockherde, Fraunhofer IMS, Germany
E. Bruun, Techn. Univ. of Denmark, Denmark
K. Bult, Broadcom Netherlands, The Netherlands
R. Castello, Univ. of Pavia, Italy
F. Dielacher, Infineon, Austria
E. Dijkstra, Phonak, Switzerland
C. Enz, CSEM, Switzerland
K. Estola, Nokia Research Center, Finland
Q. Huang, ETHZ, Swizerland
J. Huijsing, DIMES, The Netherlands
J. Huisken, Philips Research, The Netherlands
A. Kaiser, IEMN-ISEN, France
R. Koch, Infineon, Germany
J. Kostamovaara, Univ. of Oulu, Finland
T. Lande, Univ. of Oslo, Norway
P. Larsson, Lucent Bell Labs, USA
F. Maloberti, Univ. of Pavia, Italy
S. Mattisson, Ericsson Mob. Comm., Sweden
P. Mole, Nortel Networks, UK
B. Nauta, Univ. of Twente, The Netherlands
T. Noll, RWTH Aachen, Germany
J. Nurmi, Tampere Univ. of Tech., Finland
O. Nys, Xemics, Switzerland
F. Op't Eynde, Alcatel Mietec, Belgium
C. Piguet, CSEM, Switzerland
P. Pirsch, Univ. of Hannover, Germany
R. van de Plassche, TU Eindhoven, NL
W. Pribyl, AMS, Austria
W. Redman-White, Philips Semicond., UK
A. Rodriquez-Vazques, IMSE-CNM, Spain
A. Rothermel, Univ. of Ulm, Germany
S. Rusu, Intel, USA
W. Sansen, K.U.Leuven, Belgium
P. Senn, CNET, France
J. Sevenhans, Alcatel, Belgium
W. Simbürger, Infineon, Germany
M. Steyaert, K.U.Leuven, Belgium
M. Torkelson, Ericsson Radio Systems, Sweden
C. Toumazou, Imperial College, UK
H. Veendrick, Philips Research, NL

Corresponding members:

A. Abidi, UCLA, USA
J. Rabaey, Univ. Berkeley, USA

19.09.00 Room A

09:00 to 09:15 Opening

09:15 to 09:20 ESSCIRC 1999 Best Paper Award

09:20 Invited Paper

Future is in Wireless

Y. Neuvo
Nokia Mobile Phones, Finland

10:10 to 10:40 Coffee Break

Session 1.1: Analogue Integrated Circuits

Chairman: Willy Sansen
Katholieke Universiteit Leuven, Heverlee, Belgium

10:40 Ultra-low Voltage CMOS Cascode Amplifier

T. Lehmann, M. Cassia
Technical University of Denmark, Lyngby, Denmark

11:05 Curvature Compensated BiCMOS Bandgap with 1 V Supply Voltage

P. Malcovati[1], F. Maloberti[1], M. Pruzzi[1], C. Fiocchi[2]
[1]University of Pavia, Italy
[2]Mikron AG

11:30 Front-end Processor Core for up to 64X Speed CD-ROM Drive in 0.35um CMOS

A. Wada, T. Otsuka, K. Tani, T. Sawai
Sanyo Electric Co., Ltd, Anpachi-Gun, Gifu, Japan

11:55 A Dynamically Controllable DC/DC Level Converter and Its Application to High-Speed, Low-Power Circuits

T. Enomoto[1], H. Shikano[1], H. Iwata[1], M. Fujii[2], No. Yoshida[2]
[1]Chuo University, Tokyo, Japan
[2]NEC Corporation, Ibaraki, Japan

12:20 to 14:00 Lunch Break

14:00 Invited Paper
Bluetooth (TM): From Antenna to Silicon
J. Haartsen
Ericsson Radio Systems, The Netherlands

Session 1.2: Low Voltage Analogue Filters
Chairman: Bram Nauta
University of Twente, Enschede, The Netherlands

14:50 A Micropower Class AB CMOS Log-Domain Filter for DECT Applications
D. Python[1], C. Enz[2]
[1]Ukom inc, San Jose, CA, United States
[2]Centre Suisse d'Electronique et de Microtechnique, Neuchatel, Neuchatel

15:15 Low-Voltage Analog Filters using Floating-gate MOSFETs
E.O. Rodriguez-Villegas, A. Rueda, A. Yuúera
Universidad de Sevilla, Spain

15:40 to 16:10 Coffee Break

Session 1.3: Sigma Delta Convertors
Chairman: Bill Redman-White
Philips Semiconductors, Southampton, United Kingdom

16:10 A 400MHz 5th-Order CMOS Continuous-Time Switched-Current Sigma-Delta Modulator
L. Luh, J. Choma, J. Draper
University of Southern California, Los Angeles, CA, United States

16:35 A 1.8V MOSFET-Only Sigma-Delta Modulator Using Compensated MOS-Capacitors in Depletion with Substrate Biasing
Th. Tille[1], J. Sauerbrey[2], M. Mauthe[2], W. Kraus[1], D. Schmitt-Landsiedel[1]
[1]Technical University of Munich, Germany
[2]Infineon Technologies AG, Germany

17:00 A 73dB SFDR 10.7MHz 3.3V CMOS Bandpass Sigma-Delta Modulator sampled at 37.05MHz
P. Cusinato[1], F. Stefani[1], A. Baschirotto[2]
[1]STMicroelectronics, Cornaredo (MI), Italy
[2]University of Lecce, Italy

18:00 to 20:00 Reception

19.09.00 Room B

Session 1.4: RF Transceivers

Chairman: Rudolf Koch
Infineon Technologies, Munich, Germany

10:40 A Low-Power 1GHz Super-Regenerative Transceiver with time-shared PLL control
P. Favre, N. Joehl, P. Deval, M. Declercq, C. Dehollain
Swiss Federal Institute of Technology, Lausanne, Switzerland

11:05 A CMOS 2V Quadrature Direct Up-Converter Chip for DCS-1800 Integration
M. Borremans, M. Steyaert
K.U.Leuven, Heverlee, Belgium

11:30 A 900MHz/1.9GHz Integrated Transceiver and Synthesizer IC for GSM
R. Magoon, J.L. Tham, A. Molnar, B. Pregardier,
M. Margarit, M. Conta, Ja. Cheng, A. Ali, S. Lloyd
Conexant Systems, Inc., Newport Beach, CA, United States

11:55 A 2-GHz Low-Power Single-Chip CMOS Receiver for WCDMA Applications
D. Yee, C. Doan, D. Sobel, B. Limketkai, S. Alalusi,
R Brodersen
University of California, Berkeley, CA, United States

12:20 to 14:00 Lunch Break

Session 1.5: RF CMOS Power Amplifiers

Chairman: Werner Simbürger
Infineon Technologies AG, Munich, Germany

14:50 A Low Stress 20dBm Power Amplifier for LINC Transmission with 50% Peak PAE in 0.2µm CMOS
M. Tarsia[1], J. Khoury[2], V. Boccuzzi[1]
[1]Lucent Bell-Labs, Murray Hill, NJ., United States
[2]Lucent Bell-Labs, Allentown, PA, United States

15:15 A 700MHz, 1W fully differential Class E power amplifier in CMOS
K. Mertens, M. Steyaert, B. Nauwelaers
K.U.Leuven, Heverlee, Belgium

15:40 to 16:10 Coffee Break

Session 1.6: RF Low Noised Amplifiers

Chairman: Qiuting Huang
ETH Zentrum, ETZ, Zürich, Switzerland

16:10 A Universal Dual Band LNA Implementation in SiGe-Technology for Wireless Applications
S. Catala, A. Schmidt
Infineon Technologies AG, Munich, Germany

16:35 A 9mW, 900-MHz CMOS LNA with 1.05dB-Noise-Figure
G. Gramegna, A. Magazzù, C. Sclafani, M. Paparo,
P. Erratico
STMicroelectronics, Catania, Italy

17:00 Using Capactive Cross-Coupling Technique in RF Low Noise Amplifiers and Down-Conversion Mixer Design
W. Zhuo[1], S. Embabi[1], J. Pineda de Gyvez[2], E. Sánchez-Sinencio[1]
[1]Texas A&M University, College Station, TX, United States
[2]Philips Research Laboratories, Eindhoven, The Netherlands

19.09.00 Room C

Session 1.7: Digital Systems and Signaling

Chairman: Stefan Rusu
Intel Corporation, Santa Clara, CA, United States

10:40 A low power reconfigurable 12-tap FIR interpolation filter with fixed coefficient sets
C. Henning, R. Schwann, V. Gierenz, T.G. Noll
University of Technology RWTH Aachen, Germany

11:05 Optimum voltage swing on on-chip and off-chip interconnects
C. Svensson
Linköping University, Sweden

11:30 Itanium(tm) Processor System Bus Design
A. Ilkbahar, S. Venkataraman, H. Muljono
Intel Corp., Santa Clara, CA, United States

11:55 Self Calibrating and Adjustable CMOS Pad Driver for Improved Electromagnetic Compatibility
R. Klein[1], D. Roemer[1], H. Eichfeld[2], H.-J. Pfleiderer[2]
[1]Infineon Technologies AG, Munich, Germany
[2]University of Ulm, Germany

12:20 to 14:00 Lunch Break

Session 1.8: Systems on Chip

Chairman: Christer Svensson
Linköping University, Sweden

14:50 A New Contactless Smartcard IC using an On-Chip Antenna and an Asynchronous Micro-controller
A. Abrial[1], J. Bouvier[1], P. Senn[1], M Renaudin[2], P. Vivet[3]
[1]France Telecom, Meylan, France
[2]TIMA, Grenoble, France
[3]STMicroelectronics, Crolles, France

15:15 Fully Integrated Motor Driver Controller for Hard Disk Drive Using Digital Approach
R. Bardelli[1], L. Fontanella[1], F. Forte[1], G. Frattini[1], G. Martinelli[1], G. Ricotti[1], M. Rossi[2]
[1]STMicroelectronics S.r.l., Cornaredo (MI), Italy
[2]STMicroelectronics, Grenoble, France

15:40 to 16:10 Coffee Break

Session 1.9: Logic Circuits

Chairman: Albrecht Rothermel
Universität Ulm, Germany

16:10 High-Speed and Low-Swing On-Chip Bus Interface Using Threshold Voltage Swing Driver and Dual Sense Amplifier Receiver
B.-D. Yang, L.-S. Kim
Korea Advanced Institute of Science and Technology, Taejon, Korea (South)

16:35 Iterative Self-Timed Multiplier with Early Completion
D.-W. Kim, D.-K. Jeong
Seoul National University, Korea (South)

17:00 Low PowerSelf-Timed Floating-Point Divider in 0.25um Technology
J.-H. Won, K. Choi
Seoul National University, Korea (South)

20.09.00 Room A

08:30 Invited Paper

Software-Radio Base-Stations, A Challenge for Analogue IC-Design

A. Rydin, Ericsson Radio Systems, Sweden

Session 2.1: Audio Circuits

Chairman: Juha Kostamovaara
University of Oulu, Finland

09:20 Battery Supplied Low Power Analog-Digital Front-End for Audio Applications

R. Klootsema[1], O. Nys[1], E. Vandel[1], D. Aebischer[1], P. Vaucher[1], O. Hautier[1], P. Bratschi[1], F. Bauduin[1], G. van Oerle[2], A. Jakob[2], S. Menzl[2]
[1]Xemics SA, Neuchatel, Switzerland, [2]Phonak AG, Stafa

10:10 A 147 dB Dynamic Range Electronic Attenuator for Audiometric Applications with On-Chip 1 W Power Amplifier

S. Brigati[1], F. Francesconi[1], F. Francesconi[1], D. Fumagalli[2], G. Grassi[2], P. Malcovati[3], M. Poletti[1]
[1]Micronova Sistemi S.r.l., Trivolzio, Italy
[2]Amplifon S.p.A., Milan, [3]University of Pavia

10:10 to 10:40 Coffee Break

10:40 Invited Paper

Analogue Design in Deep Submicron CMOS Technology

K. Bult, Broadcom Netherlands B.V., The Netherlands

Session 2.2: Continuos Time Filters

Chairman: A. Rodriguez-Vazquez
University of Seville, Sevilla, Spain

11:30 An Eighth-Order CMOS Lowpass Filter with 30-120 MHz Tuning Range and Programmable Boost

G. Bollati[1], S. Marchese[1], R. Castello[2], M. Demicheli[1]
[1]STMicroelectronics, Cornaredo (MI), Italy
[2]Università di Pavia, Italy

11:55 Programmable direct digital tuning circuit for a continuous-time filter

T. Salo, S. Lindfors, T. Hollman, K. Halonen
Helsinki University of Technology, Espoo, Finland

12:20 to 14:00 Lunch Break

14:00 Invited Paper

SOI CMOS Circuit Design Exposed - Another Dirty Tricks Campaign?

W. Redman-White, Philips Semiconductors, United Kingdom

Session 2.3: Programmable Analogue Filters

Chairman: Erik Bruun
Technical University of Denmark, Lyngby, Denmark

14:50 A 350 MHz Programmable Analog FIR Filter Using Mixed-Signal Multiplier

H. Jin, E.K.F. Lee
Iowa State University, Austin, Texas, United States

15:15 A 2.7V CMOS Dual-Mode Baseband Filter for PDC and WCDMA

T. Hollman, S. Lindfors, M. Länsirinne, J. Jussila, K. Halonen
Helsinki University of Technology, Espoo, Finland

15:40 to 16:00 Coffee Break

20.09.00 Room B

Session 2.4: Linear Receiver Circuits

Chairman: Sven Mattisson
Ericsson Mobile Communication AB, Lund, Sweden

09:20 A High IP3 RF Receiver Chip Set for Mobile Radio Base Stations up to 2 GHz
H.-D. Wohlmuth, W. Simbürger
Infineon Technologies AG, Munich, Germany

09:45 High Performance SiGe Upconverter for Double Conversion Tuner
M. Ipek[1], M. Rieger[2], H. Schemmann[1]
[1]THOMSON multimedia, Villingen-Schwenningen, Germany
[2]University of Applied Sciences Albstadt-Sigmaringen

10:10 to 10:40 Coffee Break

Session 2.5: Low Power ADCs 1

Chairman: Peter J. Mole
Nortel Networks, Harlow, United Kingdom

11:30 1.0-Volt, 9-bit Pipelined CMOS ADC
M. Waltari, K. Halonen
Helsinki University of Technology, Espoo, Finland

11:55 A Low-Power 14-b 5 MS/s CMOS Pipeline ADC with Background Analog Self-Calibration
J. Goes[1], J.C. Vital[1], L. Alves[1], N. Ferreira[1], P. Ventura[1], E. Bach[2], J.E. da Franca[1], R. Koch[2]
[1]Instituto Superior Técnico, Lisbon, Portugal
[2]Infineon Technologies AG, Munich, Germany

12:20 to 14:00 Lunch Break

Session 2.6: Low Power ADCs 2

Chairman: Olivier Nys
Xemics SA, Neuchatel, Switzerland

14:50 12 Bit Low Power Fully Differential Switched Capacitor Non-Calibrating Successive Approximation ADC with 1MS/s
G. Promitzer
Austria Mikro Systeme International AG, Unterpremstätten, Austria

15:15 An 8-bit 13-Msamples/s Digital-Background-Calibrated Algorithmic ADC
E.B. Blecker[1], O.E. Erdogan[2], P.J. Hurst[1], S.H. Lewis[1]
[1]University of California, Davis, CA, United States
[2]C-Cube Microsystems Inc., Milpitas, CA, United States

15:40 to 16:00 Coffee Break

16:00 to 19:30 Poster Session
20:00 to 23:00 Conference Banquet

20.09.00 Room C

Session 2.7: Memory Circuits
Chairman: Jari Nurmi
Tampere University of Technology, Finland

09:20 A Dual-Phase-Controlled Dynamic Latched (DDL) Amplifier for High-Speed and Low-Power DRAMs
H. Fujisawa, T. Takahashi, M. Nakamura, K. Kajigaya
Hitachi Ltd., Tokyo, Japan

09:45 A High-Efficiency Back-Bias Generator with Cross-Coupled Hybrid Pumping Circuit for sub-1.5 V DRAM applications
K.-S. Min, K.-W. Jin, J.-B. Kim
Hyundai Electronics Industries Co., Ltd., Cheongju-Si, Korea (South)

10:10 to 10:40 Coffee Break

Session 2.8: Memories
Chairman: Jari Nurmi
Tampere University of Technology, Finland

11:30 A Low Power Reconfigurable I/O DRAM Macro with Single Bit line Writing Scheme
J. Kook, H.-J. Yoo
Korea Advanced Institute of Science and Technology, Taejon, Korea (South)

11:55 A 1-V, 3.44-ns, 4.1-mW at 50-MHz, 128-Kb Four-Way Set-Associative CMOS Cache Memory Implemented by 1.8V 0.18µm Foundry CMOS Technology for Low-Voltage Low-Power VLSI System Applications
J.B. Kuo[1], P. F. Lin[1], F. Wang[2], H. H. Chang[2], W. T. Wang[2], C. H. Chen[2]
[1]National Taiwan University, Taipei, Taiwan
[2]Taiwan Semiconductor Manufacturing Company

12:20 to 14:00 Lunch Break

Session 2.9: Fully Integrated Synthesizers
Chairman: Franz Dielacher
Infineon Technologies AG, Villach, Austria

14:50 A 2-V 900-MHz Monolithic CMOS Dual-Loop Frequency Synthesizer for GSM Wireless Receivers
W.S.-T. Yan, H.C. Luong, Howard Luong
Hong Kong University of Science & Technology, Kowloon, Hong Kong

15:15 Measurements and Analysis of PLL Jitter Caused by Digital Switching Noise
P. Larsson
Bell Labs, Lucent Technologies, Holmdel, NJ, United States

15:40 to 16:00 Coffee Break

20.09.00 Poster Room

16:00 to 19:30 Poster Session

Split-Drain MOST Based Circuit for Measuring Electric Power
C.A. dos Reis Filho[1], Carlos Alberto dos Reis Filho[2]
[1]State University of Campinas, Campinas, SP, Brazil
[2]Faculty of Electrical Engineering, UNICAMP

Low Power Column ADC for CMOS Imagers
A. van der Avoird, M. Vertregt
Philips Research Laboratories, Eindhoven, The Netherlands

Ultra Low Power A/D Converters Using an Enhanced Differential Charge-Transfer Amplifier
W.J. Marble, D. Comer
American Microsystems, Inc., American Fork, United States

SiGe Track-and-Hold with HD3=-87dBFS for fck=110MHz, fin=(110MHz-1kHz) and Vin=1Vpp,diff
V. Dias[1], U. Gatti[2], F. Maloberti[3]
[1]Infineon Technologies AG, Munich, Germany
[2]Siemens ICN S.p.A., Milano, Italy
[3]University of Pavia, Italy

A 2.5 Volt 6 bit 600MS/s Flash ADC in 0.25µm CMOS
P. Scholtens
Philips Research Laboratories, Eindhoven, The Netherlands

An 8-bit, 1-Gsample/s Folding-Interpolating Analog-to-Digital Converter
W. An, C.A.T. Salama
University of Toronto, Toronto, Ontario, Canada

A 2.7V 50 MHz IF-Sampling Delta-Sigma Modulator with +37dBV IIP3 for Digital Cellular Phones
S. Lindfors[1], M. Länsirinne[2], K. Halonen[2]
[1]KTH, Kista, Sweden
[2]Helsinki University of Technology, Finland

Adaptive Noise Shaping ADC Based on LMS Algorithm
J. Koh, G. Han, S.H.K. Embabi, F. Maloberti[2]
Texas A&M University, College Station, TX, United States

A digitally programmable burst-mode 155 Mb/s transmitter for PON
M. Doci[1], C. Fiocchi[1], U. Gatti[2], A. Profumo[1], G. Promitzer[3]
[1]Italtel
[2]Siemens ICN S.p.A., Milano, Italy
[3]AMS, Austria

A 0.8 µm SOI CMOS On-Board Data Handling Bus Modem for Satellite Applications
R. Boi[1], S. Brigati[2], F. Francesconi[2], C. Ghidini[3],
P. Malcovati[1], F. Maloberti[1], M. Poletti[2]
[1]University of Pavia, Italy
[2]Micronova Sistemi S.r.l., Trivolzio, Italy
[3]LABEN S.p.A., Vimodrone, Italy

A 12GHz /128 frequency divider in 0.25µm CMOS
B. De Muer, Michiel Steyaert
K.U.Leuven, Heverlee, Belgium

An 18-mW 2.5-GHz/900-MHz BiCMOS Dual Frequency Synthesizer with < 10-Hz RF Carrier Resolution
W. Rhee[1], B. Bisanti[2], A. Ali[1]
[1]Conexant Systems, Inc., Newport Beach, CA, United States
[2]Texas Instruments, Nice, France

A 500MHz Supply Noise Insensitive CMOS PLL with a Voltage Regulator using DC-DC Capacitive Converter
C.-H. Lee[1], Ke. McClellan[2], J. Choma[3]
[1]Conexant Systems, Inc., Irvine, CA, United States
[2]Entridia
[3]University of Southern California, Los Angeles, U.S.A.

A Novel Structure for DCO PLLs with Equivalent 16 Bit Digital Phase Quantization, Digital Loop Filter and 18ps Long-term Jitter
C. Sandner[1], N. Da Dalt[1], Nicola Da Dalt[2]
[1]Infineon Technologies, Villach, Austria
[2]Infineon Technologies MDCA

A Channel Selection Filter for a WCDMA Direct Conversion Receiver
J. Jussila[1], A. Pärssinen[2], K. Halonen[2]
[1]Helsinki University of Technology, Espoo, Finland
[2]Helsinki University of Technology/ECDL

CMOS Switched-Capacitor Decimation Filter for Mixed-Signal Video Applications
F. A. P. Barúqui[1], A. Petraglia[1], J. E. Franca[2], S.K. Mitra[3]
[1]Federal University of Rio de Janeiro, Brazil
[2]Instituto Superior Técnico, Lisbon, Portugal
[3]University of California, Santa Barbara, USA

A CMOS gm-C Polyphase Filter with High Image Band Rejection
P Andreani[1], S. Mattisson[1], B. Essink[2]
[1]Lund University, Sweden
[2]Ericsson Business Mobile Networks, Enschede, The Netherlands

A CMOS Switched-Capacitor Bandpass Filter with 100 MSample/s Input Sampling and Frequency Downconversion
R. Ferreira Neves, J.E. da Franca
Instituto Superior Técnico, Lisbon, Portugal

A Hilbert sampler/filter and complex bandpass SC filter for I/Q demodulation
S. Karvonen, J. Kostamovaara, T. Riley
University of Oulu, Finland

A low-distortion digitally programmable continuous-time filter and variable-gain amplifier
S. Celma, J. Sabadell
Universidad de Zaragoza, Spain

An Analog CMOS High-Speed Continuous-Time FIR Filter
E. Burlingame, R. Spencer
University of California, Davis, CA, United States

APD Implementation to GHz Range Receiver Channel for a Pulsed Time-of-Flight Laser Radar
R. Pennala, A. Kilpelä, J. Kostamovaara
University of Oulu, Finland

A low-power microphone preamplifier with EMI canceling
G. Reitsma, M. Kouwenhoven, A. Mosterd
Delft University of Technology, The Netherlands

A 2.8V 200MHz Replicating Current Comparator for Convolutional Decoders
A. Demosthenous, J. Taylor
University College London, United Kingdom

New Regulated Voltage Down Converter based on Modified Band-Gap Cells
E. Kuessner[1], H. Barthélémy[1], A. Kaiser[2], A. Roberts[3], A. Malherbe[3]
[1]ISEM, Toulon, France
[2]IEMN-ISEN, France
[3]STMicroelectronics, Rousset

A 2GHz Low-Distortion Low-Noise Two-Stage LNA Employing LowImpedance BiasTerminations and Optimum Inter-Stage Match for Linearity
P. Shah, P. Gazzerro, V. Aparin, R. Sridhara, C. Narathong
Qualcomm Inc., San Diego, CA, United States

A high Dynamic Range 3.4 GHz CMOS micropower mixer
P. Vancorenland, P. Coppejans, W. De Cock, M. Steyaert
K.U.Leuven, Heverlee, Belgium

Generating All 2-Transistor Circuits Leads to New Wide-Band CMOS LNAs
F. Bruccoleri, E.A.M Klumperdinck, B. Nauta
University of Twente, Enschede, The Netherlands

A Self-Calibrating 900-MHz CMOS Image-Reject Receiver
R. Montemayor, B. Razavi
University of California, Los Angeles, CA, United States

A New Small Signal Modeling of RF MOSFETs including Charge Conservation Capacitances
I. Kwon, M. Je, K. Lee, H. Shin
Korea Advanced Institute of Science and Technology, Taejon, Korea (South)

Influence of substrate noise on RF performance
D. Leenaerts, P. de Vreede
Philips Research Laboratories, Eindhoven, The Netherlands

A 2.7 V, 8 GHz Monolithic I/Q RC Oscillator with Active Inductive Loads
J. van der Tang[1], D. Kasperkovitz[2], F. Centurelli[3], A. van Roermund[1]
[1]Eindhoven University of Technology, The Netherlands
[2]Philips Research Laboratories, The Netherlands
[3]University of Rome "La Sapienza", Italy

5 GHz Low-Noise Bipolar and CMOS Monolithic VCOs
H. Jacquinot, J. Majos, P. Senn
France Telecom, Meylan, France

A Fully Integrated Sub-1 V 4 GHz CMOS VCO, and a 10.5 GHz Oscillator
A.H. Mostafa, M.N. El-Gamal
McGill University, Montreal, Canada

Dynamically Programmable Parallel Processor (DPPP): A Novel Reconfigurable Architecture with Simple Program Interface
B.-K. Tan, R. Yoshimura, T. Matsuoka, K. Taniguchi
Osaka University, Japan

Transition Pattern Coding: An approach to reduce Energy in Interconnect
P. Sotiriadis, A. Wang, A. Chandrakasan
Massachusetts Institute of Technology, Cambridg, MA, United States

Accurate A Priori Signal Integrity Estimation Using A Multilevel Dynamic Interconnect Model for Deep Submicron VLSI Design
L.-R. Zheng, D. Pamunuwa, H. Tenhunen
Royal Institute of Technology, Kista, Sweden

Investigation of Cell Leakage and Data Retention in eDRAM
M. Hashimoto[1], Robert Baumann[2]
[1]Cadence Design Systems, Yokohama, Japan
[2]Texas Instruments

Source-Pulsed Dynamic-Threshold CMOS SRAMs for Fast, Portable Applications
A.J. Bhavnagarwala[1], A. Kapoor[2], J.D. Meindl[1]
[1]Georgia Institute of Technology, Atlanta, GA, United States
[2]LSI Logic Corporation, Milpitas, CA, United States

A Low-Power SRAM with Resonantly Powered Data, Address, Word, and Bit Lines
N. Tzartzanis[1], W. Athas[2], L. Svensson[3]
[1]USC - Information Sciences Institute, Marina del Rey
[2]House Ear Institute, Los Angeles, CA, United States
[3]SwitchCore, Lund, Sweden

Super-Compact Shared-Cache Memories with Low Power Consumption for Multi-Issue Single Chip Processors
K. Kishi, T. Gyohten, J. Kim, H.J. Mattausch, Y. Tatsumi, S. Nara
Hiroshima University, Higashi-Hiroshima, Japan

Nonvolatile CMOS Latch Employing GMR Resistors
B. Das[1], K.A. Wong[2], W.C. Black[1]
[1]Iowa State University, Ames, Iowa, United States
[2]Texas Instruments Inc., Dallas, TX, United States

Dynamic Flip-Flop with Improved Power
N. Nedovic[1], V.G. Oklobdzija[1], Vojin Oklobdzija[2]
[1]University of California, Berkeley, CA, United States
[2]UC Davis, ECE Department, Davis CA, United States

20:00 to 23:00 Conference Banquet

21.09.00 Room A

08:30 Invited Paper

Future Trends in Automotive Electronics, Sensors and Communication Systems

K.-T. Neumann
Volkswagen AG, Germany

09:20 to 09:25 ESSCIRC 2001

Session 3.1: Medical Sensor Systems

Chairman: Johan H. Huijsing
Delft University of Technology, The Netherlands

09:25 A Programmable Intraocular CMOS Pressure Sensor System Implant

K. Stangel, S. Kolnsberg, D. Hammerschmidt, B.J. Hosticka, H.K. Trieu, W. Mokwa
Fraunhofer Institute of Microelectronic Circuits and Systems, Duisburg, Germany

09:50 A low-power ASK demodulator for inductively coupled implantable electronics

G. Gudnason[1], Gunnar Gudnason[2]
[1]Technical University of Denmark, Lyngby, Denmark
[2]Dept of IT, Technical University of Denmark

10:15 to 10:45 Coffee Break

10:45 Invited Paper

VDSL, From Concept to Chips

P. Spruyt
Alcatel Research, Belgium

Session 3.2: Integrated Smart Sensors

Chairman: Werner Brockherde
Fraunhofer IMS, Duisburg, Germany

11:35 SC Interface and Calibration Circuit for a CMOS Humidity Sensor

Y. Qiu, K.P. Pun, C. Azeredo Leme, J. da Franca
Instituto Superior Técnico, Lisbon, Portugal

12:00 A Position Detection Sensor for 3-D Measurement

T. Nezuka[1], M. Hoshino[2], M. Ikeda[3], K. Asada[3]
[1]University of Tokyo, Japan
[2]Matsushita Electrical Industrial Co. Ltd.
[3]VLSI Design and Education Center

12:25 to 14:00 Lunch Break

14:00 Invited Paper
3-D Ics: Motivation, Performance Anlaysis and Technology
K. Saraswat
Stanford University, United States

Session 3.3: Logic Circuit Techniques
Chairman: Tobias G. Noll
RWTH Aachen, Germany

14:50 A Skew-Tolerant Design Scheme for Over 1-GHz LSIs
Y. Hagihara[1], S. Inui[1], A. Yoshikawa[1], T. Uesugi[2], T. Osada[2], S. Nakazato[3], M. Ikeda[4], M. Okada[4], S. Yamada[3]
[1]NEC Corporation, Sagamihara, Japan
[2]NEC Kofu, Ltd., Yamanashi
[3]NEC Corporation, Tokyo
[4]NEC Corporation, Kanagawa

15:15 A Novel High Speed Low Power Logic Family: Race Logic
S.J. Lee, H.J. Yoo
Korea Advanced Institute of Science and Technology, Taejon, Korea (South)

15:40 Skewed CMOS: Noise-Immune High-Performance Low-Power Static Circuit Family
A. Solomatnikov[1], D. Somasekhar[2], K. Roy[1]
[1]Purdue University, West Lafayette, IN, United States
[2]Intel Corp., Portland, OR, United States

16:05 to 16:30 Young Scientists Award & Closing Session

21.09.00 Room B

Session 3.4: Optical Receivers

Chairman: Bram Nauta
University of Twente, Enschede, The Netherlands

09:25 A Receiver Channel with a Leading Edge Timing Discriminator for a Pulsed Time-of-Flight Laser Radar
Te. Peltola, T. Ruotsalainen, P. Palojärvi, J. Kostamovaara
University of Oulu, Finland

09:50 A packaged low-noise high-speed regulated cascode transimpedance amplifier using 0.6µm N-well CMOS technology
S.M. Park, C. Toumazou
Imperial College, London, United Kingdom

10:15 to 10:45 Coffee Break

Session 3.5: High Speed ADCs

Chairman: Klaas Bult
Broadcom Netherlands B.V., Bunnik, The Netherlands

11:35 A 1.8V 20mW 1mm² 14b 100MSample/s CMOS DAC
M.P. Tiilikainen, Mika Petri Tiilikainen
Nokia Mobile Phones, Helsinki, Finland

12:00 A 10-bit 200 MS/s CMOS Parallel Pipeline A/D Converter
L. Sumanen, M. Waltari, K. Halonen
Helsinki University of Technology, Espoo, Finland

12:25 to 14:00 Lunch Break

Session 3.6: VCO Circuits

Chairman: Michiel Steyaert
ESAT MICAS, Heverlee, Belgium

14:50 A differentially tuned 1.73-GHz-1.99GHz Quadrature CMOS VCO for DECT, DCS1800 and GSM900 with a phasenoise over tuning range between -128dBc/Hz and -137dBc/Hz at 600kHz offset
M.J.G. Tiebout[1], Marc J. G. Tiebout[2]
[1]Infineon Technologies AG, Munich, Germany
[2]Infineon Technologies AG, Department Wireless

15:15 A Comparison of MOS Varactors in Fully-Integrated CMOS LC VCO's at 5 and 7 GHz
Herschel Ainspan, Herschel Ainspan, Jean-Olivier Plouchart
IBM T.J. Watson Research Center, Yorktown Heights, NY, United States

16:05 to 16:30 Young Scientists Award & Closing Session

21.09.00 Room C

Session 3.7: Wireless Modesm ASICs

Chairman: Jos Huisken
Philips Research Laboratories, Eindhoven, The Netherlands

09:25 A Low-Voltage Low-Power 0.25µm CMOS ADSL Analog Front-End IC
R. Kokozinski[1], M. Bresch[1], A. Kemna[1], D. Hammerschmidt[1], B. Klein[1], J. Niederholz[1], M. Hesener[1], B. Hosticka[1], D. Teßmann[1], K. Oda[2], K. Sato[2], K. Tagami[2], H. Yamauchi[2], H. Eichel[3], T. Iwamoto[3]
[1]Fraunhofer Institute of Microelectronic Circuits and Systems, Duisburg, Germany
[2]Toshiba Corporation, Kawasaki, Japan
[3]Toshiba Electronics Europe, Düsseldorf

09:50 A Mixed-Signal CMOS MODEM ASIC for Data Transmission on the Low-Voltage Power-Line with Sensitivity of 283µVrms at 10 Kbps
A. Rodríguez-Vázquez, R. Domínguez-Castro, M. Delgado-Restituto, G. Liñán, R. del Río, J. Ceballos, A. Acosta, J. Ramos
Instituto de Microelectronica de Sevilla, Spain

10:15 to 10:45 Coffee Break

Session 3.8: High Speed Interfaces

Chairman: Patrice Senn
France Telecom / CNET, Meylan, France

11:35 LVDS I/O Cells with Rail-to-Rail Receiver Input for SONET/SDH at 1.25Gb/s
U. Vogel[1], R. Jähne[1], S. Ulbricht[1], G. Bunk[1], M. Steinert[2], C. Zimmermann[2], T. Iwamoto[2], R. Kokozinski[3]
[1]Fraunhofer Institute for Microelectronic Circuits, Dresden, Germany
[2]Toshiba Electronics Europe, Düsseldorf
[3]Fraunhofer Institute for Microelectronic Circuits, Duisburg

12:00 A 10 Gb/s, 120/60 mA Laser/Modulator Driver IC with Dual-mode Actively Matched Output Buffer
Ha. Ransijn, G. Salvador, D. Daugherty, K. Gaynor
Lucent Technologies, Reading, PA, United States

12:25 to 14:00 Lunch Break

Session 3.9: Digital PLL Realisisations

Chairman: Patrick Larsson
Bell Laboratories, Holmdel, NJ, United States

14:50 New Fast-Lock PLL for mobile GSM GPRS applications
B. Memmler[1], E. Goetz[1], G. Schoenleber[2]
[1]Infineon Technologies, Munich, Germany
[2]GME

15:15 A 2 GHz Delta-Sigma Fractional-N Frequency Synthesizer in 0.35µm CMOS
R. Ahola, K. Halonen
Helsinki University of Technology, Espoo, Finland

15:40 An Analogue Delay Line for Virtual Clock Enhancement in DDS
R. Richter, H.-J. Jentschel
TU Dresden, Germany