IP2 “Anode Hole Generation Mechanisms”

Andrea Ghetti (ST Microelectronics, Italy), Muhammad A. Alam and Jeff Bude (Agere Systems, USA)

According to the Anode Hole Injection model, holes generated into the anode and tunneling back wear out the oxide leading eventually to breakdown.
In this talk, anode hole creation by photo-generation and impact ionization is investigated by means of experiments and simulations. Although it has been reported recently that a large number of holes can be photo-generated in the cathode, we experimentally show, for the fist time, that the number of photo-generated hole in the anode is negligible with respect to the ones created by impact ionization.
Then, it is shown that minority ionization (when secondary electron is in the valence band) significantly enhances hole generation and it is at the basis of the breakdown polarity dependence.

IP3 “From space to ground : Soft error rate (SER) in commercial microelectronic devices”

P. Calvel (Alcatel Space, France), J. Gasiot (CEM, University of Montpellier, France)

In space, Soft Error Rate (SER) have been observed since a long time, this phenomena is fully characterized, the underlying basic mechanisms are well understood, and hardening solutions have been developed. Soft errors are digital non destructive functional errors that are of increasing concern for electronic devices used on earth for high reliability applications. When a charged particle is stopped in or next to the sensitive part of the devices, the resulting displaced electrons may cause a logic change and an error propagation at the system level. The vulnerability of a device regard to soft errors is increasing with the ion fluence and mass. In space, the electronic circuits are in a severe environment, at ground level the relevant particles are quite softer, so the concern for SER is more recent and related to an increase in sensitivity for the present devices. From a general point of view, there is no difference between the mechanisms inducing soft errors at ground level or in space. The long experience in getting space electronic systems resistant to this phenomena can be of a direct use for ground applications.
Both the cosmic rays impinging the atmosphere and the natural radioactive isotopes always present in materials are well known to induce energetic ions at the device level. Cosmic rays induced neutrons and alpha unwanted nucleus emitters are the two relevant parts of the ground level environment inducing SER. To limit the increase in the SER measured in the latest advanced microelectronic devices, the radiation ground effects have been considered at the fab level, and device, circuit and system hardening methods have been applied. We must maintain our interest for radiation effects in electronic devices at ground level as a raise in the SER is currently measured as the device integration increase.

IP5 “Scanning Probe Microscopy in Semiconductor Failure Analysis”

.B Ebersberger; A. Olbrich; C. Boit (*Infineon technologies, Germany)*

Within the last few years Scanning Probe Microscopy (SPM) has developed into an essential imaging tool for semiconductor process control and failure analysis due to its unique features and diverse applications. E.g., topography imaging with Atomic Force Microscopy (AFM) is indispensable whenever 3-dimensional and quantitative surface information combined with unsurpassed resolution is needed. Various new SPM techniques can measure different electrical parameters like capacitance, potential or current. This offers previously inaccessible insights into the nanoscopic construction of semiconductors. For the first time 2-dimensional maps of physical parameters like oxide thickness, doping, temperature or current in a working IC can be obtained at sub-micron to nanometer resolution. By this SPM greatly enhances the possibilities of failure analysis to find faults and control processes.

IP6 “InP IC technologies for 40 Gbit/s transmission: progress towards maturity”

A. Scavennec (OPTO+, France)

InP microelectronics is emerging as a technology well-suited for the optoelectronic transmitters and receivers to be used in optical transmission systems operating at 40 Gbit/s per channel and above. In such applications very high-speed transistors are required for the digital parts, while output voltages of a few Volts are needed to drive electrooptic modulators. Actually InP is bringing performances in cut-off frequencies and output voltage which SiGe

and GaAs cannot offer. Record cut-off frequencies (> 300 GHz) have been reported for both High Electron Mobility Transistors (HEMTs) and Heterojunction Bipolar Transistors (HBTs), and ICs operating over 40 Gbit/s have been demonstrated (by NTT using the HEMT technology for exemple).
However, since the InP microelectronics technology is rather new and even though promising data has been reported, for instance by TRW and HRL, reliability issues are still open. This can be partly associated to the sensitivity of the fragile InP and related compounds to technological processes, but also to intrinsic characteristics of the materials used in the heterojunctions involved in the various device structures. As exemples; topics of present interest include HBT passivation, often performed using polyimide due to the rather poor efficiency of SiN or SiO_2 processes, and hot electron effects in HEMTs, inducing kink effects and access resistance degradation. The current status and recent progress on those topics will be discussed.

IP7 "Effects of Temperature and Humidity on the Reliability of Interfaces in Microelectronic Devices"
M. Lane (IBM TJ Watson Research Center, USA)

Environmental factors such as temperature and moisture may have deleterious effects on the reliability of interfaces commonly found in microelectronic devices. Specifically, moisture enhanced subcritical debond growth may occur at driving forces greatly reduced from those necessary for catastrophic or abrupt failure. This work reports on the phenomenon of subcritical delamination at both barrier/dielectric and polymer/SiO_2 interfaces and rationalizes the observed behavior in terms of the salient chemical reactions occurring at the debond tip.

IP8 "The connection beween thermal and mechanical stresses in BGA component reliability testing"
M. Ignat. (LTPCM/INP Grenoble, France)

In service stress conditions, the incompatibilities among the Materials consisting a microelectronic device, can drive it to it's failure. Even though predictive information on thermomechanical stresses can be gathered by numerical modelling, rather often a gap subsists between the modelling results, and the observed microstructures related to the mechanisms that cause the failure.
For example, the nucleation of cracks, which cause rupture and delaminations in devices, can be understood when taking into account the effects that either solid state reactions (segregation, precipitation at or near interfaces…), or internal microstructural defects (voids, impurities…) could produce. These mentioned mechanisms are not predictable from classical thermomechanical modelling. Consequently, and for reliability purposes, it is generally suitable to combine/confront any theoretical modelling, with fine micromechanical experimental analysis.
Because the chip on substrate interconnections, present a variety of forms and consisting materials, they are one of the key issues when improving a device performances. In order to understand how spherical type interconnections respond to external/internal solicitations, we developed an experimental methodology to identify and understand the mechanisms causing their mechanical failure.

IP9 "Thermal management and reliability of multi-chip power modules"
G. Lefranc (Siemens, Germany)

The most important requirements on power modules are high electrical insulation and effective dissipation of the thermal losses during operation. The placement of semiconductor components on metallized ceramics essentially solves the problem of electrical insulation safely and reliably. The aluminium oxide and nitride ceramics used possess a high thermal conductivity in addition to their high electrical insulation and thus contribute to effective dissipation of thermal losses from the chip. However, the ceramic substrates are not the only contributors to the thermal resistance of the modules. An overview of thermal management solutions will be given with consideration of particular requirements such as very high specific power dissipation, low maximum chip temperature and distribution of the parallel-connected heat sources on a large surface area. The effect of the various elements of the thermal path between heat source and heat sink on the reliability of the module will be analyzed.