ITG Informationstechnische Gesellschaft im VDE
Information Technology Society of VDE

ESREF 2000

11th EUROPEAN SYMPOSIUM ON RELIABILITY OF ELECTRON DEVICES, FAILURE PHYSICS AND ANALYSIS

DRESDEN – GERMANY
2 – 6 OCTOBER 2000

ITG VDE IEEE Electron Devices Society

Dresden – “Florence on the Elbe” and Centre of “Saxon Silicon Valley”

Dresden was founded in 1206 and entered recorded history ten years later. During the 17th and 18th century (Baroque period) under the regency of Friedrich August 11 (Augustus the Strong) and his son Dresden became a centre of art and culture.

As a residence of the kings of Saxony Dresden was called the “Florence on the Elbe” and was one of the most beautiful cities in Europe because of its Baroque and Renaissance architecture and art treasures.

During World War II the town was almost completely destroyed.

Today the “Old Town” (Altstadt) and the “New Town” (Neustadt) form the heart of Dresden. The city is a unique cluster of historical buildings in Baroque and Rococco style, churches and parks, for example the “Royal Palace” (Schloss), the “Court Church” (Hofkirche), the Church of the Holy Cross“ (Kreuzkirche) or the “Church of the Epiphany” (Dreikönigskirche). The “Church of Our Lady” (Frauenkirche) destroyed during World War II is actually under reconstruction.

Dresden accommodates numerous art galleries and museums - the famous “Zwinger”, the Old Masters and Modern Masters Picture Galleries or the treasure chamber “Green Vault” (Grünes Gewölbe). Here you will find Renaissance and Baroque paintings by Italian and Dutch masters like Raphael, Tizian, Rembrandt and Rubens as well as masterpieces by German painters like Dürer, Cranach and Caspar David Friedrich.

Dresden is a city of music and theatre. Composers like Johann Sebastian Bach, Heinrich Schütz, Robert Schumann, Richard Wagner and Carl Maria von Weber and as well as writers like Friedrich Schiller and Johann Wolfgang von Goethe were inspired by the city. Operas by Richard Strauss had their first public performances in the Opera House (“Semper Oper”).

Saxon's innovative spirit has longstanding tradition. A lot of products which are nowadays part of our daily life were invented in Dresden, like condensed milk, coffee filter paper or tea bags, as well as picture post cards, beer mats and filter cigarettes.

The city is traditionally dominated by industries of high value-added manufacturing. Dresden's industry is manufacturing electronic and electrical equipment, precision and optical instruments and machinery. During the last years high-technology enterprises settled in the capital of Saxony bringing the dream of a “Saxon Silicon Valley” within grasp.

Take the chance to spent some more hours in this city with an unique collection of picturesque baroque and rococco sightseeing objects and a concentration of some of the most modern silicon based plants in Europe.

For detailed information on Dresden visit the homepage

http://www.dresden.de

Welcome to ESREF 2000 in Dresden

ESREF 2000 will take place in a most appropriate environment

- in Dresden, which represents high technology and research combined with cultural heritage.

The organizing committee looks forward to giving you a hearty welcome here.

The programme covers the reliability issues of microelectronic components and modules corresponding to their extending application areas and conditions. The considered product groups and technologies refer to Signal and Power Silicon Devices, Compound Semiconductors, Micro-Mechanics, Packaging and Assemblies together with the advances of Characterisation and Analysis Techniques.

The programme committee was able to structure the sessions (oral and poster) based on a rich contribution of submitted papers and highlight individual topics by invited experts. The best contributed paper will be honoured by an award.

Workshops on power devices, micro-systems, and ESD provide space for exchange of experience.

In addition to the main programme, tutorials provide the opportunity to be introduced into selected topics on reliability physics and management or to be up-dated on them. They are intended as a means of education and training, partly as a continuous programme but also considering topics of actual importance.

Also two user group meetings are organised in conjunction with ESREF for interfacing between existing user groups and conference attendees interested in these areas.

The equipment demonstrations provide a platform for information and learning about latest equipment and software developments. Attendees are encouraged to contact demonstrators prior to the conference and to make arrangements for specific questions, if desired.

Finally, as Dresden is a most attractive place it will also be enjoyable for your spouses. To make your stay enjoyable, please consider that the city has a high visitors attraction and make your registration and reservation in time.

The organising committee appreciates that the conference preparation can be based largely on voluntary efforts with the intention to offer to the microelectronics reliability community an effective programme by the contributions of the speakers and co-authors and invites you heartily for attendance.

L. J. Balk W. H. Gerling E. Wolfgang

Organizing Committee

Actual Information: http://www.vde.com/ESREF2000

Conference Venue
Hotel Westin Bellevue
Grosse Meissner Str. 15
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Organisation

ITG – Information Technology Society of VDE
WG Quality and Reliability of Integrated Circuits
in co-operation with
GMM VDE/VDI-Society Microelectronics
IEEE – Electron Devices Socity

Conference Organisation and Secretariat/Pre-Registration

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ESREF 2000 Scientific Conference Secretariat

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Organizing Committees

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Design for Reliability

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J. Bisschop	Philips, The Netherlands
P. Charpenel	Aerospatiale Matra Airbus, France
G. Deleuze	Thomson TTM, France
O. Hallberg	Ericsson Telecom, Sweden
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Failure Mechanisms

A. J. Mouthaan	University of Twente, The Netherlands
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O. Bonnaud	University of Rennes, France
H. Gieser	FhG-IFT, Germany
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J. Lloyd	Jet Propulsion Laboratories, USA
N. Stojadinovic	University of Nis, Yugoslavia,
E. Vincent	ST Microelectronics, France

Fault Localisation

W. Claeys	University of Bordeaux I, France
R. Cramer	ALTIS Semiconductor, France
S. Dilhaire	University Bordeaux I, France
H. Fujioka	University Osaka, Japan
S. Görlich	Infineon Technologies, Germany
E. Gornik	Technical University Vienna, Austria
R. Heiderhoff	University Wuppertal, Germany
W. Mertin	University Duisburg, Germany

Packaging, Assemblies and Reliability

Y. Danto	University Bordeaux, France
K. Weide	University Hannover, Germany
M. Brizoux	Thomson-CSF, France
J. Lasseur	Schlumberger Ltd, France

Silicon Devices

P. Seegebrecht	University of Kiel, Germany
J. Van der Pol	Philips, The Netherlands
F. Balestra	Enserg, France
A. ten Cate	Philips, The Netherlands
U. Hartmann	Techn. University Ilmenau, Germany
R. Thewes	Infineon Technologies, Germany
G. Van den Bosch	IMEC, Belgium
H. Vogt	FhG-IMS, Germany

Product Realisation

D. Schmitt-Landsiedel	Techn. University Munich, Germany
F. G. Kuper	Philips Semiconductors, The Netherlands
H. Gieser	Fraunhofer-IZM-Munich, Germany
A. Mathewson	NMRC, Cork, Ireland
P. Perdu	CNES, France
K. J. Veelenturf	Philips Semiconductors, The Netherlands

Power Devices and High Temperature Electronics

M. Ciappa	ETH Zürich, Switzerland
W. Wondrak	DaimlerChrysler, Germany
H. Berg	Eupec, Germany
P. Cova	University of Parma, Italy
B. Cascone	University of Naples, Italy
G. Coquery	INRETS, France
D. Flandre	Cath. University Leuwen, Belgium
E. Herr	ABB Semiconductors, Switzerland
H. L. Hartnagel	Techn. University Darmstadt, Germany
P. Jacob	EMPA Zürich, Switzerland
F.-J. Niedernostheide	Siemens, Germany
S. Ramminger	Siemens, Germany
Dr. Scheuermann	Semikron, Germany
N. Seliger	Siemens, Germany
R. Sharp	AEA Technology, UK
D. Wagner	Alstom Transport, France
E. Wolfgang	Siemens, Germany

Compound Semiconductors

N. Labat	University Bordeaux, France
E. Zanoni	University of Padua, Italy
W. T. Anderson	Naval Research Lab., Washington, USA
C. Canali	Università di Modena, Italy
J. M. Dumas	ENSIL – University of Limoges, France
M. Fukuda	NTT Optoelectronics Lab., Japan
F. Garat	ESTEC – ESA, The Netherlands
G. Gregoris	Alcatel Espace, France
J.-L. Goudard	Alcatel Optronics, France
H. L. Hartnagel	Techn. University Darmstadt, Germany
B. K. Jones	Lancaster University, UK
A. Rezazadeh	King's College London, UK
L. K. J. Vandamme	Univ. of Technology Eindhoven, The Netherlands
M. Vanzi	University of Cagliari, Italy

Physical Failure Analysis

E. Zschech	AMD, Germany
M. Vanzi	University of Cagliari, Italy
W. Tittes	Infineon Technologies, Germany
E. Langer	AMD Dresden, Germany

Official Conference Language
The conference language is English. Simultaneous translation will not be available.

Schedule of activities

Sunday, Oct 1, 2000	
Registration	18:00 – 20:00
Monday, Oct. 2, 2000	
Registration	8:30 – 18:30
User Group Meetings	9:00 – 17:00
Tutorials	13:00 – 18:30
Tuesday, Oct. 3, 2000	
Registration	8:00 – 17:30
Tutorials	8:00 – 12:30
Equipment Demonstrations	13:00 – 18:00
Opening Session	14:00 – 15.40
Plenary Session	16:00 – 18:00
Cocktail at Demonstration Area	18:30 – 20:00
Wednesday, Oct. 4, 2000	
Registration	8:00 – 18:00
Technical Sessions	8:30 – 18:00
Equipment Demonstrations	9:30 – 18:00
Semper Opera	19:30
Thursday Oct. 5, 2000	
Registration	8:00 – 17:00
Technical Sessions	8:30 – 18:30
Poster Session	14:30 – 16:00
Workshops	17:00 – 18:30
Equipment Demonstrations	9:30 – 18:00
Conference Dinner	19:30 – 22:00
Friday Oct. 6, 2000	
Registration	8:00 – 14:00
Technical Sessions	8:30 – 13:20
Closing session with Award Presentation	13:20 – 14:00

On Wednesday evening (Oct. 4) there is the opportunity to visit the famous **Semper Opera.** A limited block of tickets has been reserved for attending :

Mozart and Themes of "As You Like it" (Ballet)
(preliminary programme).

Please book this event on the registration form. Registration will be made on first-come-first-serve basis. Ticket: DM 55.–

For further **social programme** options please see the last pages of this programme booklet.

Conference Scope

ESREF 2000, the 11th European Symposium on Reliability of Electron Devices and Failure Analysis will take place at Dresden, Germany from October 2 - 6, 2000.

This event will provide the European forum for the presentation of recent developments and future trends in quality and reliability assessment of micro-electronic material, devices and modules in their extending areas of application. All aspects of specification, technology, design and manufacturing advances, testing, control and analysis will be addressed.

The symposium has included the scope of the previous **EOBT** Conference, Electron and Optical Beam Testing.

Programme Overview

Technical Sessions

The accepted papers from Europe, United States, Asia contribute to the following sessions:

1 Design for Reliability

2 Failure Mechanisms in Metallizations and Dielectrics

3 Fault Localization

4 Packaging, Assemblies and Reliability

5 Silicon Devices

6 Product Realization

7 Power Devices and High Temperature Electronics

8 Compound Semiconductors

9 Physical Failure Analysis

10 Poster Session

Workshops

Workshops complete the technical sessions and provide the opportunity for exchange of know-how on subjects in progress.

Tutorials

Tutorials by experts provide both up-dates on selected topics of actual interest and opportunity for education and training.

User group meetings in conjunction with ESREF

provide detailed exchange on specific topics.

Equipment demonstration

Equipment demonstration is provided as a valuable accompanying event which provides experience with advanced techniques and recent developments for testing and analysis.

Key notes

Reliability of Flip Chip and Chip Size Packages

H. Reichl, A. Schubert, Fraunhofer Institute for Reliability and Microintegration, IZM, Berlin, Germany

300 mm – the Gateway to Next Generation Semiconductor Manufacturing

P. Kücher, Semiconductor 300, Dresden, Germany

Invited Papers

Invited speakers, who are recognized experts in their fields, will review the state of art and focus on leading work:

Packaging of CMOS MEMs

H. Baltes, O. Brand, ETH Zurich, Switzerland

Design for Reliability

A. Mathewson et al, Nat. Microel. Res. Center, Ireland

Backside Failure Analysis of CMOS Circuits Using Picosecond Imaging Circuit Analysis

J. Kash, M. McManus, IBM Yorktown Heights, USA

MOS Transistor Reliability under Analog Operation

R. Thewes et al., Infineon Technologies, Munich, Germany

Thermomechatronics of Power Electronic Packages

M. C. Shaw et al., Rockwell Science Center Thousand Oaks, USA

Reliable Use of Commercial Technology in High Temperature Environments

P. McCluskey, Calce Institute, University Maryland, USA

Reliability of Optoelectronic Components for WDM Transmission

D. Sauvage, D. Lafitte, Alcatel Optronics, Nozay, France

Overstress and Electrostatic Discharge in CMOS and BCD Integrated Circuits

G. Meneghesso et al., University of Padua, Italy

Best paper of Int. Reliability Physics Symposium (IRPS) 2000, USA: Experimental Evidence for Voltage Driven Breakdown Models in Ultrathin Gate Oxides

P.E. Nicollian et al., Texas Instruments, Dallas, USA

Best Paper of RCJ Reliability Symposium 1999, Japan: Acceleration Method for Gate-Disturb Degradation on Embedded Flash EEPROM

T. Wada, Semiconductor Corp. Matsushita Electronics, Japan

User Group Meetings in conjunction with ESREF

EFUG 2000, 4th European Focused Ion Beam User Group Meeting

Monday, Oct. 2 , 9:00 – 17 h, Room 1

Organiser: H. Bender, IMEC, Belgium

This one day meeting is intended to stimulate discussion and to exchange ideas and practical knowledge. It will start with a review lecture on the basic principles and applications of Focused Ion Beam. Subsequent sessions will address the various aspects of FIB applications :

- Device modification and gas assisted FIB
- TEM sample preparation
- FIB for failure and materials analysis
- Non-semiconductor applications of FIB

The sessions are composed of short presentations by FIB users and discuss novel applications, new materials (Cu, low-k), new procedures, case studies, new instrumentation, also unresolved problems.

Mini-posters of the participants showing results or problems encountered in FIB-life serve as starting point for the informal discussion and interaction between the participants. A prize for the "best" picture will be awarded!

Registration

For registration (no fee), contact the workshop organiser by email or fax at

Hugo Bender
IMEC
Kapeldreef 75
B-3001 Leuven
Belgium

phone: +32-16281-304
fax: +32-16281-844
email: hugo.bender@imec.be
EFUG web page: http://www.imec.be/6/efug/

ESREF / SUCCESS User Forum

Monday, October 2, 9:00 - 17 h, Room 2

Forum on Product (COTS) Performance and Reliability Engineering, Parts Assessment Processes Regarding Specific Operational Conditions

Organizer: M. Barre, Matra BAe Dynamics, France

As continuation to previous SUCCESS workshops (in combination with ESREF '97, '98) this one-day event shall serve as a User Forum to present and debate the industrial practices related to Commercial

Components Performance and Reliability Management for applications working under severe / specific operational conditions.

It covers the technical and management issues related to:

- Performance & requirement specification
- Data & expertise sharing processes with manufacturer
- Dedicated engineering regarding Performance Assessment
- Reliability Assessment based on Physics of Failure
- Redesign of system level reliability prediction processes
- Characterisation techniques dedicated to packaging & assembly level reliability

The details of the programme are available on ESREF home page: http://www.vde.com/esref2000

Registration

For registration to this forum please use the ESREF registration form

The registration fee for this forum (DM 200.-) covers lunch and documentation with CD-ROM to be mailed after the event.

Contact address:
M. Barré
Matra BAe Dynamics, France

phone: +33.1.34.88.19.61
fax: +33.1.34.88.19.88
email: mbarre@matra-def.fr

Tutorials

Tutorial 1 **Monday Oct. 2, 14:00 – 16:00 h, Room 3**

Planning and Performing Accelerated Testing of Microelectronic Devices, Traditional and New Methods.

L. Rimestad, Dept. Appl. Electronics, Danish Techn. University, Lingby

This tutorial aims at giving an overview of some of the most viable methods for accelerated testing of microelectronic devices.

The design of the test and the allocation of test specimens is important for the succes of the experiment. Damage accumulation, wear-out test methods and extrapolation to give a life estimate will be demonstrated together with the relationsship plotting techniques designed for this.

Also, the alternative robustness testing and random overload methods will be shown. Furthermore, a few examples of analysis of failure patterns, also for censored data will be given.

Tutorial 2 **Monday Oct. 2, 16:30 – 18:30 h, Room 3**

Qualification for Reliability in Time-to-Market Driven Product Creation Processes. An intercompany project *)

F. Wulfert, Motorola, Germany,
H. Tiemeyer, Infineon Technologies, Germany

The penetration of semiconductor products into the variety of application segments together with their economic forces of cost

and time-to-market enforce more efficient qualification concepts. This influences the organisation of the qualifcation process in relation to the development / innovation process as well as the choice of qualification concepts.

The practices of qualifying products for reliability are changing from traditional stress testing with qualitative relationships to use conditions to procedures which are more strictly related to the physics of failure at an improved quantitative level. This also provides the basis for adaption to specifc application segments.

Based on the project work by experts of a group of semiconductor companies, the tutorial will give the principles of the different concepts, discuss the transition and introduce into a systematic procedure for identication of those aspects, which need to be qualified,by making best use of existing knowledge (available results). As a result, qualification is integrated into the development process for improvement of time to market.

**) J. Bisschop [1], H. Brunner [2], W. Gerling [2], G. Kolmeder [3], B. Lange [4], H. K. Min [5], A. Preussger [2], F. Speroni [6], H. Tiemeyer [2], J. O. Weidner [7], F. Wulfert [8]*

[1]Philips, Nijmegen; [2]Infineon Technologies, Munich; [3]Hitachi, Landshut; [4]Texas Instruments, Freising; [5]National Semiconductors, Santa Clara; [6] ST Microelectronics, Milano; [7] AMD, Dresden; [8]Motorola, Munich

Tutorial 3 **Tuesday Oct. 3, 8:00 – 10:00 h, Room 2**

Non-Volatile Memory Reliability

J. Van Houdt, IMEC, Belgium

Nonvolatile memories based on the floating gate storage principle have recently emerged into a large volume market tracing DRAM in terms of density (currently 256-512Mbit) and cost per Megabyte. This is entirely due to the booming Flash memory market which is triggered not only by the unique properties of Flash, but also by entirely new applications for stand-alone as well as for embedded memories.

In the case of state-of-the-art stand-alone memories, the huge (Gigabit-level) density requires outstanding reliability features. But also in the embedded case, robustness is of utmost importance since complicated ECC and verify schemes are undesirable due to their larger relative overhead in terms of silicon estate as compared to stand-alonememories.

This tutorial will, therefore, focus on the major reliability issues of Floating Gate memory, addressing however also a number of typical Flash-related problems. After reviewing the physics of the major program and erase mechanisms, the respective reliability issues and the associated physics will be discussed as well as generic solutions. This includes write/erase endurance, the over-erase issue, high and low temperature charge retention behaviour, disturb phenomena during programming, erasing and read-out, soft-write effects and Stress-Induced Leakage Currents.

Tutorial 4 **Tuesday Oct. 3, 8:00 – 10:00 h, Room 3**

The Work of the GOOD-DIE II Network of Excellence in Europe on the Infrastructure for Semiconductor Technologies

J. Roggen, IMEC, Belgium, M. Roughton, MGR Consultants and D. Radley, Fretwell-Downing Facilities, Great Britain

The GOOD-DIE Network of Excellence was formed in November with the objective of collecting and disseminating information on various aspects of bare die, flip chip and CSP technologies through the means of newsletters, seminars, conferences and a web site. The partners involved in generating this information are Philips (CH), IMEC (B), Eltek (UK), Rood (UK), Fretwell-Downing (UK), Alcatel (B), Infineon (D) and MCC (USA).

This tutorial will cover the general areas of technology that the group are studying which covers road-mapping, test strategies, handling and delivery methods, training requirements, CAD/CAM interfaces and the role of microsystems using bare die.

Also a more detailed presentation will be given on the generation of a standard for procuring bare die, flip chip and CSP covering such topics as mechanical, quality, handling, thermal and electrical simulation for the procurements of such components, particular requirements for types of die such as bare die, TAB, flip chip, CSP etc. and the generation of a data exchange format and dictionary.

Tutorial 5 **Tuesday Oct. 3, 10:30 – 12:30 h, Room 2**

Using the Internet to obtain Quality and Reliability Information

R. Thomas, Technology Expert Network, USA
H. Livingston, Independent Researcher, USA

The tutorial will briefly cover the basic operation of the internet, how to access and optimize the use of browsers to view, download and store information.

The major portion of the tutorial will be directed towards accessing quality and reliability information that is available on the internet. This will begin with the use of search engines to locate information, live and recorded demonstrations of all the known internet sources that might be of interest to ESREF attendees. These would include professional sites like IEEE Opera, Computer Industry Quality Council, NASA, ESA, JPL, University sites, commercial quality and reliability data bases, and conference sites.

Other topics, such as people finders, and effective use of email for correspondence will be covered if time permits.

A complete set of notes and screen camera recordings will be available in pdf format on a CD to be handed out to all attendees at the symposium.

Tutorial 6 **Tuesday Oct. 3, 10:30 – 12:30 h, Room 3**

Application of Electron Beam Probing for Design Verifcation and Failure Analysis

S. Goerlich, Infineon Technologies, Germany

Electron beam probing has become an indispensable tool for IC-internal debugging of microelectronic devices for both design verification and failure analysis. This tutorial will start with the physical basics of voltage contrast and quantitative voltage measurement, discuss the problems of charging and radiation damage, and describe the useful areas of capacitive coupling voltage contrast. Technical principle of the modern e-beam probers will be outlined.

In the section about practical application the necessary integration with CAD and CAT will be stressed: design for analyses, CAD-navigation, and hardware integration with verification tester. Practical aspects for the typical debugging flow are choice of packaging, realization of test loops and preparation of probing pads with focused ion beam. Examples for both design verification and failure analysis at different kind of integrated circuits will be given, e.g. DRAMs, micro-controllers and consumer electronics.

ESREF Technical Sessions Programme

Tuesday, October 3, Room 2 + 3

14:00 **ESREF Conference Opening**

Conference Chairman *W. H. Gerling, Infineon Technologies, Munich, Germany*

Programme Chairmen *L. J. Balk, Bergische Universität Wuppertal, Germany*
E. Wolfgang, Siemens AG, Munich, Germany

14:20 Reliability of Flip Chip and Chip Size Packages

Keynote *H. Reichl, A. Schubert, Fraunhofer Institute for Reliability and Microintegration IZM, Berlin, Germany*

15:00 Packaging of CMOS MEMs

Invited Paper *H. Baltes, O. Brand, ETH Zürich, Switzerland*

15:40 Coffee Break

Session 1: Design for Reliability **Room 2 + 3**

Chairmen: *M. Barre, Matra BAe Dynamics, Velizy-Villacoubloy France*
J. Moeltoft, Technical University of Denmark, Lyngby, Denmark

16:00 1.1 Relation between improved ESD ruggedness and overall reliability of deflection amplifiers
R. van Roijen, A. W. Ludikhuize, J. Voets, P. van Oosten, Philips Research Laboratories, Eindhoven, The Netherlands

16:20 1.2 Modelling of Surface Potential Induced Leakage Failures in High Voltage Integrated Circuits and Application to Design Rule Derivation
Van der Pol., J., Rongen, R. T. H., Bruggers, H. J. Philips Semiconductors, Nijmegen, The Netherlands

16:40 1.3 Establishment of Derating Rules and Worst Case Analysis Figures for EEE Components
L. Cosqueric, P. Le Blanc, G. Salvaterra, L. Toudret, Matra Marconi Space France

17:00 1.4 Qualification Versus Application, New Approach for Electronic Control Unit (ECU) Qualification in Aeronautic Area
M. Dus, J.-L. Debauche, Serma Techologies, France

17:20 **Best Paper IRPS** Experimental Evidence for Voltage Driven Breakdown Models in Ultrathin Gate Oxides
P.E. Nicollian, W. R. Hunter, and J. C. Hu, Texas Instruments, Dallas, USA

17:50 **Best Paper RCJ** Acceleration Method for Gate-Disturb Degradation on Embedded Flash EEPROM
T. Wada Semiconductor Corp. Matsushita Electronics, Japan

18:30 – 20:00 Cocktail at Demonstration Area

Wednesday, October 4, Room 2

Session 2: Failure Mechanisms in Metallizations and Dielectrics

Chairmen: *A. J. Mouthaan, University of Twente, The Netherlands*
A. Preußger, Infineon Technologies, Germany

8:30 **Invited Paper** Design for Reliability
A. Mathewson e.a. Nat. Microel. Res. Center, Cork, Ireland

9:10 2.1 Grain boundary diffusion in PVD Copper Interconnects
T. G. Koetter, H. Wendrock, C. Wenzel, H. Schuehrer, K. Wetzig, Institute for Solid State and Materials Research Dresden, Germany

9:30 2.2 Room temperature grain growth in electroplated copper thin films
H. Wendrock, W. Brueckner, M. Hecker, T. G. Koetter, H. Schloerb, IFW Dresden, Germany

9:50 2.3 Assessment of Copper Contamination on Inter-Level Dielectric Reliability Performed with Time-Dependent-Dielectric-Breakdown Tests
R. Gonella, P. Mott, J. Torres, STMicroelectronics, France

10:10 2.4 Electromigration Characterization of Damascene Copper Interconnects Using Normally and Highly Accelerated Tests
T. Berger, L. Arnaud, R. Gonella, STMicroelectronics, France

10:30 Coffee Break

11:00 2.5 Thermal Resistance Evaluation of Al-Cu Electromigration Test Structures
A. Braghieri, I. De Munari, M. Impronta, A. Scorzoni, Centro Interdipartimentale di Ricerca "Materiali e Tecnologie dell'Informazione" Università di Parma, Italy

11:20 2.6 Low frequency noise evolution during lifetime tests of lines and vias subjected to electromigration
V. Dattilo, B. Neri, C. Ciofi, Dipartimento di Ingegneria dell'Informazione, Università degli studi di Pisa, Italy

11:40 2.7 Impact of Process Steps on Electrical and Electromigration Performances of Copper Interconnects in Damascene Architecture
R. Gonella, J. Torres, P. Motte, J.-M. Gilet, E. van der Vegt, STMicroelectronics, France

12:00 2.8 Influence of Fluorine Contamination on Intrinsic Reliability of Thin Gate Oxides
D. Krüger, P. Gaworzewski, R. Kurps, K. Pomplun, IHP, Frankfurt, Germany

12:20 2.9 Annealing Behavior of Gate Oxide Leakage Current after Quasi-breakdown
Zhen Xu, Byung Jin Cho, Ming Fu Li, Department of Electrical and Computer Engineering, NUS, Singapore

12:40 2.10 Low-field latent plasma damage depassivation in thin-oxide MOS
G. Cellere, L. Pantisano, A. Paccagnella, P. Colombo, M. G. Valentini, Dipartimento di Elettronica e Informatica, Università di Padua, Italy

13:00 Lunch Break

Session 3: Fault Localisation **Room 3**

Chairmen: *W. Claeys, University Bordeaux I, France*
R. Cramer, ALTIS Semiconductor, Paris, France

8:30 **Invited Paper** Backside Failure Analysis of CMOS circuits using Picosecond Imaging Circuit Analysis (PICA)
J. Kash, M. McManus, IBM Yorktown Heights, USA

9:10 3.1 Study of triggering inhomogenities in gg-nMOS ESD protection devices via thermal mapping using backside laser interferometry
M. Litzenberger, K. Esmark, D. Pogany, C. Fürböck, H. Gossner, E. Gornik, W. Fichtner, Institute for Solid State Electronics, University of Technology, Vienna, Austria

9:30 3.2 Thermal and free carrier concentration mapping during ESD event in Smart Power ESD protection devices using a modified laser interferometry technique
C. Fürböck, K. Esmark, M. Litzenberger, D. Pogany, G. Groos, R. Zelsacher, M. Stecher, E. Gornik, Institute for Solid State Electronics, University of Technology, Vienna, Austria

9:50 3.3 Laser Cross Section Measurement for the Evaluation of Single-Event Effects in Integrated Circuits
V. Pouget, P. Foullat, D. Lewis, H. Lapuyade, F. Darracq, IXL, Université Bordeaux I, France

10:10 3.4 Automatic EB Fault-Tracing System Using Fuzzy-Logic Approach
Katsuyoshi Miura, Koji Nakamae and Hiromu Fujioka, Department of Infomation Systems Engineering, Osaka University, Japan

10:30 Coffee Break

11:00 3.5 Correlation of Scanning Thermal Microscopy and Near-field Cathodoluminescence Analyses on a Blue GaN Light Emitting Device
R. Heiderhoff, M. Palaniappan, J. C. H. Phang, L. J. Balk, University Wuppertal, Germany

11:20 3.6 Voltage-influence of biased interconnection line on integrated circuit-internal current contrast measurements via magnetic force microscopy
R. Weber, M. Mertin, E. Kubalek, Gerhard-Mercator-Universität, Werkstoffe der Elektrotechnik, Duisburg, Germany

11:40 3.7 Quantification of Scanning Capacitance Microscopy Measurements for 2D Dopant Profiling
P. Malberti, L. Ciampolini, M. Ciappa, W. Fichtner, Swiss Federal Institute of Technology (ETH) Zurich, Switzerland

12:00 3.8 Cross-talk in electric force microscopy testing of parallel sub-micrometer conducting lines
U. Behnke, W. Mertin, E. Kubalek, Werkstoffe der Elektrotechnik, Gerhard-Mercator-Universität Duisburg, Germany

12:20 3.9 In-Situ SEM Observation of Electromigration in Thin Metal Films at Accelerated Stress Conditions
J. d'Haen, J. Van Ollmen, Z. Beelen, J. V. Manca, T. Martens, W. De Ceuninck, M. d'Olieslaeger, L. De Schepper, M. Cannaerts, K. Maex, Institute for Materials Research (IMO), Limburg University, The Netherlands

12:40 3.10 Analysis of High Power Devices Using Proton Beam Induced Currents
M. Zmeck, T. Osipowicz, F. Watt, F. Niedernostheide, H.-J. Schulze, G. Fiege, L. J. Balk, Lehrstuhl für Elektronik, Bergische Universität Wuppertal, Germany

13:00 Lunch Break

14:30 Poster Session **Room 4**

Chairman: *E. Langer, AMD, Dresden, Germany*

P1 Faster Fault Isolation Using a Dichotomy Reduction of Node Candidates
R. Desplats, G. Rolland, P. Perdu CNES- French Space Agency, Toulouse, France

P2 New Non-Destructive Layer Ablation Based Backside Sample Preparation Method
F. Beaudoin, D. Lewis, F. Salin, F. Saviot, P. Peru IXL, Université Bordeaux I, Talence, France

P3 A Review of Sample Backside Preparation Techniques for VLSI
P. Perdu, R. Desplats, F. Beaudoin CNES, Toulouse, France

P4 A Multifunctional Laser Linking and Cutting Structure
Ole Mende, Dirk Niggemeyer Laboratorium für Informationstechnologie Universität Hannover, Germany

P5 Reliability and stability of GaAs-based pseudomorphic quantum wells for high-precision power metering
Y. Haddab, V. Mosser, F. Kobbi, R. Pond Montrouge Technology Center, Schlumberger Industries, France

P6 A Method For HBT Process Control and Defect Detection using Pulsed Electrical Stress
C. Sydlo, B. Mottet, M. Schüßler, M. Brandt, H. L. Hartnagel Inst. für Hochfrequenztechnik, TU-Darmstadt, Germany

P7 Electrochemical Wet Etching in KOH: H_2O Solution and Secondary/Ion Image Passive Voltage Contrast as a Complementary Technique in Failure Analysis
Oh Chong Khiam, Bi Jian Hua, Shailesh Redkar Chartered Semiconductor Manufacturing Ltd, Failure Analysis Laboratory, Singapore

P8 Effects of Test Sequences on Degradation Analysis in High Speed Connectors
M. Catelani, M. Mugnaini, R. Singuaroli, A. Falciani Department of Electronic and Telecommunications Università di Firenze, Italy

P9 A Methodology to Determine and Prioritize a Set of Key Parameters for Statistical Process Control in Semiconductor Manufacturing
M. Mercado Infineon Technologies, Germany

P10 Bulk and Surface Degradation Mode in 0.35µm Technology gg-nMOS ESD Protection Devices
D. Pogany, K. Esmark, M. Litzenberger, C. Fürböck, H. Gossner, E. Gornik Institute for Solid State Electronics, University of Technology, Vienna, Austria

P11 Numerical investigation for a grounded gate NMOS transistor under electrostatic discharge ESD through TLP method
P. Galy, V. Berland, B. Foucher, I. Lombaert-Valot, A. Guilhaume, J.-P. Chante, St. Dufrene, S. Bardy Pole Universitaire Léonard de Vinci, Paris, France, Aerospatiale CCR, Suresnes Cedex, France, CEGELY INSA Lyon, France, Philips Semiconducteurs Composants, Caen, France

P12 Dimensional Effects on the Reliability of Polycrystalline Silicon Thin-Film Transistors
H.-W. Zan, Po-S. Shih, C.-Y. Chang, T.-C. Chang Institute of Electronics, National Chao Tung University, Taiwan

P13 About Long-Term Effects of Hot-Carrier Stress on n-MOSFETS
Barbara Stadlober Infineon Technologies Villach AG, Villach, Austria

P14 Reliability of Passivated Polycrystalline Silicon Thin Film Transistors
D. Z. Peng, P. S. Shih, T. C. Chang, C. Y. Chang Institute of Electronics, National Chiao Tung University, Taiwan, National Nano Device Laboratory, Taiwan

P15 The Role of the Spreading Resistance Profiling in Manufacturing Control and Technology Development
J. Lin-Kwang, St. Ramey, J. M. Reynes, B. Hillard, T. Thieme Motorola Semiconductor Products Sector, Toulouse Cedex, France, Solid State Measurement Inc, Pittsburgh, PA, USA, Solid State Measurements GmbH, Dresden, Germany

Session 4: Packaging, Assemblies and Reliability

Room 2 + 3

Chair Persons: *Y. Danto, IXL, University Bordeaux, France, K. Weide, Universität Hannover, Germany*

16:00 4.1 The Mode I Popcorn Effect, Moisture Sensitivity Level Estimation of P-DSO Packages
Alpern, P., Lee, Kheng Chooi, Infineon Technologies, Germany/Singapore

16:20 4.2 Measurement of the Thermomechanical Strain of Electronic Devices by Shearography
S. Dilhaire, S. Jorez, L.D. Patini-Lopez, W. Claeys, Laboratoire de Caractérisation de Composants Electroniques, CPMOH and IXL Université de Bordeaux I - France

16:40 4.3 Surface Oxide Films on Aluminium Bondpads: Influence on Thermosonic Wire Bonding Behavior and Hardness
Petzold, M., Berthold, L., Katzer, D., Knoll, H., Memhard, D., Meier, P., Lang, K.-D., FhG Halle, Germany

17:00 4.4 Reliability Model for Al Wire Bonds subjected to Heel Crack Failures
N. Seliger, S. Ramminger, G. Wachutka, Siemens AG, Corporate Technology, Munich, Germany

17:20 4.5 Thermal Fatigue and Metallurgical Reactions in Solder Joints of LTCC Modules
R. Rautioaho, O. Nousiainen, T. Saven, S. Leppävuori, J. Lenkkeri, Laboratory of Materials Engineering and EMPART Research Group of Infotech, University of Oulu, Finland

17:40 4.6 Vertical Die Crack Stresses of Flip Chip induced in Major Package Assembly Processes
D. G. Yang, L. J. Ernst, C. van't Hof, M. S. Kiasat, Delft University of Technology, The Netherlands

18:00 4.7 Flip Chips and Acoustic Micro Imaging: An Overview of Past Applications, Present Status, and Roadmap for the Future
J. E. Semmens, Sonoscan, Inc., USA

Session 5: Silicon Devices

Chairmen: *P. Seegebrecht, Christian-Albrechts-University, Kiel, Germany*, *J. van der Pol, Philips Semiconductors, The Netherlands*

8:30 **Invited Paper** MOS Transistor Reliability under Analog Operation
R. Thewes e.a., Infineon Technologies, Munich, Germany

9:10 5.1 The Impacts of SILC and Hot Carrier Induced Drain Leakage Current on the Refresh Time in DRAM
S. H. Hong, J. Y. Chun, C. G. Yu, J. T. Park, University of Inchon, China

9:30 5.2 Data retention prediction for modern floating gate non-volatile memories
G. Tao, A. Scarpa, J. Dijkstra, W. Stidi, F. Kuper, Philips Semiconductors, Nijmegen, The Netherlands

9:50 5.3 Transconductance Increase due to Charge Trapping During Hot-Carrier Stress of nMOSFETs
J. M. Rafi, F. Campabadal, Institut de Microelectrònica de Barcelona, IMB, Spain

10:10 5.4 Stability of Polysilicon Thin Film Transistors under Switch Operating
J.F. Llibre, H. Toutah, B. Tala-Ighil, T. Mohammed-Brahim, K. Mourgues, Y. Helen, F. Raoult, O. Bonnaud, Cite Universitaire, LUSAC, Octeville, France

10:30 5.5 Evaluation of the Ionising-Radiation/Hot-Carrier Induced Effects on the RF Characteristics of Low-Complexity SiGe Heterojunction Bipolar Transistors through Numerical Simulation
J. Kuchenbecker, M. Borgarino, A. Coustou, R. Plana, J. Graffeuil, F. Fantini, LAAS-CNRS, 7 Toulouse, France

10:50 5.6 RTS Noise in Submicron SiGe Epitaxial Base Bipolar Transistors
L. Militaru, A. Souifi, M. Mouis, G. Brémond, Laboratoire de Physique de la Matière, Lyon, France

11:10 Coffee Break

11:40 5.7 A Complementary Molecular-Model, Including Field and Current, for TDDB in SiO_2 Dielectrics
J. W. McPherson, R. B. Khamankar and A. Shanware, Texas Instruments, Inc. Dallas, Texas

12:00 5.8 Modeling the Conduction Characteristics of Broken Down Gate Oxides
Enrique Miranda, Jordi Suné, Universidad de Buenos Aires, Argentina

12:20 5.9 Shot Noise Partial Suppression in the SILC Regime
F. Crupi, G. Iannaccone, B. Neri, S. Lombardo, Università degli Studi di Pisa, Italy

12:40 5.10 Does Short Wavelength Lithography Process Degrade the Integrity of Thin Gate Oxide?
Kim, S. J., Cho, B. J., Chon, P. F., Chor, E. F., Ang, C. H. Ling, C.H., Joo, M. S., Yeo, I.S., National University of Singapore

13:00 Lunch Break

Session 6: Product Realization **Room 2 + 3**

Chair Persons: *F. G. Kuper, Philips Semiconductors, Nijmegen, The Netherlands*
D. Schmitt-Landsiedel, Techn. University Munich, Germany

14:30 **Keynote** 300 mm - the Gateway to Next Generation Semiconductor Manufacturing
P. Kücher, Semiconductor 300, Dresden, Germany

15:10 6.1 Technique for Determining a Prudent Voltage Stress to Improve Product Quality and Reliability
J. Courtney Black, Ben Hui, Don T. Prince, Richard C. Blish, II, Sunnyvale, USA

15:30 6.2 Impact of Drain Junction Soft ESD Damage on Product Lifetime
J. C. Reiner, T. Keller, H. Jäggi, S. Mira, Philips Semiconductors AG, Zürich, Switzerland

15:50 6.3 CALYPSO - Critical Area, Lifetime, and Yield Predicting Software
P. Miskowiec, D. Kunze, K. Lukat, IMS Dresden, Germany

16:10 6.4 Yield and Reliability Analysis of Digital Standard Cells with Resistive Defects
M. Huber, Th. Nirschl., J. Gstöttner, M. Heinitz, Th. Zanon, W. Maly, D. Schmitt-Landsiedel, Techn. University Munich, Germany

16:30 – 17:00 Coffee Break

Workshops **Thursday Oct. 4 , 17:00 – 18:30 h, Room 3**

WS 1: Power Devices Workshop:
High Temperature Silicon Power Electronics

Moderators: *M. Ciappa, ETH Zurich, Switzerland*
E. Wolfgang, Siemens, Germany

There is a major trend towards higher operating temperatures up to 200°C junction temperature and 125°C ambient temperature. This is driven mainly by automotive electronics where mechanical and hydraulic components will be replaced by electric motors and the corresponding power electronics. A few examples are: Electromagnetic valves, integrated starter generator, and brake by wire. In industrial applications we can expect a similar trend because of the integration of the electronics and the hot motor.

Leading experts from US and Europe will give short statements and will discuss topics like:

- chip and packaging reliability at higher temperatures

- passive components

- printed circuit boards and connectors

- integrated systems

It is very appreciated, if the attendees of the workshop will play an active role, e.g. by showing their results or by addressing specific problems.

Thursday Oct. 4 , 17:00 – 18:30 h, Room 2

WS 2: Electro Static Discharge (ESD) Workshop
– Requirements, Testing, Protection Development –

Moderator: *H. Gieser, Fraunhofer IZM-Munich, Germany*

ESD continues to be a major concern. Effective protection of advanced technologies from foundries, as well as high speed, mixed voltage, and high pin count devices in demanding development cycle times is an increasing challenge.

Experts from industry and academia will identify problems and discuss solutions.

Thursday Oct. 4 , 17:00 – 18:30 h, Room 4

WS 3: Microsystems Workshop

Moderator: *J. Villain, University of Applied Sciences Augsburg, Germany*

The aim of the workshop will be the presentation of specific reliability problems and open questions of microsystems today. After short presentations of exemplary microsystems, for example of a finger print sensor, a discussion will start together with the participants about the necessary qualification steps with regard to the design, the used materials and the manufacturing processes to achieve microsystems with high reliability.

19:30 – 22:00 Conference Dinner

Friday, October 6, Room 3

Session 7: Power Devices and High Temperature Electronics

Chairmen: *M. Ciappa, ETH-Zentrum Zurich, Switzerland, W. Wondrak, DaimlerChrysler, Frankfurt, Germany*

8:30 **Invited Paper** Thermomechatronics of Power Electronic Packages
M. C. Shaw e.a., Rockwell Science Center Thousand Oaks, USA

9:10 7.1 Back side Optical Beam Induced Current Method for the Localization of Electric Field Enhancements in Edge Termination Structures of Power Semiconductor Devices
G. Soelkner, J. Kreutle, J. Quincke, W. Kaindl, G. Wachutka, Siemens AG, Munich, Germany

9:30 7.2 Use of Electrical Stress and Isochronal Annealing for Power MOSFETs in order to Characterize the Effects of a 60Co Irradiation
C. Picard, C. Brisser, A. Hoffmann, F. Joffre, J.-P. Charles, L. Adams, A. Holmes Siedle, LETI - Gif-sur-Yvette, France

9:50 7.3 Modelling the Mechanical Behaviour of Large-Area Solder Joints
Poech, M. H., Eisele, R., FhG ISIT, Itzehoe, Germany

10:10 7.4 Reliability Testing of Multichip High Power IGBT Modules
G. Lefranc, T. Licht, G. Mitic, H.-J. Schultzu, R. Beinert, E. Wolfgang, Siemens AG, Munich, Germany

10:30 7.5 Failure Criteria for Long Term Accelerated Power Cycling Test on High Power Traction IGBT Module 1200A-3300V
G. Coquery, R. Lallemand, INRETS-LTN, Arcueil, France

10:50 Coffee Break

11:20 **Invited Paper** Reliable Use of Commercial Technology in High Temperature Environments
P. McCluskey, Calce Institute, University Maryland, USA

11:40 7.6 Reliability Aspects of High Temperature Power MOSFETs
J. V. Manca, W. Wondrak, W. Schaper, K. Croes, W. De Ceuninck, B. Dieval, H. L. Hartnagel, L. De Schepper, Limburgs Universitair Centrum, Institute for Materials Research, Belgium

12:00 7.7 Thermal Stability of Laser Welded Thermocouple Contacts to Si for High Temperature Thermal Sensor Application
Ernst, H., Müller, E., Kaysser, W.A., German Aerospace Center, DLR, Köln, Germany

12:20 7.8 Reliability of AlGaN/GaN HFETs comprising refractory ohmic and Schottky contacts
Würfl, J. , Hilsenbeck, J. Nebauer, E., Tränkle, E., Obwoh, H., Philips Semicondutors, The Netherlands

12:40 7.9 3-D analysis of the breakdown localized defects of ATM through a triac study
S. Forster, T. Lequeu, R. Jerisian, A. Hoffmann, CLOES, Metz, France

Session 8: Compound Semiconductors **Room 2**

Chair Persons: *N. Labat, University Bordeaux I, France*
E. Zanoni, University of Padua, Italy

8:30 **Invited Paper** Reliability of optoelectronic components for WDM transmission
D. Sauvage, D. Lafitten, Alcatel Optronics, Nozay, France

9:10 8.1 Reliability of InAlAs/InGaAs HEMTs grown on GaAs substrate with metamorphic buffer
M. Dammann, M. Cherouk, W. Jantz, K. Köhler, G. Weimann, Fraunhofer-Institut für Angewandte Festkörperphysik, Freiburg, Germany

9:30 8.2 Parasitic Effects and Long Term Stability of InP-based HEMTs
G. Meneghesso, R. Luise, D. Buttari, A. Chini, H. Yokoyama, T. Suemitsu, E. Zanoni, Univ. of Padua, Italy

9:50 8.3 A Method to Minimize Test Time for Accelerated Ageing of pHEMT's by Analysis of the Electronic Fingerprint of the Initial Stage of Degradation
R. Petersen, W. De Ceuninck, L. De Schepper, J.-L. Muraro, Institute for Materials Research (IMO), Limburgs Universitair Centrum, Belgium

10:10 8.4 Comparison of RF and DC life-test effects on GaAs power MESFETs
B. Lambert, N. Saysset-Malbert, N. Labat, F. Verdier, A. Touboul, P. Huguet, F. Garat, IXL ENSERB-Université Bordeaux 1, France

10:30 8.5 Model for the Decrease in HBT Collector Current under DC Stress based on Recombination Enhanced Defect Reactions
M. Schüßler, B. Mottet, C. Sydlo, H. L. Hartnagel, R. Jakoby, Techn. University Darmstadt, Germany

10:50 Coffee Break

Session 9: Physical Failure Analysis **Room 2**

Chair Persons: *M. Vanzi, University of Cagliari, Italy*
E. Zschech, AMD Saxony Manufacturing GmbH, Dresden, Germany

11:20 **Invited Paper** Overstress and Electrostatic Discharge in CMOS and BCD Integrated Circuits
G. Meneghesso e.a., University of Padua, Italy

12:00 9.1 Application of Analytical TEM for Failure Analysis of Semiconductor Device Structures
Engelmann, H. J., Saage, H., Zschech E., AMD Saxony Manufacturing, Dresden, Germany

12:20 9.2 New FIB/TEM Evidence for a REDR Mechanism in Sudden Failures of 980 nm SL SQW InGaAs/AlGaAs Pump Laser Diodes
M. Vanzi, G. Salmini, R. De Palo, University of Cagliari, Italy

12:40 9.3 Calculation of the Optimal FIB Milling and Deposition Operations for Easier and Faster Circuit Reconfiguration
R. Desplats, T. Dargnies, J.-C. Courrege, P. Perdu, CNES,Toulouse, France

13:00 9.4 X-Ray Structure Characterisation of Barriers for Copper Metallization
Mattern, N., Hecker, M., Fischer, D. Wenzel, C., Schell N., Matz, W., Engelmann, H. J., Zschech E., Institute for Solid State and Materials Research Dresden, Germany

13:20 Best Paper Award Presentation **Room 2 + 3**

13:40 **Conference Closing**

Equipment Demonstration

The following companies/organisations participate (as of June 15, 2000):

Allied High Tech Products Inc.
Material Characterization and Failure Analysis Equipment

Unaxis Nextral
RIE + HDP Systems for Failure Analysis

DESTIN N. V.
Electromigration/Hot Carrier/TDDB Testing

FEI / Philips Electron Optics
FIB work stations, Dual Beam (TM.) Systems, SEM, TEM

Hamamatsu Photonics Dt. GmbH
Emission Microscopy

HTT GmbH
DC-Parametric Analyzer, Acoustical Microscope, Analytical Prober

Karl Suss Dresden GmbH
Probe Systems / Accessories for Microelectronic Industry

Knights Electroglass
CAD navigation and yield management software

Microinstruments
Electromigration and TDDB Testing Software

Maser Engineering
Engineering Services for the Microelectronics Industry

Omicron Vakuumphysik GmbH
AFM, Scanning Nearfield Optical Microscopy

ORS Oneida Research Services
Gas Analysis, Service Laboratory

Oxford Instruments
Plasma Etch Equipment

Qualitau
Electromigration, dielectric breakdown, hot carrier degradation testing

Raith GmbH
CAD-navigation software, retrofit stager, complete SEMs

SERMA Testlab for Microelectronics
Test and Analysis of electronic components

Sonix Inc
Scanning Acoustic Microscopy

Sonoscan
C-Sam Acoustic Microscope, non-destructive inspection of micro-el. components

Synatron GmbH
Test- & QA-Systems

Triple O Microscopy GmbH
Scanning Probe Microscopy

Specialists Literature Display by Publishers:

Elsevier Science Ltd

John Wiley and Sons

Equipment Demonstrations

The equipment demonstrations take place in Room 1 and foyer of the Conference Centre of Hotel Westin Bellevue.

Opening hours:
Tuesday, Oct 3, 13:00 – 18:00 h
Wednesday, Oct 4 to Thursday Oct 5, 9:00 – 18:00 h

For information on the exhibition please contact:
Meet Ideas
Mrs. Iris Merkel
Rosengartenplatz 2
68161 Mannheim
Germany

phone: +49-621-4106 138
fax: +49-621-4106 207
email: i.merkel@mkt.de

General Information

Registration Fees

Fees for attendees, speakers, committee members in DM

Conference	registration before Sept. 1, 2000	late registration
VDE, EUREL, IEEE Members	900	1.000
Non-Members	1.000	1.100
University Members	750	850
Students*)	400	450
User Forum ESREF/SUCCESS	200	225
Tutorials, full package	450	500
Tutorials for one day only (Mo or Tue)	300	350
Additional proceedings	80	80
Additional dinner ticket	100	100
Opera ticket	55	55

*) A copy of student certification must be added to the regsitration form; student registration does not include proceedings and dinner ticket.

The full conference registration includes :
- admission to sessions and demonstrations
- proceedings and CD-ROM
- coffee breaks, lunch snacks
- one ticket for the Conference Dinner

To register, each registration form must be accompanied by the corresponding Credit Card information.
Cancellations by written notice must be received before Sept. 1, 2000 for reimbursement of paid registration fees reduced by DM 100.– for handling cost.

Conference Secretariat On-Site
On-Site registration is open according the schedule of activities on page 7.

phone: +49-351-805-1946
fax: +49-351-805-1946
e-mail: VDE_Tagungen@compuserve.com

Messages for participants may be routed to these telecom contacts.

Badges
A badge will be issued to each participant, which gives access to the conference sessions and demonstrations. It shall be worn for all events of the symposium.

Accommodation
A block of rooms has been reserved at the Conference Hotel Bellevue, effective **until Sept. 1,** 2000. As Dresden has a high visitors attraction, it is strongly recommended to register in time in order to take advantage of this.

Also reservations other than for the Conferene Hotel shall be made well in advance to ensure that rooms in the required category will be available. Please us the **Hotel Reservation Form.**

Theatre
The Wednesday evening (Oct. 4) gives the opportunity to visit the famous **Semper Opera.** A limited block of tickets has been reserved for attending :

Mozart and Themes of "As You Like it" (Ballet)
(preliminary programme).

Please book this event on the **registration form.**

Spouses Corner
A Spouses Corner will be prepared as meeting point in the Lobby of the Bellevue Hotel during the conference days, opening Tuesday 9.00 h.

Suggestions for tours (arrangements on site or by contacting the "Tourist Information").

- visit of historical Dresden with its famous buildings in Baroque and Rococco style
- visit of "Zwinger" Historical Museums with Old Masters Gallery, Porcelain Collection, "Albertinum" with New Masters Gallery, Treasure Chamber "Grünes Gewölbe" (Green Vault) an impression of the glory of the 17th and 18th centuries.
- visit of famous Porcelain Manufacture in Meissen
- excursion to Pillnitz Castle and "Saxonian Switzerland" by Paddle Wheeler on the Elbe river (day tour)
- excursion to Freiberg Cathedral and visit of a carving workshop at Seiffen / Erzgebirge (day tour)

Tourist Information
Dresden Werbung und Tourismus GmbH
Ostra-Allee 15
01067 Dresden
Germany

phone: +49-351-49192-0
fax: +49-351-49192-116
internet: http://www.dresden-congress.de

Shopping and bank opening hours

Shops	9:00 – 18:00 (Mon – Fri) 9:00 – 14:00 (Sat) closed (Sun)
Department Stores	9:00 – 20:00 (Mon – Fri) 9:00 – 14:00 (Sat) closed (Sun)
Banks	9:00 – 13:00 (Mon – Fri) closed (Sat, Sun)

Tax free shopping
In Germany the value-added tax (Mehrwertsteuer, MWSt) currently is 16%. Visitors from Non-Members of the European Union may receive a tax refund for purchase of more than 300.– DM upon leaving the country at the refund office at the airport or the border.

Travelling

Airport Dresden,
9 km from city centre.
Connections e.g. to Frankfurt (1 h), Hamburg (1.2 h), Munich (1 h) Amsterdam (2 h), Paris (2.5 h), Zurich (2.5 h), Vienna (2.5 h)
Shuttle service with Airport City Liner (every 20 min), public transportation, taxi.

Railway services
to all major German cities
e.g. Berlin (2 h), Frankfurt (5,5 h), Munich (7h)
and international connections, e.g. Prag/Tschechia (2.75 h)

Travelling by car
leave High Way A4 at exit “Dresden Altstadt” and follow sign “Zentrum”, some distances: Berlin (210 km), Frankfurt (470 km), Munich (490 km), Prag /Tschechia (150 km)

Electricity / phone patch
The mains power supply is 230 VAC, 50 Hz.
Texas or TAE6 (German) phone standard plugs are necessary to connect to the phone net.

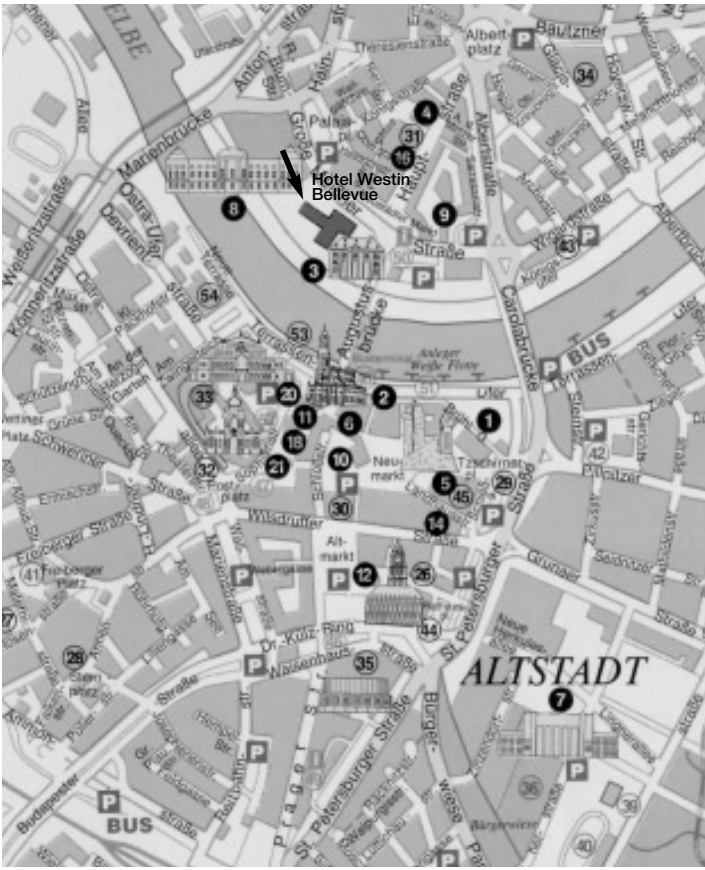
Liability / Insurance
The organiser cannot assume responsibility whatsoever for damage or injury to persons or property during the conference.
It is recommended to arrange for your own travel and health insurance.

Formalities / Visa
Some foreign Nationals may require entry Visa to Germany. Please check in time with the German Embassy or Consulate in your country and request for assistance. Please note that VDE or the organising bodies cannot issue any “Invitation”.

Emergency Services

Police call	110
Ambulance, Firebrigade call	112

City map Dresden



Sights/Museums

1 Albertinum (Brühlsche Terrasse)
- Picture Gallery of Contemporary Masters
- Green Vault
- Numismatic Collection
- Collection of Sculptures
- Special exhibition

2 Brühlsche Terrasse
- Museum für Mineralogy and Geology (entrance on the right hand side of the stairs)

3 Block house
4 Dreikönigskirche/House of the Church
5 Frauenkirche (building site)
6 Fürstenzug
7 German Hygiene Museum
8 Japanese Palace
- Museum for Ethnology
- Museum for Early Histroy

9 Jägerhof
- Museum for Folk Art

10 Johanneum with Stallhof
- Traffic Museum

11 Catholic Court Church
12 Kreuzkirche
13 Collection of Copper Engravings
14 Country House
- Town Museum

16 Museum for Dresdner Early Romaticism
18 Castle
- Exhibition in connection with the Dresdner Castle

20 Semper Opera

21 Zwinger
- Picture Gallery of Old Masters
- Armory (Historical Museum)
- Porcelain Collection
- Mathematical-Physical Museum
- Zoological Museum

Theaters and places of culture

26 French Cultural Center
27 theater 50
28 Herkuleskeule
29 Jazz Club "Tonne"
30 Kulturpalast
31 PODIUM
32 Theater (Schauspielhaus)
33 Semper Opera
34 Theater "Kleines Haus"
35 UFA-Palast
53 Dresdner Brettl (theatre on board)

Parks and sports places

36 Blüherpark
37 Grosser Garten
- Botanical Garden
- Open-air stage
- Park Railway
- Zoological Garden

39 Georg-Arnhold-Bad
40 Rudolf-Harbig-Stadion
41 Swimming Hall Freiberger Strasse
42 Swimming Hall Steinstrasse

Authorities

43 Landesregierung Sachsen
- (Government of the Land Saxony)

44 Stadtverwaltung Dresden
- (Municipal administration Dresden)

45 Polizeidirektion (Police Headquarters)
Polizeirevier Dresden-Mitte (Police station Dresden Center)
54 Saxon Parliament

Tourist Information

46 Bus stops for the town sight-seeing tour (Augustusbrücke, Dr.-Külz-Ring)
47 Stops for the town sightseeing tour "Hamburger Hummelbahn"
48 Tramway stops for the town sightseeing tour
49 Tourist information Prager Strasse
50 Tourist information Neustädter Markt
51 Landing stage for the ships
52 Central advance booking box office Schinkelwache for Opera

The City Map is part of the complete city map, consequently the sequence of numbers is not consecutive.

The way to Dresden

Highways and roads

- Highways A 4 and A 13
- Roads B 6, B 97, B 170, B 172, B 173

Railways

- Daily services to all major German cities
- Connections to the ICE and EC/IC networks
- International connections to more than 10 major European cities
- Two main-line railway stations

Air traffic

- Airport in Dresden-Klotzsche, 9 km from the city centre
- 2 terminals, 1,200 parking spaces
- Airport shuttle services with Airpport-Cityliner between the airport and the city, as well as public transport