50th Electronic Components & Technology Conference

May 21 - 24, 2000 • Caesars Palace

Las Vegas, Nevada

Advance Program

- 8 Half-Day Short Courses - CEU Credit Approved
- 2 Full-Day Short Courses - CEU Credit Approved
- 38 Technical Program Sessions
- Technology Corner Exhibits
- Plenary Session and New Panel Discussion on Emerging Technologies
- 2 Educational Sessions

Sponsored by:

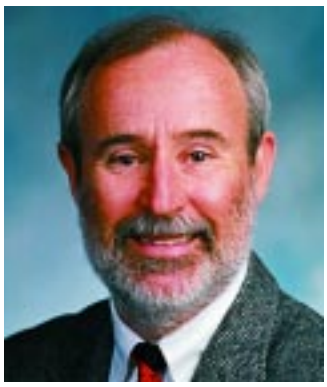
ECA Electronic Components, Assemblies & Materials Association

IPC 1950-2000

IEEE

For detailed information about the conference, visit the ECTC website www.ectc.net

Introduction from the 50th ECTC Program Chairman



The 50th Electronic Components and Technology Conference (ECTC) will be held May 21 - 24, 2000 at Caesars Palace, Las Vegas, Nevada, USA.

ECTC is jointly sponsored by the IEEE Components, Packaging and Manufacturing Technology Society and the Electronic Components, Assemblies, and Materials Association, the Electronic Components Sector. This international conference brings together the best in components and packaging science, technology and education in an evironment of close cooperation to exchange technical information on the state-of-the-art.

This year there are more than 300 technical presentations organized in 38 Technical Sessions covering a variety of topics from components, RF, connectors, contacts, interconnections, packaging and technology. There are sessions on wafer-level packaging and lead free interconnects. Also, there are six sessions devoted to optical and optoelectronic technologies.

The 50th ECTC will feature a Sunday evening Panel Session on New and Emerging Technologies organized by Dr. Ephraim Suhir and a Monday evening Plenary Session organized by Dr. Rao Tummala.

In addition, 12 Short Courses will be offered for the 50th ECTC. Dr. Al Puttlitz and his committee have brought together industry experts from a wide variety of disciplines to offer state-of-the-art courses such as wireless packaging, optoelectronics, polymers for microelectronics, environmental issues and others. These courses offer the opportunity to get the latest technology update in a condensed format and at the same time to obtain Continuing Education Units (CEUs).

Education for the 21st century will be addressed in two sessions which will highlight currect programs and recommended programs in electronic and packaging from universities worldwide.

Each ECTC attendee will receive a choice of the Proceedings in a CD-ROM or the printed book. Both can be purchased for a nominal fee.

Two Poster Sessions have been expanded with more posters and will offer a unique opportunity for authors and ECTC attendees to interact and discuss specific topics in a more relaxed and detailed manner. To emphasize the importance of this method of technical presentation, ECTC will be recognizing and giving an award for the Best Poster.

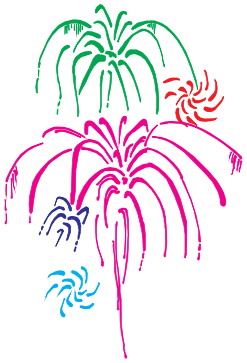
The ECTC would not be possible without the support of our sponsors, IEEE CPMT and EIA/ECA, as well as the many corporate participants in the Technology Corner and the Coffee Break and Reception Sponsors.

The Operating and Program Committees and the more than 100 engineers and scientists who contribute their time and energy to make this conference, hope you will find the 50th ECTC to be the premier international meeting for electronic components and packaging technologies.

Please join us to celebrate our 50th year.

Michael B. McShane
Motorola

A 50th Celebration



The year *2000* is special for all of us in a myriad of ways. As the new millennium arrives, we each take the time to reflect upon personal and professional accomplishments and highlights of the 20th century. We have a major milestone and accomplishment to celebrate, attained by no other electronics industry conference. In the year *2000*, the Electronic Components & Technology Conference is celebrating its 50th year. We are planning a celebration to recognize those who over the years have contributed to make ECTC what it is today! Come and join us as we reflect upon and recognize our history and just plain celebrate! The leadership and professional contribution of countless many have helped ECTC establish and sustain its reputation as the **Premier Packaging Electronics Conference** in the universe!

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ITHERM 2000
May 23 - 26, 2000 • Caesars Palace
Las Vegas, Nevada
Sponsored by: IMAPS, IEEE CPMT, ASME, NIST, K-16
Seventh Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems
Visit the ITHERM website www.itherm.org for information about the conference.

50th ECTC Registration

Advance Registration

To register in advance for the 50th ECTC, your application, and payment check must be received no later than May 5, 2000. Register early . . . . save $100. All applications received after May 5, 2000 will be considered Door Registrations. Those who register in advance may pick up their tickets and proceedings at the ECTC Registration Desk in the Prefunction I Area, 4th Floor Palace Tower at Caesars Palace. Additional Advance Programs are available from:

Jim Bruorton, Publicity Chairman
Phone: (864) 963-6621 Fax: (864) 963-6444
Email: margieballinger@kemet.com

Do not send advance registrations to the above address. See pages 26 and 27 for complete registration information.

3 Easy Ways to Register for ECTC 2000:

- Visit www.ectc.net.
- Fax completed form on page 27 to (703) 907-7549.
- Mail completed registration form on page 27 to EIA/ECA, P.O. Box 75023, Baltimore, MD 21275.

Registration Fees

Advance registration with proceedings (printed or CD), ECTC, CPMT and Program Chair Luncheons . . . *$500
Door registration with proceedings (printed or CD), ECTC, CPMT and Program Chair Luncheons *$600
One Day Registration $350
Speaker/Session Chair (Door Rate $425) $325
Speaker/One Day $200
Student $125
Special Sunday Half-Day Courses with Luncheon . . . #$300
Special Sunday All-Day Courses with Luncheon . . .#$500
Student Special Sunday All-Day Courses $25
Joint ECTC/ITHERM Advance $650
Joint ECTC/ITHERM Door $750
Proceedings Only, U.S. Postpaid $300
Foreign. $350

* IEEE Member - Advance/$425 - Door/$525
\# Door rate will be an additional $50

Note: There will be no refunds on cancellations after May 5, 2000. Substitutes can be made at any time.

At Door Registration Schedule

Registration will be held in the Prefunction I Area, 4th Floor Palace Tower:

Saturday, May 20, 2000 – 3:00 PM to 5:00 PM
Sunday, May 21, 2000 – 7:30 to 8:30 AM **(Short Courses Only)**
Sunday, May 21, 2000 – 1:00 PM to 5:00 PM
Monday, May 22, 2000 – 7:00 AM to 4:00 PM
Tuesday, May 23, 2000 – 7:30 AM to 4:00 PM
Wednesday, May 24, 2000 – 7:30 AM to 12:00 PM

Transportation

The 50th ECTC has two designated airline carriers this year. To take advantage of these special fares, see information below.

1. Call **United** (1-800-521-4041, 7:00 AM - Midnight EST daily). Refer to Meeting ID code 597BE.
2. Call **US Air** (1-877-874-7687) and refer to Gold File 94691375.
3. The special fares are available only through each airline's toll free number, so call today, or have your travel agent call for reservations. Certain restrictions may apply and seats are limited.

General Information

Conference organizers reserve the right to cancel or change the program without prior notice.

Loss Due to Theft

Conference management is not responsible for loss or theft of personal belongs. Security for each individual's belongings is the individual's responsibility.

Tax Deductions

Treasury regulation 1.162.5 currently permits an income tax deduction for educational expenses (fees and cost of travel, meals, and lodging) undertaken to (1) maintain or improve skills required in one's employment; or (2) meet express requirements of an employer. Check with your accountant or tax attorney.

Coffee Break Sponsors

Sponsorships are available for companies who would like to participate in the 2000 Electronic Components and Technology Conference by assisting in sponsoring the conference breaks. Your company's name will be included in the conference final program and will be displayed on a sign in the refreshments area. A table will be provided nearby to display limited promotional/informational material about the companies sponsoring breaks. To sign up to sponsor a coffee break, simply indicate your interest on the Conference Advance Registration form (page 27) and enclose the $350 sponsorship fee, payable to the 50th Electronic Components and Technology Conference. *Please note: Sponsorships must be prepaid, and must be received at least four weeks before the conference in order to be listed in the Final Program. For further information, call EIA (703) 907-7536.*

Register before May 5, 2000 to receive the $100 discount.

Technology Corner Exhibits

More and more companies are discovering that the quality of the prospects they identify while exhibiting their products or services in the ECTC Technology Corner is far superior to those in even larger conferences or trade shows. This is primarily due to the fact that the engineers and managers who attend ECTC hold decision making positions at the world's leading electronics industry's equipment and components manufacturers. They are attracted by ECTC's strong technical program. Authors in the field believe that ECTC offers the best forum for presenting their work. A record 300 papers, organized into 38 sessions, will be presented this year. Also this year (even numbered years only) the audience for exhibitors will include the attendees from the Seventh Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITHERM).

Following is a list of exhibitors as of February 5, 2000. Exhibit hours will be from 1:30 PM to 6:30 PM on Tuesday, May 23 and 9:00 AM to Noon and 1:30 PM to 6:00 PM on Wednesday, May 24. A few exhibit spaces are still available. To obtain information about exhibiting your products or services, call Bill Moody at (302) 478-4143, fax to (302) 478-7057, or email to b.o.moody@ieee.org. The exhibit application can be printed by going to the ECTC website at www.ectc.net.

Aavid Thermal Products
ACT Microdevices
Advanced Ceramics Corporation
Advanced Packaging Magazine
AI Technology, Inc.
ANSYS, Inc.
Applied Simulation Technology
Bergquist Company (The)
Cambridge AccuSense, Inc.
Chip Coolers, Inc.
Chip Scale Review
Chomerics
Dexter Electronic Materials
Dymatix
Electronic Materials, Inc.
Electronic Packaging & Production
Electronics Cooling
Emerson & Cuming
Enertron, Inc.
EPA Centre, University of Hong Kong
Epoxy Technology, Inc.
ESI
FCI Electronics
Ferro Electronic Materials
Flomerics Inc.
Fluent Inc.
Georgia Tech Packaging Research Center
Harvard Thermal, Inc.
High Density Interconnect
Holometrix Micromet
Institute of Microelectronics
Interconnect Systems, Inc.
Japan REC Co. Ltd.
Karl Suss America, Inc.
KEMET Electronics Corporation
Kyocera America, Inc.
Kyocera Industrial Ceramics Corporation
Loctite Corporation
Loyalty Founder Enterprise Co. Ltd., Heat Pipe Division
Mathis Instruments Ltd.
MAYA Heat Transfer Technologies, Ltd.
MH&W International Corporation
National Semiconductor
Nitto Denko America, Inc.
Occidental Chemical
Optimal Corporation
PAC TECH
Power Devices Inc.
Pure Technologies, Inc.
R-Theta Inc.
Relative Metrics, Inc.

Technology Corner Exhibits (cont)

SIGRITY, Inc.
Silicon Coast Associates, Ltd.
Sumitomo Electric USA, Inc.
Superior Micropowders
TechSearch International, Inc.
Teledyne Electronic Technologies
Teledyne Microelectronics
Tempo Electronics
Thermagon, Inc.
Thermoset, Lord Chemical Products
Toray Engineering Co., Ltd.
Vishay Intertechnology, Inc.
W. L. Gore & Associates, Inc.

ECTC 2000 Panel Discussion

New and Emerging Technologies (NET2000): What's New

Sunday, May 21, 2000 – 7:30 PM - 9:30 PM

Moderator: E. Suhir Bell Laboratories

1. Introduction: "A Disruptive Technology: Can One Recognize It?" – Ephraim Suhir, Bell Laboratories, Lucent Technologies, Inc.
2. "New and Emerging Technologies - Net 2000" – Ralph W. Wyndrum. Jr., Program Planning and Management, Vice President, AT&T Laboratories
3. "Infrastructure for e-business: Is More, soon, better?" – Rajeev Kohl, Columbia University
4. "Future Directions and Pathways in Electronics Manufacturing" – Dr. Michael A. Schen, NIST Advanced Technology Program
5. "Overcoming Environmental Challenges of the 21st Century" – Diana Bendz, Senior Location Executive and Director of Environmentally Conscious Products, IBM Corporation
6. "Trends and Challenges in Optoelectronic Packaging" – Rob Hannemann, Vice President Technology, Oak Industries, Inc.
7. "Molecular Assembly: A Potentially Disruptive Technology for VLSI Fabrication" – Bernard Yurke, Bell Laboratories, Lucent Technologies, Inc.
8. "The System is the Chip–How Technology and Design are Changing the Way Systems are Put Together" – Subramanian S. Iyer, IBM Semiconductor Research and Development Center
9. "Concept of 3D System Assembly" – Vladimir Gorelik, Vice President of Engineering, Integrated Data Systems
10. "Integrated Knowledge-Based Engineering for Design of Electronic Systems" – Behzad Mottahed, Bell Laboratories, Lucent Technologies, Inc.
11. "A Neural Network Paradigm for High-Frequency Component Modeling, Simulation and Optimization" – Q. J. Zhang, Carleton University
12. "Power-Density Challenges of Next Generation IP Networks" – Alex Vukovic, John Watkins, Mirjana Vukovic, Nortel Networks

ECTC Plenary Session

Monday, May 22, 2000 – 7:30 PM - 9:00 PM

Chairman: Professor Rao Tummala – Georgia Institute of Technology and Dr. Phil Garrou – Dow Chemical

1. "Microvia Technologies - An Asian Update" – Toshio Komiyatani – Sumitomo Bakelite, Japan
2. "The Latest and Hottest Topic in Systems Packaging: Contract Manufacturing, Status and Prospects" – Srinivas Rao, Vice President of Technology – Solectron
3. "SOC vs. SOP: Is a Paradigm Shift on the Horizon?" – Professor Rao Tummala, Chair Professor and Director, Packaging Research Center, Georgia Institute of Technology

Luncheons

ECTC Luncheon

The Electronic Components and Technology Conference will sponsor on Monday, May 22nd, for conference attendees and guests.

CPMT Luncheon

The Components, Packaging and Manufacturing Technology Society of IEEE will sponsor a luncheon for attendees and guests on Tuesday, May 23rd. The ECTC awards will be presented.

Program Chair Luncheon

On Wednesday, May 24th, the Program Chairman will sponsor a luncheon for attendees and guests.

50th ECTC Celebration Reception

Emperors Ballroom I & II (4th Floor)

All attendees and guests are invited to attend a reception hosted by AVX Corporation, KEMET Electronics Corporation, KOA Speer Electronics, Inc., Murata Electronics North America, ROHM Electronics USA, and Vishay on Tuesday, May 23rd at 6:30 PM.

Hotel Accommodations

Caesars Palace

The *New* Caesars Palace is the splendor of Rome available now with greater luxury and comfort. Now with 2,500 rooms and suites, three spacious casinos, four lounges, nineteen restaurants, health spa, fitness center, three swimming pools, Omnimax theatre, and the expanded Appian Way and Forum Shops.

Room reservations must be made directly with the hotel by April 20, 2000 to ensure special convention rates. *The ECTC special conference rate is $165 for single/double. (Check-in time is 3:00 PM Monday through Thursday and 5:00 PM Friday through Sunday and check-out time is Noon daily). A one night's deposit is due by each attendee at the time of making their reservation. Reservations will NOT be held after 30 days without a deposit. Reservations must be cancelled three (3) days or 72 hours prior to arrival to avoid forfeiture of deposit. Most major credit cards are accepted.* ***Call for booking assistance today at (702) 731-7222 or 800-634-6661 and mention ECTC for discounted rates or fax (702) 731-7172.***

Photographs provided by Caesars Palace and the Las Vegas Convention and Visitors Authority.

Chairman's Speakers Reception

Florentine I & II (3rd Floor)

Sunday, May 21, 2000
6:00 PM - 7:00 PM

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Conference Overview

May 21, 2000
Morning Short Courses
8:30 AM - 12:00 PM

1. Chip Scale Packaging
2. Analytical Acoustic Micro Imaging for Assessing IC Package Reliability
3. Eliminating Lead In Electronic Assemblies
4. Microelectronics Packaging & Interconnection – A Worldwide Perspective

May 21, 2000
Afternoon Short Courses
1:30 PM - 5:00 PM

5. Fiber-Optics Structures: Design for Reliability
6. Wafer Scale Packaging – Principles and Practices
7. RF/Wireless Packaging: Status and Challenges
8. Thermal Management, Thermal/Thermomechanical Modeling, Packaging, and Reliability of Plastic IC Packages

May 21, 2000
All-Day Short Courses
8:30 AM - 12:00 PM & 1:30 PM - 5:00 PM

9. Polymers for Electronic Packaging: Materials, Process and Reliability: Part I - The Fundamentals of Packaging and Materials Science and Engineering
10. Polymers for Electronic Packaging Materials, Process and Reliability - Part II
11. Business and Technical Perspectives for Optical Networking and Opto-electronics Components
12. Optoelectronics Components and Modules for Datacom and Telecom

Note: courses 9, 10, 11, or 12 can be taken as self-contained Half-Day Short Courses.

May 22, 2000
8:00 AM - 12:00 PM

S1 Automated Assembly of Optoelectronic Modules
S2 Flip Chip
S3 Wafer-Level Packaging Technologies
S4 Solder Technology
S5 Solder Materials and Joints Reliability
S6 Passive Components

May 22, 2000
1:30 PM - 5:30 PM

S7 Optical Alignment Techniques
S8 Systems Level Electrical and Thermal Modeling
S9 Underfill Materials
S10 Chip Scale Packaging
S11 Reliability Test Methods
S12 RF

May 23, 2000
8:00 AM - 12:00 PM

S13 High Speed Optoelectronic Packaging
S14 Electrical Modeling and Characterization
S15 High Density Chip and PWB Technologies
S16 Material Characterization and Modeling
S17 Flip Chip Reliability
S18 MEMS Packaging and Bonding Technology

May 23, 2000
1:30 PM - 5:30 PM

S19 Low-Cost Optoelectronic Packaging
S20 Power Distribution and EMI Modeling
S21 Low Cost Good Die (KGD/Burn-In)
S22 Plating and Under Bump Materials
S23 Adhesives
S24 MCM and Advanced Packaging Technology

May 24, 2000
8:00 AM - 12:00 PM

S25 Optoelectronic Packaging Materials and Reliability
S26 Electronic Packaging Education I
S27 Thermo-Mechanical Simulation and Modeling I
S28 Lead Free Interconnects: Solders and Conductive Adhesives
S29 Connectors and Contacts
S30 BGA Packaging

May 24, 2000
1:30 PM - 5:30 PM

S31 Parallel Optical Interconnects
S32 Electronic Packaging Education II
S33 Thermo-Mechanical Modeling and Simulation II
S34 CSP Reliability
S35 Lead-Free Soldering Technology
S36 Emerging Technologies

May 23, 2000
1:30 PM - 6:00 PM

S37 Poster Session

May 24, 2000
1:30 PM - 6:00 PM

S38 Poster Session

Session Summary by Interest Area

Packaging
S3, 10, 24, 30, 36

Interconnections
S2, 18, 21, 28, 29

Optoelectronics
S1, 7, 13, 19, 25, 31

Materials & Processing
S4, 9, 16, 22, 23

Components
S6, 12

Manufacturing Technology
S15, 35

Modeling & Simulation
S8, 14, 20, 27, 33

Quality & Reliability
S5, 11, 17, 34

Education
S26, 32

Short Courses

May 21, 2000

Albert F. Puttlitz, Cochairman
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Morning Courses
8:30 AM - 12:00 PM

1. Chip Scale Packaging
Course Leader: Patrick Thompson – Motorola, Inc.

Course Objective:

In only six years, chip scale packaging (CSP) has transitioned from a novelty, to a buzzword, to a legitimate choice among the array of commercially available packages. In 1999, two types of CSPs, wafer-level CSPs had stacked CSPs, began generating significant interest. This course will provide an overview of chip scale package technology and application, with an emphasis on new developments in CSP availability and infrastructure. This course will help provide the potential CSP manufacturer, buyer or user an understanding of the advantages of a CSP, as well as issues in their application.

Course Outline:

- Introduction to chip scale packaging
  - Definitions of chip scale packaging
  - Attributes of chip scale packages
- Description of chip scale packaging types
  - Array interposer
  - Peripheral interposer
  - Custom lead frame
  - Newly popular CSP implementations-wafer level and stacked CSPs
- Chip scale package performance
  - Electrical and thermal
  - Mechanical and materials
  - Reliability
- Infrastructure considerations
  - Package materials and manufacturing
  - Test
  - Board level assembly
  - Shipping and handling
  - Printed circuit boards and other system issues
- Chip scale packaging's role in the semiconductor packaging spectrum
  - CSP, KGD and MCM
  - Potential chip scale packaging applications and market

Who should attend:

This course should be beneficial to:

- Potential manufacturers of chip scale packages who want to understand how chip scale packages may help meet their packaging needs, and challenges in chip scale packaging production.
- Potential purchasers/users of chip scale packaging who want to know system and assembly issues of using chip scale packages.
- Those in the electronic field who want to obtain a basic knowledge of chip scale packaging concepts, issues and applications.

2. Analytical Acoustic Micro Imaging for Assessing IC Package Reliability
Course Leaders: Sridhar Canumalla and Lawrence W. Kessler – Sonoscan, Inc.

Course Objective:

Acoustic Micro Imaging (AMI) has found increasing use as a nondestructive inspection technique for microelectronic packages. This is due to its high sensitivity to variations in material properties and discontinuities such as delaminations, voids, cracks. There are several modes of inspection in AMI with different modes being suitable for particular kinds of defects. A solid understanding of the physics behind AMI techniques is essential for fully exploiting the acoustic microscope as a nondestructive tool. This course, in addition to introducing fundamental concepts of AMI, presents a practical treatment of the subject suitable for critical analysis of AMI data.

Course Outline:

- Introduction to AM
  - What is AMI? Benefits?
  - Sample Applications – Plastic ICs, PBGA, Flip Chip
- Fundamentals of Ultrasonics
  - Terminology
  - Nature of Ultrasonic waves
  - Types of waves
  - Generation and Detection of Ultrasonic Energy
  - Acoustic Properties of Materials
  - Reflection and Refraction at Interfaces
  - Resolution, Penetration and Frequency
  - The A-scan explained
  - Exercises to interpret A-scans
- A Comparative Review of Different Techniques
  - Interface scan
  - Multiple interface scan
  - Bulk scan
  - Loss of back wall echo
  - Through Transmission
- Practical Applications of Acoustic Microscopy
  - Plastic ICs
  - BGA
  - CSP
  - Flip Chip
  - Passive and active elements, substrates
  - Wafer bonding and MEMs
  - Hybrids
- Interpreting Acoustic Images and Optimizing Analysis Schemes

Who Should Attend:

This course is designed for engineers and technical managers involved in packaging, reliability, and process development in the microelectronic industry. Prior exposure to AMI is desirable to get the most out of this course, but not essential for understanding the fundamental concepts.

The goal is to apply the physics behind AMI to practical problems and facilitate optimal inspection for assessing component reliability.

3. Eliminating Lead in Electronic Assemblies
Course Leader: Karl J. Puttlitz – IBM Corporation

Course Objective:

The toxic effect of lead (Pb) is well known and widely reported to be related to certain health risks, thus a cause for grave concern that has led to a global movement including pending legislation to create a lead-free environment. The intent of this course is to familiarize participants with health-related and other global issues/perspectives, materials selection issues and potential candidates; understanding the design implications, and the implementation and manufacturing challenges associated with a conversion to a lead-free material set for electronic assemblies.

Course Outline:

- Health Related Issues
  - Lead sources, toxicity, regulations, findings
- Global Perspectives
  - History/status of Pb-free electronic assemblies
  - Legislation/activities in Europe, Asia, North America
  - Some OEM market-driven initiatives
- PB-Free Materials
  - Selection issues, advantages/disadvantages
  - Form: solder paste (SMT), wave solder (PIH), balls (PBGA)
  - Finishes: boards, components
- Manufacture
  - Assembly/inspection/test considerations
  - Equipment issues
  - Elevated temperature impacts: PWB, components, equipment, profiles
  - Need for protective atmospheres
  - Assembly issues
- Reliability Considerations
  - Components/flip chip
  - Metallurgical considerations, intermetallic formation
  - Mechanical property considerations
- Economic Considerations
  - Material
  - Energy
  - Equipment/implementation/modifications
  - Yield
- Some Pb-Free Products/ Experiences

Who Should Attend:

This course will be useful for all those faced with a need to gain an understanding of the issues involved in adopting and implementing a Pb-free technology in their products and/or manufacturing operations. The course will be particularly useful to design, development and process engineers; quality and purchasing personnel; technical managers and other professionals involved in the lead-free conversion, and also academia.

4. Microelectronics Packaging & Interconnection – A Worldwide Perspective
Course Leaders: Jan Vardaman – TechSearch International Inc. and Tom Chung – FICTA Technology Inc.

Course Objective:

Will present an updated and broad perspective of microelectronics packaging and interconnect technology, from chip to board level especially in the key development areas such as ball grid array (BGA), Chip Scale Packaging (CSP), and Flip Chip (FC).

Course Content:

- Overview of microelectronics packaging and interconnect technology
- Trends in microelectronics packaging and interconnection
- BGA-Definition, options and characteristics; key guidelines and considerations for design, assembly and reliability; major volume applications and package types, snapshots and new developments
- CSP-Definition, options and characteristics; key quidelines and considerations for design, assembly and reliability; major volume applications by package type, snapshots and new developments including wafer-level CSPs
- Flip-chip related technologies-Definition, options and characteristics; key guidelines and considerations for design, assembly and reliability; future trends in new applications, snapshots and new developments
- BGA versus CSP versus Flip Chip–Comparisons design issues, performance, manufacturability, and applications

In addition, samples of packages/ substrates/modules will be used during this course to illustrate the topics described above.

Who Should Attend:

This course will be beneficial to all managers and individual contributors from electronic industry who need fundamental understanding and broad perspective on microelectronics packaging and interconnect technology especially in technology trends and key developmental areas such as BGA, CSP and Flip Chip.

Afternoon Courses
1:30 PM - 5:00 PM

5. Fiber-Optics Structures: Design for Reliability
Course Leader: E. Suhir – Lucent Technologies, Inc.

Course Objective:

Examine typical failure modes and mechanisms in microelectronics and photonics materials and structure, and present easy-to-use formulas indicating the role of the major factors affecting their reliability. Discuss how to choose the appropriate material(s) for a particular design and how to change, if necessary, the geometrical characteristics of the design to create a viable and reliable fiber optic structure.

Course Outline:

- Bending of bare fibers
- Bare fibers under the combined action of bending and tension
- Role of the nonlinear stress-strain relationship of the silica material
- Polymer coated or metallized fibers
- Optical glass fibers adhesively bonded at the ends: role and interaction of the "global" and "local" thermally induced stresses
- Elastic stability and microbending of optical fibers
- Solder materials and joints for photonics applications
- Thermally induced stresses in optical fibers soldered into ferrules
- Dynamic response of fiber optic structures to shocks and vibrations

Who Should Attend:

Engineers and technical managers that would like to get familiar with the mechanical, materials and reliability problems encountered in the fiber optics engineering.

6. Wafer Scale Packaging – Principles and Practices
Course Leader: Tom Chung – FICTA Technology Inc.

Course Objective:

Will review and discuss fundamentals and latest developments of Wafer Scale Packaging (WSP) technology including definition, types of WSP, manufacturing considerations and issues, board assembly guidelines, reliability data and guidelines, and applications especially in the area of Wafer Level Chip Scale Packaging (WLCSP).

Course Content:

- Introduction
- WSP Technology – Options and examples of WSP, WSP versus WLCSP, WSP versus conventional single chip package (SCP), pros and cons, concerns and issues for WSP manufacturing and applications, board assembly and rework of WLCSP, reliability data, etc.
- Design concerns/barriers/guidelines for WLCSPs – Electrical and thermomechanical performance, availability of chip scale substrate, escape routing guideline, etc.
- WLSCP infrastructure, developments, and applications – Assessment and comparison of various CSPs, availability of CSPs, examples of WLCSP suppliers, users and applications, standards, WLCSP status and new developments, Wafer Level Burn-in and Test (WLBT), CSP as a KGD/MCM enabler, CSP cost considerations and comparison, WLCSP versus CSP versus Flip Chip, etc.
- Summary

In addition, samples of packages/substrates modules will be used during this course to illustrate the topics described above.

Who Should Attend:

This course will be beneficial to all managers and individual contributors from the microelectronics industry who need fundamental understanding and broad perspective on WSP especially in the areas of technology options, pros and cons, trends, key considerations and developments.

7. RF/Wireless Packaging: Status and Challenges
Course Leaders: Manos M. Tentzeris and Joy Laskar – Georgia Institute of Technology

Course Objective:

The objectives of this course are to review the latest developments affecting next generation RF/Microwave Packaging: Vertical Interconnects (Flip-Chip/BGA), Embedded Components (Filters, Passives and Multilayer design) and MEMs (current state of the art and future developments). The course material is primarily based upon the instructors research at Georgia Tech's Packaging Research Center in collaboration with numerous industries and universities.

Course Outline:

- Multilayer Technologies (LTCC, HDI, PCB)
- Embedded Passives (e.g. Inductors) and Challenges of their application to Resonators and Filters in Wireless Systems
- Vertical Interconnects (BGA, Flip-chip)
- RF-MicroElectroMechanical Systems (RF-MEMS)
- Popular Numerical Techniques for the Design of RF Packages (Commercial Tools, FDTD, MRTD)

Who Should Attend:

The course is intended to both the packaging expert (Electrical and Mechanical Engineers) as well as persons new to the field. The course will concentrate on new and emerging technologies and their impact on the electrical performance at RF-Microwave Frequencies.

8. Thermal Management, Thermal/Thermomechanical Modeling, Packaging, and Reliability of Plastic IC Packages
Course Leaders: Tony Mak – Dallas Semiconductor Corporation and An-Yu Kuo – Optimal Corporation

Course Objective:

Today's electronics components are driven by the move of lower cost and higher performance. With increasing requirements for higher power on the plastic IC packages, proper thermal designs are essential for reliable operation of the electronic components or products. In addition to thermal requirements, plastic IC packages are also designed to withstand both mechanical and thermal stresses under given environmental loading conditions. This course covers thermal design guidelines for reliability and packaging, application of finite element methods for plastic IC package thermal/thermomechanical modeling and analysis, measurement techniques for thermal characterization of plastic IC packages.

Course Outline:

- Overview of thermal management of both plastic IC leaded and BGA packages
- Package design for reliability (examples and packaging guidelines)
- Methods of thermal characterization
- Thermal finite element modeling of plastic IC packages
- Influence of temperature on microelectronics
- Moisture induced reliability issues
- Warpage, Popcorn, Delamination & Die Cracking
- Key material properties to plastic IC package reliability
- Use of the finite element methods to predict package reliability
- Solder joint fatigue

Who Should Attend:

Engineers, managers, and technical staff who are involved with IC package application, package design and development, analysis, and manufacturing of plastic IC packages and subassemblies.

All-Day Courses
8:30 AM - 12:00 PM & 1:30 PM - 5:00 PM

9. Polymers for Electronic Packaging: Materials, Process and Reliability: Part I-The Fundamentals of Packaging and Materials Science and Engineering
Course Leader: C.P. Wong – Georgia Institute of Technology

Course Objective:

Polymers are widely used in electronic packaging as adhesives, encapsulants, insulators, dielectrics, molding compounds and conducting elements for interconnects. These materials also play a critical role in the recent advances of low-cost, high-performance multi-chip module (MCM), chip-on-board (COB), Ball Grid Array (BGA), Flip-Chip (FC), Novel No Flow Underfills, Chip Scale Packaging (CSP) and Reliability without Hermeticity (RWOH) Plastic Packaging. It is imperative that both material suppliers, formulators and their users have a thorough understanding the polymeric materials and their importance in the advances of the electronic packaging and interconnect technologies.

Course Outline:

- The Present and Next Generation of Electronic Packaging
- The Next Generation of Electronic Interconnects – Materials and Processes
- Pre-packaging Preparation – Cleaning Methods and Controls
- Recent Advances in RWOH by Polymers
- Overview Electronic Packaging: Present and Future Trends
- Fundamentals of Polymers and their Physical and Mechanical Properties Measurements
- IC Device Interconnection and Packaging Technology
  - Wire-bond, TAB, Flip Chip, Polymer Interconnects – Current and Future Trends
- Purpose of Pre-encapsulation Cleaning, Encapsulation and Packaging
  - Conventional Cleaning, Reactive Oxygen and Hydrogen Cleaning Processes
- Overview of Inorganic and Organic Polymers for Electronic Packaging
  - Silicon Dioxides Nitrides and Oxynitrides
  - Epoxies, Silicones, Polymides, Silicone-Polyimides, Polyurethanes, Benzocyclobutenes, Parylenes, BT resins, Sycars, Polyester, High Temperature and Liquid-crystal polmers
- Reliability Testing of Polymeric Materials – Test Set Up
- Recent advances in non-hermetic MCM packaging

Who Should Attend:

Engineers, scientists and managers involved in the design, process and manufacturing of IC electronic components and hybrid packaging, electronic material suppliers involved in materials, manufacturing and research and development.

10. Polymers for Electronic Packaging: Materials, Process and Reliability – Part II
Course Leader: C.P. Wong – Georgia Institute of Technology

Course Objective:

Polymers are widely used in electronic packaging as adhesives, encapsulants, insulators, dielectrics, molding compounds and conducting elements for interconnects. These materials also play a critical role in the recent advances of low-cost, high-performance multi-chip module (MCM), chip-on-board (COB), Ball Grid Array (BGA), Blip-Chip (FC), Novel No Flow Underfills, Chip Scale Packaging (CSP) and reliability without hermeticity (RWOH) Plastic Packaging. It is imperative that both material suppliers, formulators and their users have a thorough understanding of polymeric materials and their importance in the advances of the electronic packaging and interconnect technologies.

Course Outline:

- Next Generation of Electronic Packaging
- Common Electronic Packaging Materials: Conformal Coating, Glob-top, Potting and Casting
- Epoxy Modeling Compounds – Materials: Processes and Reliability
- Ball Grid Array Packaging
- Chip Scale Packaging
- Low-cost Flip-Chip Packaging: Materials and Processes
- Overview of Semiconductor Packaging Technology
- Packaging Techniques
  - Conformal Coating, Chip-on-Board, Glob-top, Molding, Potting
- Recent Advances in Epoxy Molding Compounds
- Chip Scale Packaging (CSP)
- BGA Packaging
- The Next Generation of Flip-Chip Packaging: Materials, Processes and Reliability

Who Should Attend:

Engineers, scientists and managers involved in the design, process and manufacturing of IC electronic components and hybrid packaging, electronic material suppliers involved in materials manufacturing and research and development.

11. Business and Technical Perspectives for Optical Networking and Optoelectronics Components
Course Leaders: Michael Lebby – Intel Corporation and Bill Ring – Tycoelectronics

Course Objective:

The next generation of telecommunications opportunity will come from today's implementation of basic WDM systems to more efficient and higher performance optical networks. These high performance and efficient networks will be enabled by new optoelectronic component technologies and new system architectures. This course review and road maps some of the key optoelectronic component and module based technologies that will be needed to support telecommunications over the next decade.

Course Outline:

- Overview of Datacom and Telecom Environment
  - Optical Networking – impact
  - Optical Components for Networking – impact
- Effect of WDM on the Optical Network
  - New Architectures with DWDM
  - Network Bottlenecks – areas for upgrade
- Network Components
  - Active Solutions
  - Passive Solutions
- Optical Network Trends
  - Road Maps
  - Market Impact
- Investment in Optical Networking
  - Trends in Optical Networking
- Future Trends

Who Should Attend:

This course is intended for engineers and managers who are interested in building a vision of optical components and networking trends. The course will benefit those who require a fundamental understanding and broad perspective on business and technology issues and those who want to review technology road maps that show how the optical architecture and associated optical components will evolve.

12. Optoelectronics Components and Modules for Datacom and Telecom
Course Leaders: Michael Lebby – Intel Corporation and Bill Ring – Tycoelectronics

Course Objective:

Optoelectronics components and modules for the Telecommunication industry and Datacom Networks are rapidly advancing in terms of speed, lower cost and design. The main objectives of this course are to review the current and future trends for active devices and packaging technology for discrete components and data network modules. The course will cover in detail the fundamental active III-V devices and components used today and review current trends in both III-V device technology and packaging for telecom and datacom applications.

Course Outline:

- Overview of Datacom and Telecom Requirements
  - Networks and Applications
  - System Requirements and Reliability
- Semiconductor Devices for Telecom/Datacom
  - Edge Emitting Fabry-Perot Devices
  - Distributed Feedback and Grating Devices
  - EA Modulators
  - Pump Sources
  - VCSEL Devices
  - PINs
- Packaging Technology for Telecom and Datacom Components
  - Active Alignment
  - Passive Alignment
  - Hermetic vs. Non-hermetic
  - System Issues
- Modules for Datacom
  - SC Duplex
  - Small Form Factor
  - Pluggable
- Future Trends

Who Should Attend:

This course is intended for engineers and managers who are involved in the design of components and modules for communication networks. It will be beneficial for those who require a fundamental understanding and broad perspective on active components for datacom and telecom, especially technology, trends, pros and cons and key developments.

Note: Courses 9, 10, 11 or 12 can be taken as self-contained Half-Day Short Courses.

Continuing Education Units

The IEEE Components, Packaging and Manufacturing Technology Society (CPMT) has been authorized to offer Continuing Education Units (CEUs) by the International Association for Continuing Education and Training (IACET) for all Short Courses that will be presented at the 50th ECTC. CEUs are recognized by employers for continuing professional development as a formal measure of participation and attendance in "non-credit" self-study courses, tutorials, symposia and workshops. IEEE CPMT CEUs can be applied towards the newly created "IEEE CPMT" Professional Development Certificate." Complete details including voluntary enrollment forms will be available at the conference. All costs associated with ECTC Short Courses-CEUs will be underwritten by the conference, i.e. no additional costs for Short Courses attendees to obtain CEU credits.

Register early. Don't wait until the last minute. You will save time at the Registration Desk if you have registered in advance. Make sure you have your receipt or a copy of your fax to verify your registration.
See you in Las Vegas!

50th ECTC Program Sessions

Monday, May 22, 2000

8:00 A.M. - 12:00 P.M.
Session 01: Automated Assembly of Optoelectronic Modules
Committee: Optoelectronics
Session CoChairs:
Mark W. Beranek – The Boeing Company
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Atsushi Takai – Hitachi, Ltd.
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High Accuracy Machine Automated Assembly for Opto Electronics
G. Lecarpentier – Karl Suss France S. A.

Automated Fiber Attachment for 980nm Pump Modules
P. Muller, B. Valk – JDS Uniphase AG

Automation Manufacturing Systems Technology for Opto-electronic Device Packaging
S. Jang – Newport Corporation

Submicron Flip Chip Bonding Technology for Optoelectronic Devices
A. Yamauchi – Toray Engineering Co., Ltd.

Automated Mass Production Line for Optical Module Using Passive Alignment Technique
K. Yamauchi, K. Kurata, M. Kurihara, Y. Sano, Y. Sato – NEC Corporation

Fiber-Optic Pigtail Assembly and Attachment Shift Using a Low-Cost Robotic Platform
C. R. Witham, M. W. Beranek, B. R. Carlisle, E. Y. Chan, D. G. Koshinz – Adept Technology

Automated Surface Mounting of Miniaturized Optical Elements
A. Wuersch, C. de Graffenried, R. Clavel, R.P. Salathe, T. Sidler, B. Gachter, H. Ehbets, P. Vigouret, C.A. Knuchel – EPFL

8:00 A.M. - 12:00 P.M.
Session 02: Flip Chip
Committee: Interconnections
Session CoChairs:
Rajen Dias – Intel Corporation
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Email: rajen.c.dias@intel.com

Christine Kallmayer – TU Berlin
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Investigation of Under Bump Metallization Systems for Flip-Chip Assemblies
T. P. Siong, H. Y. Wen, T. C. Hang, M. R. Marks, L. T. Beng – Singapore Institute of Microelectronics

Behavior of Platinum as UBM in Flip Chip Solder Joints
M. Klein, B. Wiens, M. Hutter, H. Oppermann, R. Aschenbrenner, H. Reichl – Fraunhofer IZM

Squeegee Bump Technology
J. K. Lin, T. Fang, R. Bajaj – Motorola,Inc.

The Effect of Cu Stud Structure and Eutectic Solder Electroplating on Intermetallic Growth and Reliability of Flip-Chip Solder Bump
X. Guowei, P. Chan, C. Jian, A. Teng – The Hong Kong University of Science and Technology

Kinetics of Flip Chip Solder Bump Degradation in Overly Aggressive Storage Test (HTOL)
R. N. Master, P. Patel, R. Blish, A. Ghaemmaghami, S. Yin – Advanced Micro Devices

Comparison of Electroplated Eutectic Sn/Bi and Pb/Sn Solder Bumps on Various UBM Systems
S. Y. Jang, K. W. Paik – Korea Advanced Institute of Science and Technology

Failure Mechanisms of Flip Chip Assembly Using Eutectic Solder
Q. Tan, A. Mistry, C. Beddingfield – Motorola Inc.

8:00 A.M. - 12:00 P.M.
Session 03: Wafer-Level Packaging Technologies
Committee: Advanced Packaging
Session CoChairs:
Phil Garrou – DOW at MCNC
Tel: 919-248-9261 Fax: 919-248-9265
Email: pegarrou@dow.com

Tim Adams
Dow Corning Corporation
Tel: 517-496-8867 Fax: 517-496-5121
Email: tim.adams@dowcorning.com

Fab Integrated Packaging (FIP): A New Concept for High Reliable Wafer-Level Chip Size Packaging
M. Topper, J. Auersperg, V. Glaw, P. Coskina, D. Jager, D. Petter, O. Ehrmann, K. Samulewicz, C. Meinherz, C. Karduck, S. Fehlberg, H. Reichl – Fraunhofer IZM Berlin / Technical University of Berlin; K. Kaskoun, E. Prack, B. Keser – Motorola

Board Level Reliability of a Waferlevel CSP using Stacked Solder Spheres and a Solder Support Structure (S3)
J. Simon, H. Reichl – Technical University of Berlin

The Solder Joint and the Runner Metal Reliability of Wafer-Level CSP, Omega-CSP
I. S. Kang, I. S. Park, J. H. Kim, J. W. Cho – HYUNDAI Electronics Industries Co., Ltd.

Low Cost Wafer-Level CSP: A Novel Redistribution Methodology
G. A. Rinne, J. D. Walling, J. D. Mis – Unitive Electronics Inc.

A Manufacturing Perspective of Wafer Level CSP
L. Nguyen, N. Kelkar, S. Lee and H. Takiar – National Semiconductor Corporation

Recent Advances on a Wafer-Level Flip Chip Packaging Process
Q. Tong, B. Ma, A. Savoca, L. Nguyen, C. Quentin, C. P. Wong, S. Luo – National Starch and Chemical Company

Wafer Level CSP Using Low Cost Electroless Redistribution Layer
T. Teutsch, T. Oppert, E. Zakel – Pac Tech - Packaging Technologies GmbH

8:00 A.M. - 12:00 P.M.
Session 04: Solder Technology
Committee: Materials & Processing
Session CoChairs:
Chin C. Lee – University of California
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William E. Estes – DuPont Photopolymers & Elec. Matls.
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Low Temperature Fluxless Bonding Technique Using In-Sn Composite
S. Choe, W. W. So, C. C. Lee – University of California

Mounting of High Power Laser Diodes on Boron Nitride Heat Sinks Using an Optimized Au/Sn Metallurgy
W. Pittroff, G. Erbert, G. Beister, F. Bugge, A. Klein, A. Knauer, J. Maege, P. Ressel, J. Sebastian, R. Staske, G. Traenkle – Ferdinand-Braun-Institut fur Hochstfrequenztechnik

Screen Printing, Placement and Joining Technologies with Leadfree Joining Materials
M. Detert, Th. Herzog, K.-J. Wolter, Th. Zerna – Dresden University of Technology

Lead-Free Flip Chip Process Development
K. Gaffney, J. Poarch, D. Delaney – Motorola, Inc.

Microstructural Coarsening of Lead-Free Solder Joints During Thermal Cycling
L. Ye, Z. Lai, J. Liu, A. Tholen – Chalmers University of Technology

Interface Microstructure and Mechanical Fatigue Behavior of Sn63Pb37 on Electrolytically Plated Cu and Ni
C. Zhang, P. Liu, J.-K. Shang – Motorola

A Study of Solder Paste Flow inside a Sealed Printing Head
D. He, N. N. Ekere – University of Salford

8:00 A.M. - 12:00 P.M.
Session 05: Solder Materials and Joints Reliability
Committee: Quality & Reliability
Session CoChairs:
Ephraim Suhir – Lucent Technologies
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George Harman – NIST
Tel: 301-975-2097 Fax: 301-948-4081
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Failure Modes and Mechanisms in Organic Land Grid Array Packages
R. Dias, A. Lucero, S. Niemeyer – Intel Corporation

Missing Solder Ball Failure Mechanisms in Plastic Ball Grid Array Packages
C. H. Zhong, C. P. Howel – Broadcom Corporation; S. Yi – Nanyang Technological University; Y. C. Mui – Advanced Micro Devices; D. Olsen, W. T. Chen – Institute of Material and Engineering Research

Material Challenges for Wafer-level Flip-Chip Packaging
B. Ma, E. Zhang, S. H. Hong, Q. K. Tong, A Savoca – National Starch and Chemical Company

The Influence of Room Temperature Aging on Ball Shear Strength and Microstructure of Area Array Solder Balls
R. J. Coyle, P. P. Sloan, A. J. Serafin – Bell Labs, Lucent Technologies

Mechanical Behavior of Reflow Soldered Lead-free Joint
J. R. P. Nykunen, G. A. Grandi, J. P. Lavlkko, S. T. Nurml, T. K. Lepisto, E. Ristolainen – Tampere University of Technology

Advanced Packaging Technologies in MOSFETS for Power Management
A. Tsui, J. Sarkis, H. Chen – Vishay/Siliconix

Processability and Reliability of *Commercial Palladium Plated Structures*
K.C. Chan, T.C. Chai, Z.Y. Yang, R. Gopalakrishnan – Institute of Microelectronics

8:00 A.M. - 12:00 P.M.
Session 06: Passive Components - Embedded and Systems
Committee: Components & RF
Session CoChairs:
Rao Bonda – Motorola, Inc.
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Albert F. Puttlitz – Consultant
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Novel High Dielectric Constant Nano-structure Polymer-ceramic Composite for Embedded Capacitor Application
Y. Rao, C. P. Wong, S. Ogitani, P. Kohl – Georgia Institute of Technology

The Ferrite Embedded Drop-in Circulator for Millimeter Wave Communications System
Y. Okada, Y. Shimada, M. Furuya, O. Myohga, T. Shimoto, N. Senba – NEC Corporation

A Low-Cost and High-Density RF Multi-Chip Module Transceiver For 1.8 GHz Personal Communication Service
W. Ryu, J. Kim, N. Kim, H. Kim, S. Ahn, J. Kim – Korea Advanced Institute of Science and Technology; S. Kim, H. Song, S. Lee – LG Production Eng. Research Center

Statistical Analysis of Embedded Capacitors Using Passive Modeling Methodology and Monte Carlo Simulation
L. Carastro, H. Yun, R. Poddar, M. A. Brooke, G. S. May, N. M. Jokerst – Georgia Institute of Technology

Packaging-Compatible Microtransformers on a Silicon Substrate
J. Y. Park, H. K. Hong, J. U. Bu LG Corporate Institute of Technology

Embedded Passive Components in MCM-D for RF Applications
C.-W. Ju, S.-P. Lee, Y.-M. Lee, S.-B. Hyun, S.-S. Park, M.-K. Song – Electronics and Telecommunications Research Laboratory

Complex Ultrasound Emitter and Micro-Wave Irradiator for Inner-Cavity Action
S. V. Belavskaya, V. A. Vityugov, V. G. Adoniev, L. I. Lisitsyna – Novosibirsk State Technical University

Monday, May 22, 2000

1:30 P.M. - 5:30 P.M.
Session 07: Optical Alignment Techniques
Committee: Optoelectronics
Session CoChairs:
Dariusz Sieniawski – Nortel Networks
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Bill Ring – Hewlett-Packard Company
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An Innovative Micro Optical Elements Assembly Robot Characterized by High Accuracy and Flexibility
A. Wuersch, M. Scussat, de Graffenried, R. Clavel, R.P. Salathe, T. Sidler, B. d Gachter, H. Ehbets, P. Vigouret, C.A. Knuchel – EPFL

Analysis of Alignment Tolerant Hybrid Optoelectronic Receivers for High Density Interconnection Substrates
M. Vrazel, N.M.Jokerst, R. Malloy, Y. Joo, M. Brooke, J. Chang, L. Carastro – Georgia Institute of Technology

3D Optoelectronic Stacked Processors and Free-Space Optical Interconnects
P. Marchand, S. Esener, X. Zheng, D. Huang, E. Yuceturk, Y. Liu, M. Hibbs-Brenner, V. Ozguz, J. Carson, S. He, D. Albert – UCSD-ECE

Two-Dimensional Optical Interconnect between CMOS IC's
L. Vanwassenhove, R. Baets, M. Brunfaut, J. Van Campen-hout, J. Hall, K. Ebeling, H. Melchior, A. Neyer, H. Thienpont, R. Vounckx, J. Van Koetsem, P. Heremans, F.-T. Lentes, D. Litaize – University of Gent-IMEC

Methods for Passive Fiber Chip Coupling of Integrated Optical Devices
R. Hauffe, R. Moosburger, U. Siebel, K. Petermann, J. Kropp, D. Arndt – Technical University of Berlin

Comparison of Active and Passive Fiber Alignment Techniques for Multimode Laser Pigtailing
P. Karioja, J. Ollila, V.-P. Putila, K. Keranen, J. Hakkila, H. Kopola – VTT Electronics & Infotech Oulu

Electroless Plating of Optical Fibers for Hermetic Feedthrough Seals
J. E. Watson, G. Shreve, M. Miller, D. Stevens, C. Sykora, D. LaBella, K. Ostby, W. Smith – 3M Fiber Optics and Electronic Materials Technology Center

1:30 P.M. - 5:30 P.M.
Session 08: Systems Level Electrical and Thermal Modeling
Committee: Modeling & Simulation
Session CoChairs:
John L. Prince – University of Arizona
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Tony Mak – Dallas Semiconductor Corporation
Tel: 972-371-4364 Fax: 972-371-4381
Email: t.mak@ieee.org

Bandwidth Predictions for High-Performance Interconnections
A. Deutsch, G V. Kopcsay, P.W. Coteus, C.W. Surovic, P. E. Dahlen, D. L. Heckmann, D.-W.Dian – IBM Research Division, T. J. Research Center

Design, Modeling and Simulation Methodology for Source Synchronous DDR Memory Subsystems
N. Pham, M. Cases, J. Bandyopad-hyay – IBM Corporation, Netfinity PC Servers

Enhancing Power Distribution System through 3D Integrated Models, Optimized Designs, and Switching VRM Model
Y. L. Li, David G. Figueroa, C. Y. Chung, T. G. Yew, Shamala A. Chickamenahalli – Intel Corporation

Meeting the Heat Removal Requirements of High Density Wafer Level Packages
C. Patel, S. Agraharam, K. Martin, J. Meindl – Georgia Institute of Technology

Bridging the Gap: Package Level and System Level Thermal Modeling
W. Wang, S. Liou, Y. S. Sun, J. Y. Lai, C. Tien, T. D. Her, M. Michael, B. Jafari – Siliconware USA Inc.

High Resolution Thermal Simulation of Electronic Components
G. Hanreich, J. Nicolics – Vienna University of Technology, Inst. 355

Thermal and Electrical Performance for Wafer Level Package
S. W. Park, J. M. Kim, H. Gil Baik, J. T. Moon – Hyundai Electronics Co., Ltd.

1:30 P.M. - 5:30 P.M.
Session 09: Underfill Materials
Committee: Materials & Processing
Session CoChairs:
Rajen Chanchani – Sandia National Laboratories
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A. Schubert – Fraunhofer Institute
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Fax: 011-49-30-46403-211
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Investigation on Effect of Coupling Agents in Epoxy Based Underfill Material for Flip-Chip Applications
S. Luo, C. P. Wong – Georgia Institute of Technology

Study of Reliability and Processability for Preset Under Fill Sheet Material As Future Standard Flip Chip Packaging Process
H. Noro, M. Mizutani, M. Kuwamura, H. Usui, S. Ito – Nitto Denko Corporation

Study on Reflowable Underfill Materials for Different Clip Chip Processes
C. Kallmayer, E. Jung, K.-F. Becker, J. Kloeser, R. Aschenbrenner, H. Reichl – Fraunhofer Institute of Reliability and Microintegration

Studies on a Reflowable Underfill for Flip Chip Applications
T. Wang, C. Lum, J. Kee, T. H. Chew, P. Miao, L. Foo, C. Lin – Questech Solutions Pte., Ltd.

Evaluating Underfill Materials for High Reliability Applications
J. P. Goodelle, J. J. Gilbert, R. E. Fanucci – Lucent Technologies

Adhesion Characterization of No-Flow Underfills Used in Flip Chip Assemblies and Correlation with Reliability
J. Lu, B. Smith, D. F. Baldwin – Georgia Institute of Technology

Study on Rate-Dependent Behaviors of Underfills Based on Two-Phase Composites
H. Wang, Z. Qian, S. Liu, M. Lu, J. Wul – Wayne State University; C. P. Wong – Georgia Institute of Technology

1:30 P.M. - 5:30 P.M.
Session 10: Chip Scale Packaging
Committee: Advanced Packaging
Session CoChairs:
Sudipta K. Ray – IBM Microelectronics
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Raj N. Master – AMD
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Characterization of a Novel Fine Pitch Ball Grid Array Package for Flash Memory Application
Sidharth, V. Valluri, R. Gannamani, M. Zhang – Advanced Micro Devices

The Application of HITCE Ceramic Material for LGA-type Chip Scale Package
K. Maeda, M. Higashi, M. Kokubu, S. Nakagawa – Kyocera Corporation

Mini-LOC, A Low Cost, High Reliability Leadframe Based CSP Package
J.-M. Jao, T. Dar Her, C. P. Hung, E. Ko, R. H.Y. Lo – Siliconware Precision Industries Co., Ltd.

Chip-Scale Packaging of Power Devices and its Applications in Integrated Power Electronics Modules
X. Liu, G.-Q. Lu – Virginia Tech

Development of Flex Stackable Carriers
H. Isaak, P. Uka – Dense-Pac Microsystems

Triple-Chip Stacked CSP
Y. Fukui, Y. Yano, H. Juso, Y. Matsune, K. Miyata, A. Narai, Y. Sota, Y. Takeda, K. Fujita, M. Kada – SHARP Corporation

CSP Assembly Reliability and Effects of Underfill and Double-sided Population
R. Ghaffarian, N. P. Kim – California Institute of Technology

1:30 P.M. - 5:30 P.M.
Session 11: Reliability Test Methods
Committee: Quality & Reliability
Session CoChairs:
Patrick Thompson – Motorola, Inc.
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Jo Caers – Nederlandse Philips Bedrijven
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Fax: 011-31-40-273-6815
Email: caers_jfj@cft.philips.nl

Prediction of the Crack Initiation of GaAs in a Soldered Assembly
B. Su, M. L. Dunn, Y. C. Lee – University of Colorado at Boulder

Interfacial Degradation of Epoxy Coated Silicon Nitride
J. Park, D. G. Harlow – Lehigh University

Characterization of Interfaces Involving Electrically Conductive Adhesives Using Electron-Beam Moire and Infrared Microscopy
A. J. Slifka, E. S. Drexler – NIST

A Novel Method and Device for Solder Joint Quality Inspection by Using Laser Ultrasound
S. Liu, D. Erdahl, I. C. Ume – Georgia Institute of Technology; A. Acharil – Visteon-Ford

Wire Pull on Fine Pitch Pads: An Obsolete Test for First Bond Integrity
V. Sundararaman, D. Edwards, W. Subido, H.Test – Texas Instruments, Inc.

Qualification Processes of PEMS for a USMC Missile System: A Case Study
N. E. Strifas, C. W. Vaughan – Naval Surface Warfare Center D/D

Non-Invasive Optical Assessment of Packaging-Induced Defects in High-Power Laser Diodes
A. Baerwolff, J. W. Tomm – Max-Born-Institut fur Nichtlineare Optik und Kurzzeitspektroskopie

1:30 P.M. - 5:30 P.M.
Session 12: RF Components/Performance
Committee: Components & RF
Session CoChairs:
Amit P. Agrawal – Hewlett Packard Company
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Lih-Tyng Hwang – Motorola, Inc.
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MCM Technology for RF Tunable Band Pass Filters Implemented by Integration of GaAs FET's and Selectively Oxidized Porous Silicon (SOPS)
J.-S. Lee, M.-L. Ha, Y.-S. Keon – Korea Advanced Institute of Science and Technology

A New Method to Interconnect PCB Layers in GHz Frequency Range
S. Kiani – MIT; M. Khusid – Teradyne Connection Systems

Electrical Performance Improvements on RFICs Using Bump Chip Carrier Packages as Compared to Standard Small Outline Packages
T. S. Horng, S. M. Wu, J. Y. Li – National Sun Yat-Sen University; C. T. Chiu, C. P. Hung – Advanced Semiconductor Engineering

A New Technique for the High Frequency Characterization of Multi-Terminal Capacitors
D. G. Figueroa, Y. L. Li, C. Y. Chung, F. Yahyaei-moayyed, M. Taniguchi – Intel Corporation

RF Electrical Measurements of Fine Pitch BGA Packages
M. F. Caggiano, S. Bulumulla, D. Lischner – Rutgers University

High Frequency Performance of Integral Capacitors in Cofired Ceramic Substrates
Y. Taguchi, M. Itagaki, O. Inoue, J.-I. Kato, K. Eda – Matsushita Electric Industrial Co., Ltd.

Accurate Measurement and Characterization up to 50 GHz of CPW-Based Integrated Passives in Microwave MCM-D
G. Carchon, S. Brebels, W. De Raedt, B. Nauwelaers – ESAT-TELEMIC

Tuesday, May 23, 2000

8:00 A.M. - 12:00 P.M.
Session 13: High Speed Optoelectronic Packaging
Committee: Optoelectronics
Session CoChairs:
Werner Hunziker – Opto Speed SA
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William M. Sherry – ANADIGICS
Tel: 908-668-5000 ext.5582
Fax: 908-412-5985
Email: wsherry@anadigics.com

High Speed, High Performance Laser Modules
A. M. Benzoni – Ortel Corporation

High Speed Packaged Electro-absorption Modulators for Optical Communications
A. E. Bond, G. Shtengel, Y. Akulova, P. Singh and C. L. Reynolds – Bell Labs, Lucent Technologies

Packaging Technology for 40-Gb/s Optical Receiver Module with an MU-Connector Interface
N. Iwasaki, M. Yanagibashi, H. Tsunetsugu, K. Kato, F. Ishitsuka, M. Hosoya, H. Kikuchi – NTT Telecommunications Energy Laboratories

Impedance Measurement Techniques and Impedance Requirements of Package/Driver Interfaces with Lithium Niobate External Modulators
G. McBrien – JDS Uniphase

Module Packaging for High-Speed Serial and Parallel Transmission
H. Karstensen, F. Auracher, N. Ebel, J. Fiedler, V. Plickert, L. Melchior, L. Leininger, M. Bittner, M. Festag, M. Wicke, S. Meyer – Infineon Technologies AG

Physical Layer Strategies for 10 Gigabit Ethernet
R.V. Penty, M. Webster, A.B. Massara, I.H. White – University of Bristol

800Mbit/s/ch x 12ch, True DC-coupled Parallel Optical Interconnects Using Single-Mode Fiber and 1310 nm LD Array
A. Takai, H. Furuichi. K. Tonehira, A. Miura, Y. Fukashiro, S. Ueno, T. Haga, T. Toyonaka, T. Suejima, K. Saitoh – Hitachi Corporation

8:00 A.M. - 12:00 P.M.
Session 14: Electrical Modeling and Characterization
Committee: Modeling & Simulation
Session CoChairs:
Ravi Kaw – Hewlett Packard Company
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Bruce Kim – Michigan State University
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Email: kimb@egr.msu.edu

High-Frequency Electrical Performance of a New High-Density Multiple Line Grid Array (**MLGA) Package
S. Ahn, J.-W. Lee, J. Kim, W. Ryu, J. Kim – Korea Advanced Institute of Science and Technology; Y.-S. Kim, C. K. Yoon – Glotech

Rules for Robust Generation of Accurate Reduced-Order Model of High-Speed Coupled Interconnections
A. C. Cangellaris, M. Migarashi – University of Illinois at Urbana-Champaign

Characterization of Microstrip Meanders in PCB Interconnects
N. Orhanovic, R. Raghuram, N. Matsui – Applied Simulation Technology

An All Purpose Dispersive Multiconductor Interconnect Model Compatible with PRIMA
S. Pasha, A.C. Cangellaris, J.L. Prince – University of Arizona

Network Analyzer Calibration Methods for High-Density Packaging Characterization and Validation of Simulation Models
C. L. Hammond, K. L. Virga – University of Arizona

A Measurement Study of Transmission Lines on Microstrip and Stacked Pair Structure for High Speed Signals
T. Usami, Y. Ohdate, Y. Ikemoto, T. Suga – University of Tokyo; K. Otsuka – Meisei Unversity

Optimal Structure of Wafer Level Package for the Electrical Performance of RDD
M.-H. Ahn, D. Lee, S.-Y. Kang – Samsung Electronics Company

8:00 A.M. - 12:00 P.M.
Session 15: High Density Chip and PWB Technologies
Committee: Manufacturing Technology
Session CoChairs:
Claude Ladouceur – IBM Canada, Ltd.
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Tom Swirbel – Motorola, Inc.
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Ultra-thin Bumped and Stacked WLP Using Thru-Silicon Vias
S. Savastiouk, O. Siniaguine, E. Korczynski – Tru-Si Technologies

Sacrificial Metal Wafer Level Burn-In KGD
W. L. Ivy, P. Godavarti, N. Alizy, T. McKenzie, D. Mitchell – Motorola Inc. - Semiconductor Products Sector (SPS)

Hybrid Assembly Technology for Flip Chip on Chip (FCOC) using PBGA Laminate Assembly
J. Dufresne, S. Ouimet, T. R. Homa – IBM Corporation

Study on Metal Adhesion Mechanisms in High Density Interconnect Study on Metal Adhesion Mechanisms in High Density Interconnect Printed Circuit Boards
L. Martin – Motorola, Inc.; C. P. Wong – Georgia Institute of Technology

Manufacturing Productivity Improvements for PBGA and Flip Chip Substrates in PWB Factory
D. E. Chrzanowski, D. A. Stanke, R. A. Lapcevich – IBM Microelectronics

The Other Side of UV:YAG Laser in PCB Production, Some Experiments and Experiences, Not Always Microvia Related
R. Kohler, J. Kaminski – Multek Europe

Endoscopic Inspection of Solder Joint Integrity in Chip Scale Packages
Y. C. Chan, C. W. Tang, P. L. Tu – City University of Hong Kong

8:00 A.M. - 12:00 P.M.
Session 16: Material Characterization and Modeling
Committee: Materials & Processing
Session CoChairs:
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C.P. Wong – Georgia Institute of Technology
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The Mechanics and Impact of Hygroscopic Swelling of Polymeric Materials in Electronic Packaging
E.H. Wong, K.C. Chan, R. Rajoo, T.B. Lim – Institute of Microelectronics

Influence of Chemistry and Applied Stress on Reliability of Polymer and Substrate Interfaces
S. Y. Y. Leung, S.-J. Luo, D. C. C. Lam, C. P. Wong – The Hong Kong University of Science and Technology

Study on Surface Tension and Adhesion in Electronic Packaging
S. Luo, M. Vidal, C. P. Wong – Georgia Institute of Technology

Thermal and Mechanical Characterization of ViaLux (TM) 81: A Novel Epoxy Photo-Dielectric Dry Film (PDDF) for Microvia Applications
R. C. Dunne, S. K. Sitaraman, S. Luo, C. P. Wong, W. E. Estes, M. Periyasamy, J. C. Coburn – Georgia Institute of Technology

Interface Adhesion Between Copper Leadframe and Epoxy Molding Compound: Effects of Surface Finish, Oxidation and Dimples
J.-K. Kim, M. Lebbai, M. F. F. Yuen, J. Liu, J. H. Kim – Hong Kong University of Science and Technology

Modeling the Conduction Mechanism of Isotropic Conductive Adhesives: ECRM Model
A. Mikrajuddin, F. G. Shi, K. Okuyama, S. Chungpaiboonpatana, J. M. Adams, C. Davidson – University of California

Effective Dielectric Constant Prediction of Polymer-ceramic Composite Based on Self-consistent Theory
Y. Rao, J. Qu, C. P. Wong, T. Marinis – Georgia Institute of Technology

8:00 A.M. - 12:00 P.M.
Session 17: Flip Chip Reliability
Committee: Quality & Reliability
Session CoChairs:
Donna Noctor – Lucent Technologies
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Harry Charles – The Johns Hopkins Univ. APL
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Email: Harry_Charles@jhuapl.edu

Reliability Modeling of Flip-chip Interconnect Bump Extrusion
A. Lucero, N. Mencinger, R. Dias – Intel Corporation

Experimental and Numerical Reliability Investigations of FCOB Assemblies with Process-induced Defects
A. Schubert, R. Dudek, J. Kloeser, B. Michel, H. Reichl – Fraunhofer IZM; T. Hauck, K. Kaskeun – Motorola

Assessment of Flip Chip Interconnect Integrity using Scanning Acoustic Microscopy
R. K. Wolf, T. Hooghan, M. Bachman, R. Weachock – Lucent Technologies

Flip Chip Assembly Utilizing Anisotropic Conductive Films: A Feasibility Study
J. White, D. Delaney – Motorola, Inc.

Prediction of Fatigue Crack Initiation Between Underfill Epoxy and Substrate
D. Wu, Y. C. Lee – University of Colorado at Boulder

Thermally Induced Deformations in a Flip-Chip HDI Substrate
E. S. Drexler – NIST

Effect of Circuit Board Flexure on Flip Chips Before Underfill
M. K. Chengalva, N. Jester, S. C. Baxter – Delphi Automotive Systems

8:00 A.M. - 12:00 P.M.
Session 18: MEMS Packaging and Bonding Technology
Committee: Interconnections
Session CoChairs:
Matt Schwiebert – Agilent Technologies
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David McCann – Micro Systems Engineering, Inc.
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Email: mccannd@biotronik.com

Challenges in Interconnection and Packaging of Microelectromechanical Systems (MEMS)
R. Ramesham – California Institute of Technology

One Micron Precision, Wafer-Level Aligned Bonding for Interconnect, MEMS and Packaging Applications
A. R. Mirza – Electronic Visions, Inc.

MEMS Modular Packaging and Interfaces
M. Schuenemann, V. Grosser, R. Leutenbauer, H. Reichl, G. Bauer, W. Schaefer – Fraunhofer-Institute for Manufacturing Engineering and Automation IPA

MEMS Sensor Multi-chip Module Assembly with TAB Carrier-Pressure Belt for Aircraft Flight Testing
N. P. Kim, M. J. Holland, M. H. Tanielain, R. Poff – Boeing Phantom Works, Information, Communication, Sensor & Electronic Technologies

Solder Bars - A Novel Flip Chip Application for High Power Devices
P. Elenius, H. Yang, R. Benson – Flip Chip Technologies

Feasibility of Surface Activated Bonding for Ultra-fine Pitch Interconnection - A New Concept of Bump-less Direct Bonding for System Level Packaging
T. Suga – The University of Tokyo

Gold-Aluminum Wirebond Interface Testing Using Laser-Induced Ultrasonic Energy
B. M. Romenesko, H. K. Charles, B. K. Siu – The Johns Hopkins University

Tuesday, May 23, 2000

1:30 P.M. - 5:30 P.M.
Session 19: Low-Cost Optoelectronic Packaging
Committee: Optoelectronics
Session CoChairs:
Mitchell S. Cohen – IBM Corporation
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Alan J. Morrow – Corning, Inc.
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A Compact, Low-Cost WDM Transceiver for the LAN
B. E. Lemoff, L. Buckman, Andrea Schmit, D. W. Dolfi – Agilent Laboratories

Single Mode Fiber MT-RJ SFF Transceiver Module Using Optical Sub Assembly with a New Shielded Silicon Optical Bench
M. Iwase, T. Nomura, A. Izawa, H. Mori, S. Tamura, T. Shirai, T. Kamiya – The Furukawa Electric Co., Ltd.

A Novel Low-Cost Small-Form-Factor Transceiver Module
W. Hogan, D. Gaio, M. Cohen, J. Trewhella – IBM Corporation

Packaging CWDM Optics and Electronics for Low Cost Networking Applications
E. Grann, K. Herrity – Blaze Network Products

Low-Cost Laser Modules for SMT
W. Rehm, K. Adam, A. Goth, W. Jorg, J. Lauckner, J. Scherb, P. Aribaud, C. Artigue, C. Duchemin, B. Fernier, D. Keller, S. Kerboeuf, S. Rabaron, J.M. Rainsant, D. Tregoat, J.L. Nicque, A. Tournereau, P.J. Laroulandie, P. Berthier – Alcatel SEL AG

Low-Cost Packaging Techniques for Active Waveguide Devices
M. Shaw, M. Marazzi, S. Bonino – Pirelli Cavi & Sistemi

Electro-Optical Printed Circuit Board (EOPCB)
K. Schmieder, K.-J. Wolter – Dresden University of Technology

1:30 P.M. - 5:30 P.M.
Session 20: Power Distribution and EMI Modeling
Committee: Modeling & Simulation
Session CoChairs:
Moises Cases – IBM Corproation
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J. Peter Krusius – Cornell University
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Fax: 607-254-4777
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Noise Verification Across 3 Levels of Packaging Hierarchy for the IBM G5/G6 Mainframe
H. Smith, P. Venkatachalam, S. Kuppinger, W. Becker – IBM S/390 Laboratory

Physics Based Modeling of Simultaneous Switching Noise in High Speed Systems
S. Chun, M. Swaminathan, J. Srinivasan - Georgia Institute of Technology; L. D. Smith - Sun Microsystems; Z. Jin, M. K. Iyer – Institute of Microelectronics

Investigation of Power/Ground Plane Resonance Reduction Using Lumped RC Elements
G. W. Peterson, J. L. Prince, K. L. Virga – University of Arizona

Direct Generation of Spice-Compatible Passive Reduced-Order Models of Ground/Power Plants
M. J. Choi, K.-P. Hwang, A. Cangellaris – University of Illinois at Urbana-Champaign

Electromagnetic Radiation and Simultaneous Switching Noise in a CMOS Device Packaging
T. Sudo, J. Kudo – Toshiba Corporation

Effect of Plating Stubs of BGA Packages on Spurious EM Radiation
H. Yue, M. Lamson – Texas Instruments

Design, Simulation, Fabrication, and Characterization of Package-Level Micro-Shielding for EMI/EMC Management in BGA Environment
E. Diaz-Alvarez, J. P. Krusius – Cornell University

1:30 P.M. - 5:30 P.M.
Session 21: Low Cost Good Die (KGD/Burn-In)
Committee: Interconnections
Session CoChairs:
Paul A. Totta – IBM Corporation
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Corey Koehler – Amkor Technology
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The Die Products Consortium
S. Bridges, L. Gilg – National Semiconductor

An Overview of MCM/KGD Development Activities in Japan
T. Sudo – Toshiba Corporation

Single Chip Test and Burn-in
J. A. Forster – Texas Instruments, Inc.

Wafer Level Burn-In
D. Conti, J. VanHorn – IBM Corporation

Chip Scale Package vs. Direct Chip Attach
D. Arnold, R. Richmond – Texas Instruments

Selecting Methods for Packing, Shipping, and Handling of Low Cost Die
C. E. Gutentag, R. A. Sierra – Tempo Electronics

1:30 P.M. - 5:30 P.M.
Session 22: Plating and Under Bump Materials
Committee: Materials & Processing
Session CoChairs:
Eric Perfecto – IBM Microelectronics
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Ted Tessier – Micro Systems Engineering
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Selective Etching of Ti/TiW Barrier Layers in the Presence of Electroplated Pb-Sn Solders in Flip Chip Systems: Challenges and Development
L. N. Ramanathan, D. Mitchell, C. Beddingfield – Motorola, Inc.

Under Bump Metallurgies for a Wafer Level CSP with Eutectic Pb-Sn Solder Ball
S. J. Cho – Hyundai Electronics Industries

Investigation of High Reliability Micro Bump Plating Technique on Tape Carrier
A. Chinda, A. Matsuura, O. Yoshioka, M. Mita – Hitachi Cable, Ltd.

A Barrier Metallization Technique on Copper Substrates for Soldering Applications
W. W. So, S. Choe, R. Chuang, C. C. Lee – University of California

Advanced Surface Plating on the Organic FC-BGA Package
Y. Tomita, Q. Wu, A. Maeda, S. Baba, N. Ueda – MITSUBISHI Electric Corporation

Assessment on the Effects of Electroless Nickel Plating on the Reliability of Solder Ball Attachment to the Bond Pads of PBGA Substrate
S.-W.R. Lee, C. C. Yan, R. Yuen – The Hong Kong University of Science and Technology

Fabrication and Adhesion of Low Stress Electroless Ni-Cu-P Bump on Copper Pad
C.-J. Chen, K.-L. Lin – National Cheng Kung University

1:30 P.M. - 5:30 P.M.
Session 23: Adhesives
Committee: Materials & Processing
Session CoChairs:
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Johan Liu – Chalmers University of Technology
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Recent Advancements in Olefin Thermoset Adhesive
M. N. Nguyen, I. Y. Chien, P. M. Knoll – Honeywell Electronic Materials

Conductive Ink for Through Hole Applications
A. Y. Xiao, Q. K. Tong, A. C. Savoca, R. L. Frentzel, H. Van Oosten – National Starch and Chemical Company

Development of Conductive Adhesive Materials for Via Fill Applications
S.K. Kang, S. Buchwalter, N. Labianca, J. Gelorme, S. Purushothaman, K. Papathomas, V. Markovich, T. Miller, M. Poliks – IBM T. J. Watson Research Center

Development of High Performance Surface Mount Conductive Adhesives
Daoqiang Lu, C. P. Wong, Quinn K. Tong, Eric Zhang – National Starch and Chemical Company

Effect of Non-Conducting Filler Additions on Anisotropic Conductive Adhesives (ACAs) - Properties and Reliability of ACAs Flip Chip on Organic Substrates
M. J. Yim, K. W. Paik – Korea Advanced Institutes Science and Technology

Electrical Characteristics of an ACF Bond as a Function of Temperature and Humidity Aging
J. D. Weidler, R. D. Burg, J. H. Constable – State University of New York

Reworkable Underfills for Flip Chip, BGA, and CSP Applications
L. Wang, R. Kang, H. Li, D. Baldwin, C. P. Wong – Georgia Institute of Technology

1:30 P.M. - 5:30 P.M.
Session 24: MCM and Advanced Packaging Technology
Committee: Advanced Packaging
Session CoChairs:
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Rick Sigliano – Kyocera America, Inc.
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Packaging Technology for High Performance CMOS Server
A. Fujisaki, M. Suzuki, H Yamamoto – Fujitsu Limited

Multichip SMT Power Package for Automotive Market
H. Wieser, M. Paulasto, T. Hauck, C. Trigas – Motorola, Inc.

Design, Numerical Simulation and Optimization of Heat Sinks using Icepak(TM)
M. J. Marongiu, G. S. Fallon, M. K. Berhe – MJM Engineering Co.

Laser Programmable Multichip Module Using Vertical Make-link
J.-H. Lee, G. Zhuo, J. B. Bernstein – University of Maryland at College Park

Evaluation and Characterization of High-Performance Filling Encapsulants for System-on-Chip (SOC) Application
J. Wu, S. Bhattacharya, M. Wong, C. Lloyd, C. P. Wong, R. Tummala – Georgia Institute of Technology

MOSFET BGA Package
R. Joshi, H.Granada, C. Tangpuz – Fairchild Semiconductor Corporation

Over-coated Flip-chip Fine Package Development for MCM Fabricated with Si IC and GaAs MMIC
H. Kurata, K. Mitsuka, H. Matsushita – New Japan Radio Co., Ltd.; T. Ogata – Saga Electronics

Wednesday, May 24, 2000

8:00 A.M. - 12:00 P.M.
Session 25: Optoelectronic Packaging Materials and Reliability
Committee: Optoelectronics
Session CoChairs:
Martin Groeneveld – Uniphase Netherlands B.V.

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Jon Hall – Caswell Technology
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Highly Accelerated Life Testing for Non-Hermetic Laser Modules
C.D. Theis, D.J. Siconolfi, R.B. Comizzoli, P.A. Kiely, U.K. Chakrabarti, J.W. Osenbach – Lucent Technologies

Self-Organized Waveguide Coupling Method "SOLNET" and its Application to Film Optical Circuit Substrates
T. Yoshimura – Fujitsu Computer Packaging Technologies, Inc.

New Technology for Electrical/Optical Systems on Module and Board Level
D. Krabe, F. Ebling, N. Arndt-Staufenbiel, G. Lang, W. Scheel – Fraunhofer-Institute for Reliability and Microintegration IZM

Epoxy Adhesives for Optical Element Attachment in Planar Passive Optical Components
J. G. Liu, B. M. Anderson, E. Bergman, S. Fairchild – Lucent Technologies, Inc.

Experimental and Numerical Studies in the Evaluation of Epoxy-Cured Fiber Optic Connectors
K. Broadwater, P. F. Mead – CALCE Electronics Products and Systems Consortium

The Corrosion Behavior of BK-7 Glasses for use in Non-Hermetic Electro-Optic Devices
C. D. Theis, D. A. Fleming, J. W. Osenbach – Lucent Technologies, Inc.

Modeling Alignment Shift of Soldered Optical Fiber
A. Powell
Massachusetts Institute of Technology

8:00 A.M. - 12:00 P.M.
Session 26: Electronic Packaging Education I
Committee: Education
Session CoChairs:
Paul Wesling – Tandem Computers, Inc.
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Rao R. Tummala – Georgia Institute of Technology
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Georgia Tech's Practice-oriented Masters Program in Microelectronics Packaging
L. Conrad, R. Tummala, G. May – Georgia Institute of Technology

Networking the Electronics Packaging Education
Z. Illyefalvi-Vitez, J. Nicolics, L. Golonka, P. Mach, P. Svasta – Technical University of Budapest

An Internet Course on Conductive Adhesives for Electronics Packaging
J. Liu, J. E. Morris – Chalmers University of Technology

New Course Development in Electronic Product and System Cost Analysis
P. Sandborn – University of Maryland

Mixed Signal System Design Course Development
H. Tenhunen – Royal Institute of Technology

Sensors' Education and Related Student Research Projects
G. Harsanyi, I. Lepsinji – Technical University of Budapest

Interactive Learning Modules for Electrical Engineering Education
D. L. Millard – Rensselaer Polytechnic Institute

8:00 A.M. - 12:00 P.M.
Session 27: Thermo-Mechanical Simulation and Modeling I
Committee: Modeling & Simulation
Session CoChairs:
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Pradeep Lall – Motorola, Inc.
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Effect of Simulation Methodology on Solder Joint Crack Growth Correlation
R. Darveaux – Amkor Technology, Inc.

Finite Element Modeling of BGA Packages for Life Prediction
G. Gustafsson, I. Guven, V. Kradinov, E. Madenci – University of Arizona

Revisit of Life Prediction Models for Solder Joints
T. Anderson, A. Barut, I. Guven, E. Madenci – University of Arizona

Determination of Visco-Elastic Properties During the Curing Process of Underfill Materials
L. J. Ernst, C. van 't Hof, D. G. Yang, M. S. Kiasat – Delft University of Technology; G. Q. Zhang, H. J. L. Bressers, J. F. J. Caers, A. W. J. den Boer, J. Janssen – Philips

FEA Simulation on Moisture Absorption in PBGA Packages Under Various Moisture Pre-Conditioning
L. T. Fai – Advanced Micro Devices (Singapore) PTE LTD

Durability/Reliability of BGA Solder Joints Under Vibration Environment
T. E. Wong, F. W. Palmierei, B. A. Reed, H. S. Fenger, H. M. Cohen, K. T. Teshiba – Raytheon Systems Company

Interfacial Adhesion Study for Low-k Interconnects in Flip-chip Packages
M. R. Miller, P. S. Ho – The University of Texas at Austin

8:00 A.M. - 12:00 P.M.
Session 28: Lead Free Interconnects: Solders and Conductive Adhesives
Committee: Interconnections
Session CoChairs:
Jong-Kai Lin – Motorola, Inc.
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Goran Matijasevic – ORMET Corporation
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Eutectic Sn-Ag Solder Bump Process for ULSI Flip Chip Technology
H. Ezawa, M. Miyata, S. Honma, H. Inoue, T. Tokuoka, J. Yoshioka – Toshiba Corporation Semiconductor Company

Flip Chip with Lead Free Solders on Halogen Free Microvia Substrates
G. Baynham, D. F. Baldwin, K. Boustedt, A. Johansson, C. Wennerholm, D. Patterson, P. Elenius – Georgia Institute of Technology

Under Bump Metallizations for Lead Free Solders
T. M. Korhonen, P. Su, M. A. Korhonen, C.-Y. Li – Cornell University

Novel Die Attach Films Having High Reliability Performance for Lead-Free Solder and CSP
S. Takeda, T. Masuko, Y. Hasegawa, Y. Odagawa, T. Kato – Hitachi Chemical Co., Ltd.

Effect of Joint Structure on Flip Chip Interconnection with FR4 Substrate Using Anisotropically Conductive Adhesive
Z. Lai, J. Liu – IVF-The Swedish Institute of Production Engineering Research

The Visibility of Anisotropic Conductive *Film (ACF) as a Flip Chip Interconnection Technology*
K. M. Kim, J. O. Kim, S. G. Kim, K. H. Lee, A. S. Chen, N. Ahmad, N. Dugbartey, M. Karnezos, S. Tam, Y. D. Kim, R. Pendse – ChipPAC, Inc.

Comparison of Flip Chip Technologies on Rigid Polyimide with Respect to Reliability and Manufacturing Costs
R. Miessner, C. Kallmayer, J. Kloeser, R. Aschenbrenner, H. Reichl, S. Ling, B. Le, A. Lew, R. Benson, E. Nhan – Fraunhofer Institute of Reliability and Microintegration

8:00 A.M. - 12:00 P.M.
Session 29: Connectors and Contacts
Committee: Connectors & Contacts
Session CoChairs:
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Rod Martens – Hewlett Packard Company
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How Do Material Properties of Electrical Conductors Effect the High Frequency Performance of Electrical Connectors?
J. Johnson, J. Milner – Brush Wellman

A New High Strength Copper-Tin-Zinc Alloy for Connectors and Other Conductive Springs
A. K. Bhargava – Waterbury Rolling Mills, Inc.

Development of a Wafer-Level Burn-in Test Socket for Fine-pitch BGA Interconnection
Q. Qiao, M. H. Gordon, W. F. Schmidt, Li Li, S. S. Ang, Biao Huang – University of Arkansas

High-Reliable Probe Card for Wafer Testing
S. Maekawa, M. Takemoto, Y. Kashiba – Mitsubishi Electric Corporation

Flexible Micro-Spring Interconnects for High Performance Probing
J. M. Haemer, S. K. Sitaraman, D. K. Fork, D. L. Smith, S. Mok, F. C. Chong – Georgia Institute of Technology

SMT Connectors for Removable Small Form Factor Transceiver Modules
W. Hogan, D. Gaio, S. Branch – IBM Corporation

The Effect of Sliding Wear on Lubricated Tin-Lead Contacts
N. Aukland, H. Hardee – New Mexico State University

8:00 A.M. - 12:00 P.M.
Session 30: BGA Packaging
Committee: Advanced Packaging
Session CoChairs:
Joseph W. Soucy – Draper Laboratory
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Luu Nguyen – National Semiconductor Corporation
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High Performance Package Designs for a 1.0 GHz Microprocessor
A. Hasan, A. Sarangi, C. S. Baldwin, R. L. Sankman, G. F. Taylor – Intel Corporation

Novel Jet Fluxing Application for Advanced Flip Chip and BGA/CGA Packages
R. N. Master, A. Dubey, M. Guardado, O. T. Ong, M.-L. Zhang, M. Khan, B. Donges, F. Okada – Advanced Micro Devices

New CBGA Package with Improved 2nd Level Reliability
R. Pendse, B. Afshari, N. Butel, J. Leibovitz, Y. Hosoi, M. Shimada, K. Maeda, H. Yonekura – ChipPAC Inc.

Assembly and Solder Joint Reliability of Plastic Ball Grid Array with Lead-Free Versus Lead-Tin Interconnect
K.-M. Levis, A. Mawer – Motorola Semiconductor Products Sector

Effect of Package Design and Layout on BGA Solder Joint Reliability of an Organic C4 Package
B. Chandran, D. Goyal, J. Thomas – Intel Corporation

Reliability of Flip Chip BGA Package on Organic Substrate
E.-C. Ahn, T.-J. Cho, J.-B. Shim, K.-W. Choi, H.-J. Moon, H.-K. Yoon, S.-Y. Kang, S.-Y. Oh – Samsung Electronics Co., Ltd.

Underfilled BGAs for Ceramic BGA Packages and Board-Level Reliability
T. Burnette, Z. Johnson, T. Koschmieder, B. Oyler – Motorola SPS

Wednesday, May 24, 2000

1:30 P.M. - 5:30 P.M.
Session 31: Parallel Optical Interconnects
Committee: Optoelectronics
Session CoChairs:
James E. Watson – 3M Company
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Torsten Wipiejewski – Siemens AG
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Current Progress of High Speed Parallel Optical Links for Computer Clusters and Switching Systems
K. Drogemuller, D. Kuhl, J. Blank, M. Ehlert, T. Kraeker, J. Hohn, D. Klix, V. Plickert, L. Melchior, P. Hildebrandt, M. Heinemann, F. P. Schiefelbein, L. Leininger, H.-D. Wolf, T. Wipiejewski, A. Ebberg – Infineon Technologies AG

Fabrication of a 2D Connector for Coupling a 4x8 Array of Small Diameter Plastic Optical Fiber (120/125 um) to MCLED or VCSEL Arrays
A. Van Hove, T. Coosemans, K. Naessens, L. Vanwassenhove, P. Van Daele, R. Baets – University of Gent

High Performance Selectively Oxidized VCSEL Arrays for Parallel High-Speed Optical Interconnects
F. Mederer, M. Grabherr, F. Eberhard, I. Ecker, R. Jager, J. Joos, C. Jung, M. Kicherer, P. Schnitzer, H. Unold, D. Weidenmann, K.J. Ebeling – University of Ulm

ParaBIT-1: 60-Gb/s-Throughput Parallel Optical Interconnect Module
M. Usui, N. Sato, A. Ohki, N. Matsuura, N. Tanaka, K. Enbutsu, M. Amano, M. Hikita, T. Kagawa, K. Katsura, Y. Ando – NTT Telecommunications Energy Laboratories

Packaging Aspects of the Litebus(TM) Parallel Optoelectronic Module
B. Chan, P. Fortier, L. Freitag, G.Johnson, J. Sherman, J. Kuczynski, f. Guindon, M. Letourneau – IBM/Rochester; D. Demangone, M. Mentzer, D. Naghski, B. Trostle – FCI Electronics

Realization of Phased-array Multi-Length Laser Using Hybridly Integrated PICs
D. Van Thourhout, A. Van Hove, T. Van Caenegem, K. Vandeputte, I. Moerman, P. Van Daele, R. Baets – University of Gent;

X. J. M. Leijtens, M. K. Smit – Delft Technical University

System Level Packaging of High Density Optoelectronic Interconnections
C. J. Sherman, J. S. Nyquist, G. J. Grimes – University of Alabama at Birmingham

1:30 P.M. - 5:30 P.M.
Session 32: Electronic Packaging Education II
Committee: Education
Session CoChairs:
Albert F. Puttlitz
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Andrew Tay – National University of Singapore
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Electronic Packaging Education at the University of Arkansas
W. D. Brown – University of Arkansas

A Web Based Course on Designing High Density Interconnect PCBs for Manufacturability
G. Ananda Rao, N. J. Rao – Indian Institute of Science

Distance Learning in Thermal Design of Electronic Systems-The IEEE/NSF Project
Y. Joshi, J. Sircars – CALCE Electronics Products; A. Bar-Cohen, K. Geisler – University of Minnesota; S. Bhavnani – Auburn University

Progress in Electronics Packaging Virtual Laboratory Development
P. Gordon, L. Hertel, I. Kallai, I. Lepsenyi, Z. Illyefalvi-Vitez, P. B. Bojta, L. Varnai – Technical University of Budapest

The Virtual Packaging Laboratory
G. S. May, D. L. Light – Georgia Institute of Technology

Recent Experiences on Developing Multimedia Educational Modules
B. C. Kim – Michigan State University

IC Packaging Education at the University of the Philippines
M. G. Mena – University of the Philippines, College of Engineering

1:30 P.M. - 5:30 P.M.
Session 33: Thermo-Mechanical Modeling and Simulation II
Committee: Modeling & Simulation
Session CoChairs:
Suresh K. Sitaraman – Georgia Institute of Technology
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George A. Katopis – IBM Corporation
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An Integrated Process Modeling Methodology and Module for Sequential Multilayered Substrate Fabrication using a Coupled Cure-Thermal-Stress Analysis Approach
R. C. Dunne, S. K. Sitaraman – Georgia Institute of Technology

Solder Joint Shape Formation Under Constrained Boundaries in Wafer Level Underfill
L. Nguyen and H. Nguyen – National Semiconductor Corporation

Modeling of Viscoelastic Effects on Interfacial Delamination in IC Packages
Z. Xiong, A. A. O. Tay – National University of Singapore

An Analysis of Interface Delamination in Flip-Chip PBGA Packages
L. L. Mercado, V. Sarihan, T. Hauck – Motorola Inc.

Numerical And Experimental Investigation of Large IC Flip Chip Attach
A. Schubert, R. Dudek, R. Leutenbauer, P. Coskina, K.-F. Becker, J. Kloeser, H. Reichl, D. Baldwin, J. Qu, M. Swaminathan – Fraunhofer Institute for Reliability and Microintegration IZM
C.P. Wong, R. Tummala, S. Sitaraman – Georgia Institute of Technology

Ceramic Column Grid Array (CCGA) Technology with Coated Solder Columns
B. Z. Hong, S. Ray – IBM Microelectronics

Advancing Polymer Process Understanding in Package and Board Applications Through Molecular Modeling
N. E. Iwamoto – Honeywell, Inc.

1:30 P.M. - 5:30 P.M.
Session 34: CSP Reliability
Committee: Quality & Reliability
Session CoChairs:
Darvin R. Edwards – Texas Instruments
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Robert Howard – R. T. Howard & Associates
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Solder-Joint Crack Propagation Analysis of WLCSP Assembly Under Thermal Cycling and Mechanical Shear Conditions
J. Lau, C. Chang, C.-C. Chen – Express Packaging Systems, Inc.

Vibration Fatigue of uBGA Solder Joint
P. L. Tu, Y. C. Chan, C. W. Tang, J. K. L. Lai – City University of Hong Kong

CSP Board Level Reliability Testing of Pb-free Sn-Ag-X (X=Cu,In) and Polymer-core Solder Balls
S. W. Yoon, J. T. Moon, N. S. Lee, C. J. Park, S. H. Hong, K. S. Park – Hyundai Electronics Industries Corporation

Reliability Characterization in Ultra CSP(TM) Package Development
H. Yang, P. Elenius, S. Barrett, C. Schneider, J. Leal, R. Moraca, R. Moody, Y.-D. Kweon, D. H. Kim, D. Patterson, T. Goodman – Flip Chip Technologies

Thermal Cyclic Fatigue of the Interconnect of a Flex-type BGA
S.C. Hung, P.J. Zheng, M.S. Liang, S.H. Ho – Advanced Semiconductor Engineering, Inc.
Effects of Lead Bonding Process on Reliability of Chip Scale Package
Y. J. Lee, M. W. Eyre – Dow Corning Corporation

New Evaluation Method of CSPs Board Level Reliability Using Strain Gauge
Y. Yamaji, T. Suzuki, H. Yamasaki, T. Ohishi, Y. Chikawa, N. Kako – Sharp Corporation

1:30 P.M. - 5:30 P.M.
Session 35: Lead-Free Soldering Technology
Committee: Manufacturing Technology
Session CoChairs:
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The Status of Lead-Free Solder Alloys
D. Suraski, K. Seelig – AIM Solder

Lead-Free Solder Implementation for Automotive Electronics
G. Whitten – Delphi Delco Electronics Systems

Lead-Free Electronic Interconnect-Current Status and Future Developments
K. G. Snowdon, C. G. Tanner – Nortel Networks

Lead Free Solder Paste Flux Evaluation and Implementation in Personal Communication Devices
A. Butterfield, V. Visintainer, V. Goudarzi – Motorola

Understanding the Process Window for Printing Lead-Free Solder Pastes
T. A. Nguty, N.N. Ekere
University of Salford

Extensive Fatigue Investigation of Solder Joints in IGBT High Power Modules
J.-M. Thebaud, E. Woirgard, C. Zardini, K.-H. Sommer – Universite Bordeaux 1

Characterization of the Melting and Wetting of Sn-Ag-X Solders
E. Bradley, J. Hranisavljevic – Motorola

1:30 P.M. - 5:30 P.M.
Session 36: Emerging Packaging Technology
Committee: Advanced Packaging
Session CoChairs:
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Karla Y. Carichner – Allied Signal
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Chip Scale Polymer Stud Grid Array Packaging and Reliability Based on Low Cost Flip Chip Processing
C. Paydenkar, D. F. Baldwin, B. Lewis – Georgia Institute of Technology

Silicon Interposer Technology for High Density Package
M. Matsuo, N. Hayasaka, K. Okumura, E. Hosomi, C. Takubo – Toshiba Corporation Semiconductor Company

Single level Integrated Packaging Modules for High Performance Electronic Systems
L.-R. Zheng, H. Tenhunen – Royal Institute of Technology

Embedded Passive Components in an RF MCM-L
D. Dearinger – Honeywell Advanced Circuits

High Power Chip Stacks with Interleaved Heat Spreading Layers
V. Ozguz, D. Albert, A. Camien, S. Gaddag, P. Marchand – Irvine Sensors

Development of Chip-on-Dot Flip Chip Technique Utilizing Gold Dot Flexible Circuitry
Z. P. Wang, Y.M. Tan, C. M. Schreiber, C. C. Tsui, J. Wei, Z. F Shi – Gintic Institute of Manufacturing Technology

Reliability of Ceramic Ball Grid Array Resistor Networks with Buried Capacitors
T. Bloom, R. Cooper – CTS Corporation

Tuesday, May 23, 2000

Session 37: Poster
Committee: Poster
Session CoChairs:
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Steve Bezuk – Kyocera America, Inc
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Packaging Guidelines for a Single Fiber Probe Based Reflective Sensors
A. K. Gnosh, A. K. Asundi – Nanyang Technological University

Fabrication of Silicon-on-Reflector for Si-based Resonant-Cavity-Enhanced photodetectors
C. Li, Q. Yang, H. Ou, Q. Wang – Chinese Academy of Sciences

Lens-less Semiconductor Optical Amplifier (SOA) Modules Using Laser Welding Techniques
M. W. Park – Samsung

Low Profile Package Technology for IrDA Compliant Transceivers
V. Nitsche – Vishay Semiconductor GmbH
Sensitivity of Lid Deflection Method for Leak Detection in Laser Pump Modules
J. Lewandowski, M. Fusco, B. Valk – JDS Uniphase AG

Alignment Considerations in Packaging Array-Based Optical Interconnects and Processors
A. K. Ghosh, P. Paul – Nanyang Technological University

The Effect of Temperature Cycling on Fiber-Solder-Ferrule Joints in Laser Module Packaging
W. H. Cheng, M. T. Sheen, J. H. Kuang, J. C. Chen, G. L. Wang, S. C. Wang, H. L. Chang, C. Wang, C. M. Wang – National Sun Yat-sen University

Advances in Multi-Channel Multi-Gbytes/ sec Bit-Parallel WDM Single Fiber Link
L. Bergman, C. Yeh, J. Morookian – California Institute of Technology

A Dry Silver Electromigration Process to Fabricate Optical Waveguides on Glass Substrates
R. Chuang, C. C. Lee – University of California

Application of Pade Approximation Via Lanczos (PVL) Algorithm to an Electromagnetic System with Expansion at Infinity
T. Zhou, S. L. Dvorak, J. L. Prince – The University of Arizona

An Efficient Wire Sweep Analysis Solution for Practical Applications
F. Su, S. K. Chen – ChipMOS Technologies, Inc.

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