Designing DC/DC Converters with the Si9110 Switchmode Controller

In distributed power systems and battery-powered equipment, the advantages of MOS over bipolar technology for pulse-width modulation (PWM) controllers are significant. First, by using a BiC/DMOS power IC process, a high-voltage DMOS transistor can be integrated with a CMOS PWM controller to serve as a pre-regulator stage. This reduces the number of external components by permitting the power controller IC to interface directly to the power bus.

The second advantage of MOS is speed. Bipolar PWM controllers can be made fast, but only with a significant increase in supply current. Logic gate delays of 5 ns are readily achievable using 5-µm CMOS, comparator propagation delays are in the 50- to 100-ns range, and the supply current is maintained *below 1 m*A.

How does speed translate into power supply performance? The answer is first in reliability and second in power density. If the delay time is long between the sensing of an overcurrent condition in the power switch and the turn-off of the switch, then the peak and RMS current values reach excessive levels and the switch fails. A well-designed power supply should tolerate a continuous short circuit on any output. To accomplish this with a slow controller IC, extra protection circuitry or an oversized switching transistor and heatsink are required. But that costs money.

Power supply density (often expressed as output power in watts divided by volume in cubic inches) has steadily been increasing over the past 5 to 10 years. By increasing the switching frequency, the size of magnetics and filter capacitors has been reduced, allowing smaller and less expensive power supplies to be built. To increase the switching frequency to the 100- to 500-kHz range and still achieve high reliability requires that the current limit delay time be kept under approximately 100 ns.

The first BiC/DMOS switchmode controller IC to meet these requirements is the Si9110. Its 500-kHz rating for maximum switching frequency is fully usable, thanks to the high-speed current limit comparator and the efficient output driver stage, which essentially eliminates the shoot-through current found in bipolar totem-pole circuits. The DMOS transistor in the input pre-regulator has a breakdown voltage rating of 120 V, which provides ample headroom for operation from typical bus voltages in distributed power systems (where 12, 24, 48, and 60 V are frequently encountered).

The appeal of such distributed power processing systems is in their flexibility and reliability. By bussing power at a higher voltage, smaller conductors can be used, as well as fewer connector pins to get the power to where it is needed-on the circuit card. An on-card power supply can then provide the voltages needed in that part of the system. The power bus voltage is usually chosen to be low enough to eliminate the need for safety agency approvals, and a battery can be connected through a diode to the power bus to provide emergency back-up. The distributed power approach is employed in telecom systems, large minicomputers, and in other applications where reliability is a primary concern.

To illustrate some of the performance capabilities of this BiC/DMOS switchmode controller IC, a 15-W forward converter design is presented. The converter provides +5-V and ±12-V outputs from a 9- to 36-V input range. This permits the power supply to operate from 12-V or 24-V batteries, or from a 28-V aircraft power source. Before describing the forward converter example, it is instructive to review the operation of each of the Si9110 switchmode controller's functional blocks.

FUNCTIONAL DESCRIPTION

Pre-Regulator

A BiC/DMOS power integrated circuit process is used to integrate a high-voltage (120-V rated) lateral DMOS transistor with the CMOS PWM controller. By using an ion implant to shift the gate threshold to a negative value, as shown in Figure 1, the transistor is made to operate as a depletion-mode device. This eliminates the need for a pull-up voltage above V_{IN} to turn the device on, and an amplifier and voltage reference can be used to implement a linear regulator, as shown in Figure 2. The CMOS circuitry is thus protected from transients which appear on the input power bus.

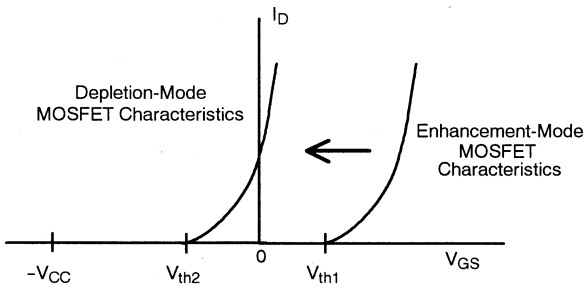


FIGURE 1. Depletion-Mode MOSFET Characteristics

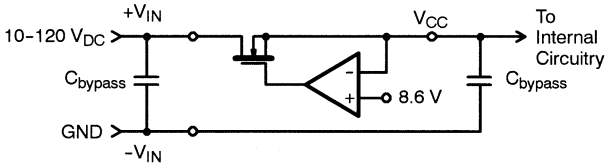


FIGURE 2. Pre-regulator/Start-up Circuit

In some applications it is useful to turn off the pre-regulator after start-up. This is easily accomplished by using an auxiliary winding on the transformer to develop a bootstrap supply voltage. After the converter starts, its own output feeds 10 to 12 V to pin 6 (V_{CC}), and the amplifier pulls the gate of the MOSFET to the $-V_{IN}$ rail. Thus, $V_{GS} = -V_{CC}$, and the device is turned off.

Oscillator

A ring of inverters and internal MOS capacitors forms the oscillator circuit, as shown in Figure 3. This circuit requires only a resistor (no external capacitor) to program the frequency. The internal capacitance is charged towards V_{CC} through R_{OSC}. When the capacitor voltage reaches $V_{CC}/2$, the CMOS logic threshold, inverter INV1 changes state (from high to low), and the INV2 output goes from a low to a high output. The capacitor, C2, provides positive feedback to ensure stable operation without frequency jitter. It also causes the “bump” at the end of the ramp until INV2 can turn on the discharge switch, Q1, to terminate the cycle.

Oscillator synchronization is achieved by prematurely terminating each clock cycle using a positive going pulse capacitively coupled onto the oscillator ramp voltage. The pulse forces INV1 to change states, Q1 discharges C = C1 + C2, and the cycle repeats. An internal flip-flop blanks out the output during every other clock cycle, so the switch duty ratio is limited to a maximum of 50%. Therefore, the oscillator frequency and SYNC pulse repetition rate must be set at two times the switching frequency, f_S.

Error Amplifier

The bias resistor connected from pin 1 (BIAS) to pin 5 ($-V_{IN}$) programs the current sources in the analog portion of the current-mode controller - including the error amplifier, the current-mode and current-limit comparators, and the voltage reference. The Si9110 data sheet guarantees the performance of these functions at one value of bias current - 15 µA. It is possible to change the performance characteristics of these functions by changing the bias current, and Appendix A explains how this is accomplished.

The error amplifier circuit employs PMOS transistors in a differential input stage to achieve a high input impedance of 40 MΩ typically (2 MΩ minimum). This input impedance, combined with a 1-kΩ small-signal output impedance, enables the amplifier to be used with feedback compensation, unlike transconductance error amplifiers. The amplifier can source 2 mA and sink 0.140 mA, as can be seen from the output stage equivalent circuit in Figure 4. Yes, an NPN transistor is used here. Most of the PWM controller is CMOS, but the process allows the flexibility of using bipolar devices where they are advantageous.

The error amplifier is unity gain stable with a typical bandwidth of 1 MHz and 60° phase margin. Bias current values of from 5 µA to 50 µA have been tested, and the error amplifier does remain stable over this range. Actually, the bandwidth and phase margin increase somewhat as I_{BIAS} is increased above 15 µA. Higher bias currents may, therefore, be useful when compensating higher frequency converters (above 250 kHz).

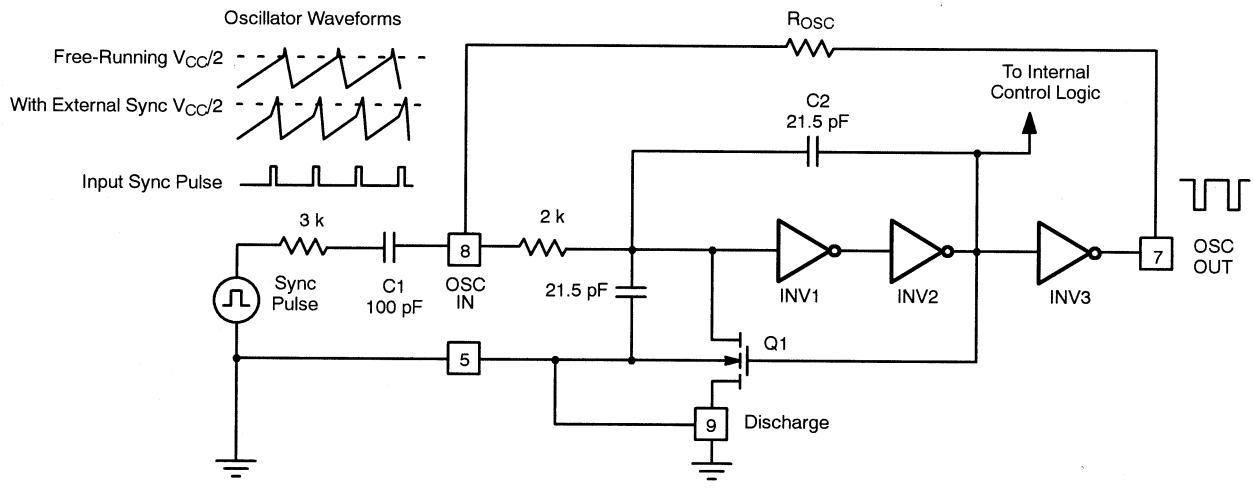


FIGURE 3. Si9110 Oscillator Circuit Operation

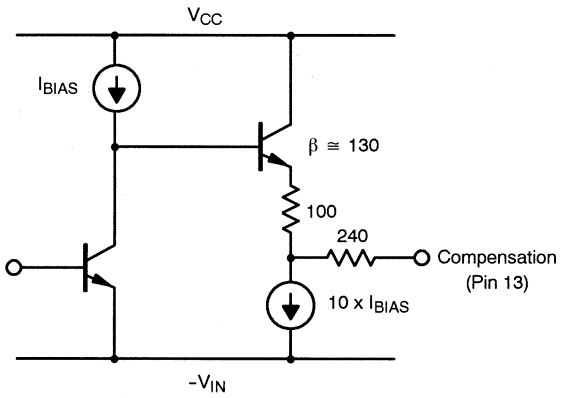


FIGURE 4. Error Amplifier Output Stage

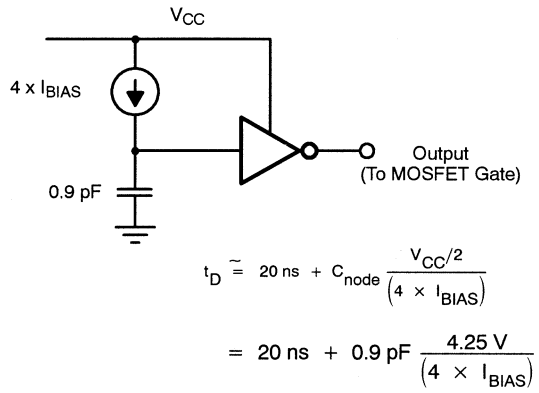


FIGURE 5. Current-limit Comparator Delay (Equivalent Circuit Model)

Voltage Reference

A buried zener with merged temperature compensating diode (patent pending) is used to achieve stability of 0.25 mV/°C.

The Si9110 voltage reference is trimmed to 4 V plus or minus 1% with a bias current of 15 µA. This voltage varies by about 1% as I_{BIAS} is varied from 5 to 50 µA. If 1% reference accuracy must be guaranteed, I_{BIAS} should be set at 15 µA.

For circuits employing an external reference on the secondary side, such as those used with optically coupled feedback, the Si9111 is an economical approach. Its voltage reference provides a dc bias point at the input to the error amplifier where its 10% accuracy is more than sufficient. The reference accuracy is the only difference between the Si9110 and Si9111.

Comparators

The delay time of the current-limit and current-mode comparators can be modeled as a current source charging an internal nodal capacitance, as shown in Figure 5. The current-mode comparator is intentionally made to be four times slower than the current-limit comparator. In many circuits, this permits the elimination of the RC filter in the current-sense circuit, which is used to prevent false trips by the leading edge current spike. After one of the comparator outputs goes high, there is an additional 20 ns of gate propagation delay before the output driver can begin switching.

The total current-limit delay to output versus I_{BIAS} is shown in Figure 6 for V_{CC} equal to 8.5 V. The delay time is 180 ns for I_{BIAS} = 5 µA, but decreases to 50 ns for I_{BIAS} = 30 µA. As operating frequency is increased, I_{BIAS} may be increased to speed up the current limiting and reduce the minimum MOSFET pulse width. As I_{BIAS} is increased, however, the current-limit trip voltage also increases. Figure 7 shows how the trip voltage is established and how it varies with I_{BIAS}. The current sense resistor and I_{BIAS} determine the peak value of switch current. Since this current limiting is very fast, the trip level of current is usually set to be well above the maximum normal operating current (by a factor of 1.5 to 2). This prevents false trips but still protects the MOSFET switch from exceeding its pulse current ratings.

MOSFET Driver

The driver circuit is a CMOS inverter whose typical characteristics are shown in Figure 8. The n-channel (turn-off) peak drive current is about 20% higher than that of the p-channel (turn-on) device. Although the on-resistance ($r_{DS(on)}$) of the output drive is specified, usually the saturation current (where $\Delta I_D/\Delta V_{DS}$ is very small) determines the switching speed. This is due to the vertical load line of capacitive loads. In other words, the MOSFET gate capacitance appears as a short circuit across the driver's output.

The CMOS driver is fast enough to effectively eliminate cross-conduction current during switching transitions, at least when $V_{CC} \leq 10$ V. Above this level, a small amount of cross conduction occurs. Therefore, the greatest gate drive efficiency (approaching 100%) is achieved by keeping $V_{CC} \leq 10$ V, and the gate drive power is given by

$$P_{gate} = Q_g \times f_s \times V_{CC} \quad (1)$$

where

Q_g = MOSFET gate charge
f_s = switching frequency
V_{CC} = supply voltage

Shutdown Logic

The shutdown logic employs an RS flip-flop to disable the output drive. Both the $\overline{\text{SHUTDOWN}}$ and RESET inputs have internal current-source pull-ups (equal to I_{BIAS}), so they can be left open when unused. As long as the $\overline{\text{SHUTDOWN}}$ input is held low, the output is OFF. If the RESET input is hard wired to $-V_{IN}$ (through a normally closed reset button if desired), any LOW input to $\overline{\text{SHUTDOWN}}$ will latch the output in the "off" state. It will remain off until power is recycled (or the reset button is pushed).

Undervoltage Lockout

During start-up, the depletion transistor charges the capacitance connected to the V_{CC} pin with a typical charging current of 18 mA. The output is disabled until V_{CC} reaches the UV lockout voltage (typically 8.1 V). The IC requires less than 0.5 mA of current during this time, since the largest component of supply current is usually for the gate drive (see Appendix B). When V_{CC} reaches 8.1 V, the output is enabled and the MOSFET begins switching. The supply current increases by Q_g x f_s, and V_{CC} charges more slowly until it reaches the pre-regulator voltage (8.5 V). If too much current is drawn from V_{CC}, for instance to supply other circuitry, it may be possible that the converter will be prevented from starting. Or it may oscillate on and off as it starts up, loads down the V_{CC} pin, shuts off, and then repeats this cycle.

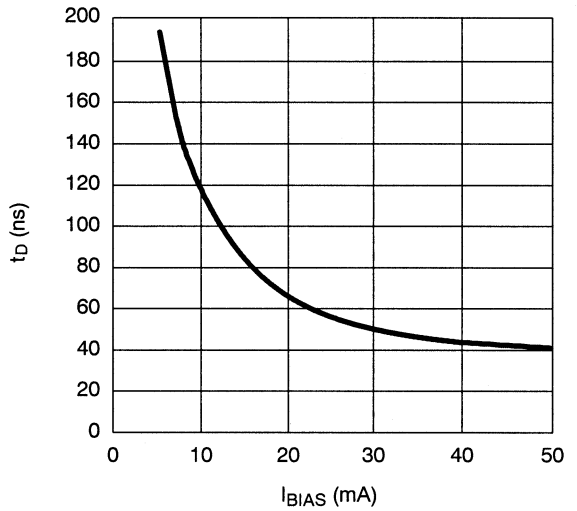


FIGURE 6. Current-Limit Comparator Delay vs. Bias Current

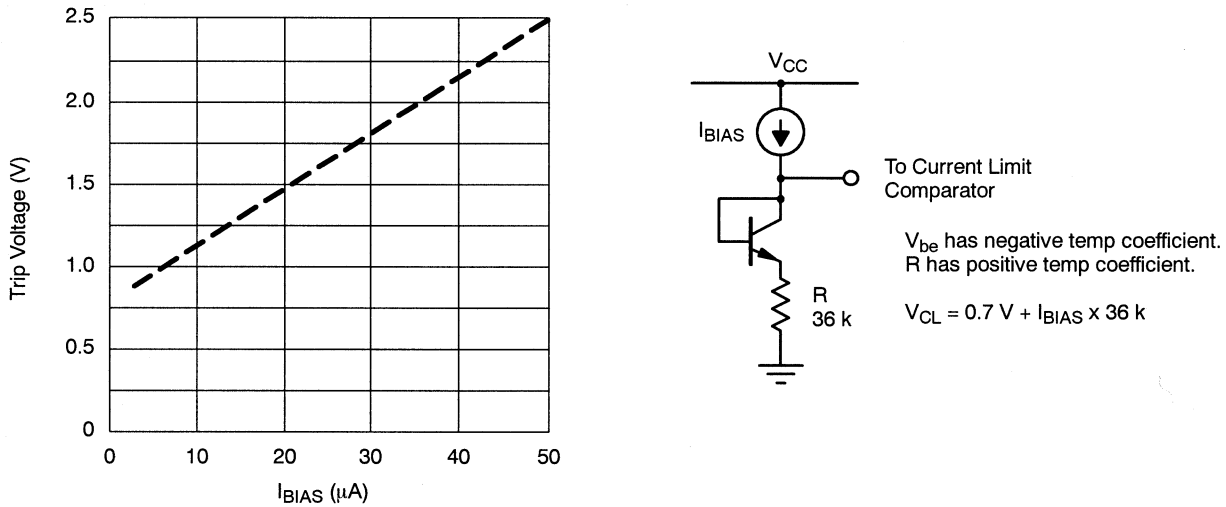


FIGURE 7. Current-Limit Trip Voltage vs. Programmed Bias Current

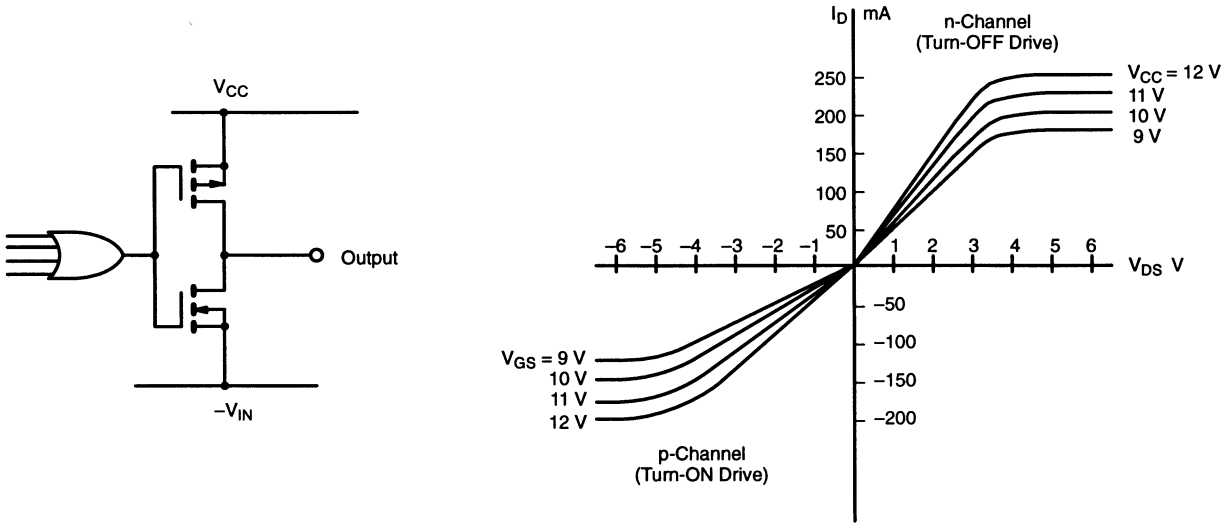


FIGURE 8. Output Drive Characteristics

FORWARD CONVERTER

Specifications

Input Voltage: 9 to 36 V

OUTPUT VOLTAGES				
	Minimum Load (mA)	Maximum Load (A)	Regulation (%)	Ripple (mV_{p-p})
+5	50	1.5	2	150
+12	50	0.310	5	40
-12	20	0.310	5	40

Efficiency:
V_{IN} = 12 V, Full Load: 78% typical, 76% minimum
V_{IN} = 12 V, ½ Load: 82% typical, 80% minimum
Switching Frequency 100 kHz

Circuit Description

The forward converter schematic is shown in Figure 9, and a block diagram of the Si9110/Si9111 controller IC appears in Figure 10 for easy reference. The circuit employs a TL431C voltage reference/amplifier to drive the LED of the opto-isolator, U3. This maintains galvanic isolation between input and output voltages. Since a reference is needed on the secondary side, external to the PWM controller IC, it is not necessary to have a precision reference on the primary side. The voltage reference of the Si9111 is specified at 4 V ±10%, which is accurate enough to establish a dc bias point for the collector current of U3. If galvanic isolation is not required, then the feedback circuitry in the box can be replaced by a voltage divider network, and the input and output grounds must be tied together. In this configuration, the reference accuracy of the PWM controller IC limits the accuracy of the output voltages, and the Si9110 with its 1% reference should be specified. The two ICs are identical in all other respects.

The SMP25N06 switching transistor (Q1) is a 25-A, 60-V MOSFET in a T0-220 package. The breadboard was operated without a heatsink on Q1, even with the power supply output shorted. Three secondaries on the transformer, T1, provide isolated voltages of +5 V and ±12 V. The output inductors are wound on a common core. This reduces the size and cost compared to separate output chokes, as well as improves the response to dynamic loads. The same core size is used for the transformer and the output inductor, the only difference being the air gap required by the inductor to sustain a dc flux. The transformer does not require a gap since the winding, N2, resets the core flux to zero during the “off” time of Q1.

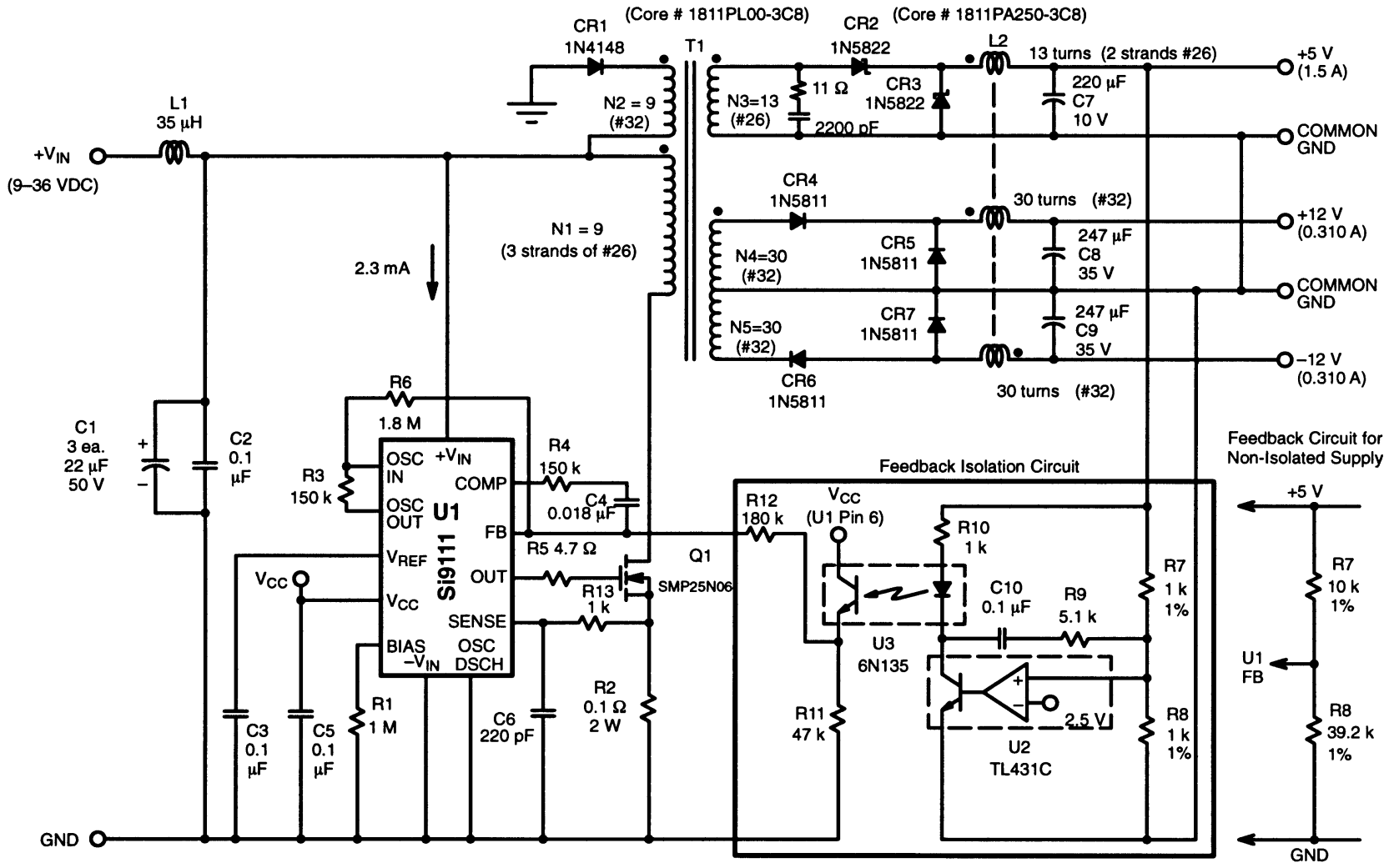


FIGURE 9. Multiple Output Forward Converter

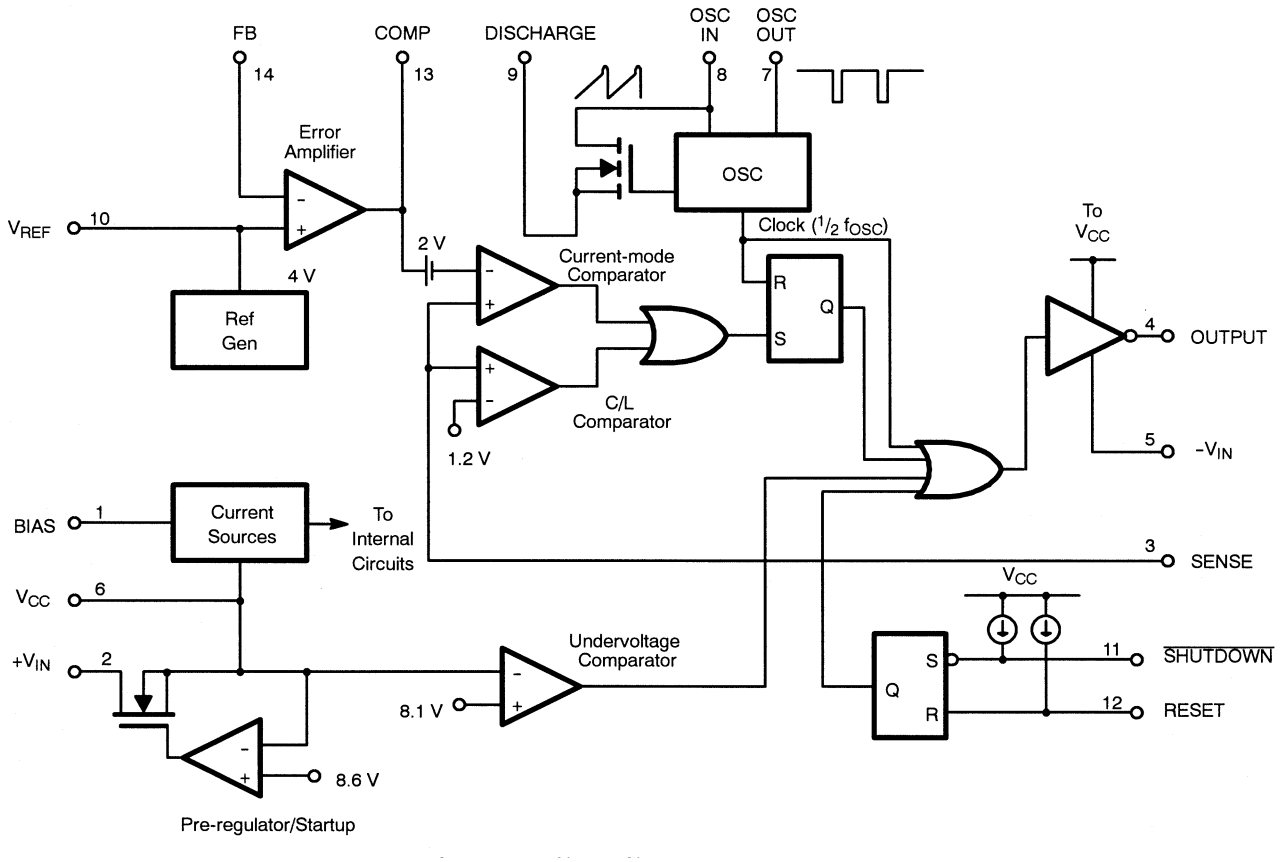


FIGURE 10. Si9110/Si9111 Block Diagram

Forward Converter Principle

The operating principle of forward converters is illustrated in Figure 11. When the switch, Q1, is on, the input voltage is applied across the primary winding, N_P. If, for example, the input voltage minus the voltage drop across Q1 and R2 is equal to 9 V, then 1 V per turn is applied across the primary. Since the same magnetic flux links all of the windings, the volts/turn is constant by Faraday's Law [V = -N(dϕ/dt)].

Therefore, V_{S1} equals 13 V, and V_{S2} and V_{S3} equal 30 V. The LC filter has a cut-off frequency well below the switching frequency, so that the average value of the pulsed secondary voltage appears at the output. For V_1 to equal 5 V, the duty ratio, neglecting diode drops, is given by

$$D = \frac{V_1}{V_{S1}} = \frac{5\ V}{13\ V} = 0.385 \qquad (2)$$

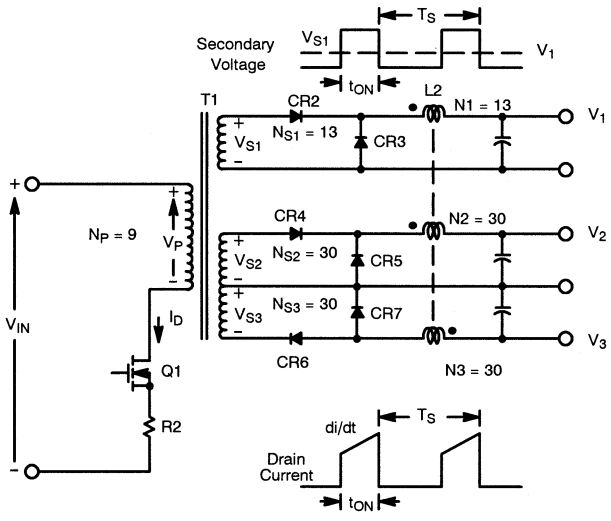


FIGURE 11. Forward Converter Operating Principle

The control loop will force the duty ratio to the value required to make the regulated output equal to 5 V. If the duty ratio equals 0.385, the secondary voltages V_2 and V_3 are given by

$$V_2 = V_3 = V_{S2} \times D = (30)(0.385) = 11.5 \text{ V} \quad (3)$$

This is the ideal case. The diode drops cause the duty ratio to be higher, and V_2 and V_3 are very close to 12 V. (The measured value was 12.1 V.) When Q1 turns off, the free-wheeling diodes CR3, CR5, and CR7 carry the inductor currents. Again, if diode drops are neglected, each output voltage appears across its corresponding inductor winding. Since the volts per turn must be constant on each winding of L2, the number of turns must be proportional to the output voltage. Therefore, the number of turns and the inductance of each winding cannot be arbitrarily assigned as they can be for individual output chokes. The ratio of turns on L2 must be an integer multiple of the T1 secondary windings. In this case, the integer is 1. The amount of inductance is then determined by the core gap, specified as inductance per 1000 turns; 250 mH per 1000 turns was used, giving an inductance for the 5-V inductor as determined from

$$L_{5V} = 250 \text{ mH}\left(\frac{13}{1000}\right)^2 = 42 \text{ µH} \quad (4)$$

Therefore, the current slope during the “on” time of Q1 (referred to the primary side of T1) is given by

$$\frac{di}{dt} = \left(\frac{13}{9}\right)\left(\frac{13 \text{ V} - 5 \text{ V}}{42 \text{ µH}}\right) = 0.275 \text{ A/µS} \quad (5)$$

This current ramp is sensed by R2 to give a voltage ramp input to pin 3 of the Si9111. The current-mode comparator changes states and turns the MOSFET switch off when this sense voltage exceeds the control voltage, V_C, from the output of the error amplifier. Thus, the peak inductor current is controlled on a cycle-by-cycle basis. The same current sense signal is also compared to an internally-generated reference of 1.2 V by the current-limit comparator. This comparator is made four times faster than the current-mode comparator to minimize the delay time required to turn the MOSFET off when an overcurrent condition exists. Such dual-threshold current sensing enables power supply designs that can tolerate shorted outputs for an indefinite period. If the short is removed, then the converter returns to normal operation.

Measured Circuit Performance

Figure 12 shows how the power supply efficiency varies with load. Under the low-line condition (V_{IN} = 9 V), the full load efficiency is 77%. At higher input voltages, the conduction losses in the MOSFET and sense resistor are reduced, permitting full-load efficiency to exceed 80%. High efficiency at light loads is permitted by the CMOS controller’s low supply current. At V_{IN} = 9 V, only 2.3 mA • 9 V = 20.7 mW are required by the Si9111.

The circuit operation at V_{IN}= 18 V with a 80% load is illustrated by the waveforms in Figure 13. The control voltage out of pin 13 is ac-coupled and shown above the current sense voltage. The downward slope of V_C is due to the slope compensation resistor connected between pin 8 and pin 14. Slope compensation is explained below in the section on loop analysis and in References 1 and 2.

When the +5-V output is shorted to ground, the waveforms appear as in Figure 14. The error amplifier output, V_C, goes to the positive rail, so the current-mode comparator would allow the duty ratio to increase to 50%. However, the faster current-limit comparator trips at about 9 A, and the duty ratio is limited to less than 10%.

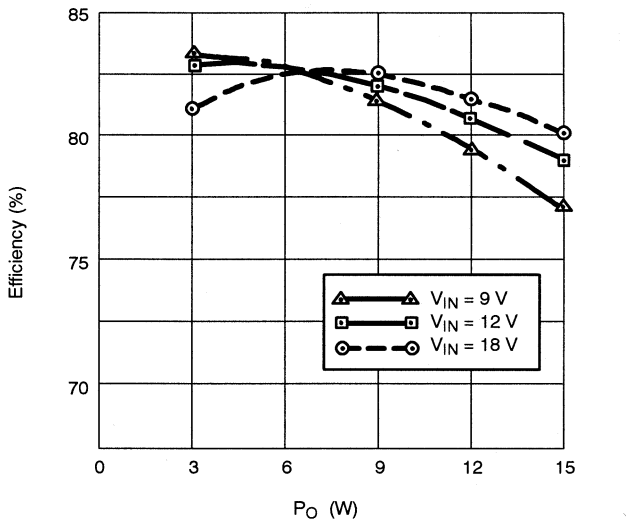
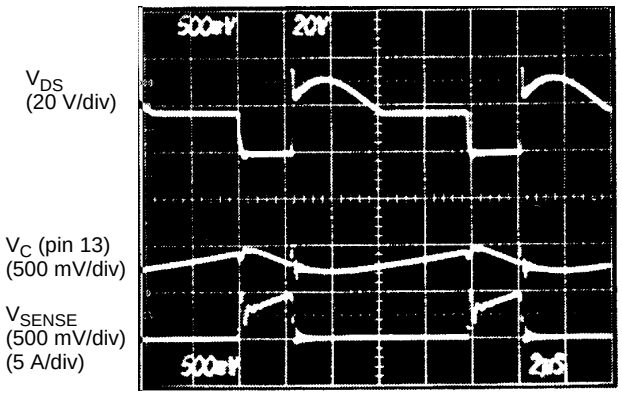


FIGURE 12. Percent Efficiency vs. Load Current



Loads: 1.2 A @ +5 V
0.25 A @ ± 12 V
V_{IN} = 18 V

FIGURE 13. Forward Converter Waveforms

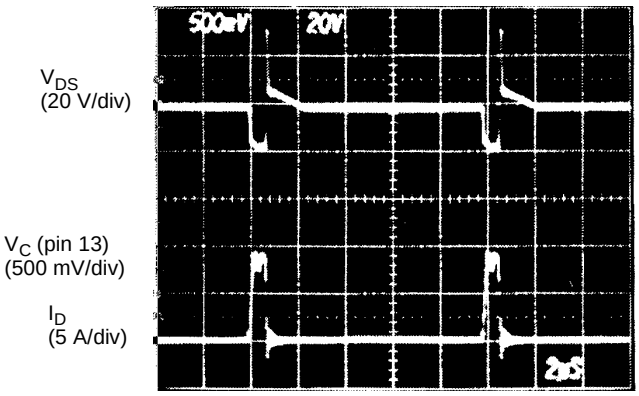


FIGURE 14. Forward Converter Waveforms with +5V Output Shorted to GND (V_{IN} = 18 V)

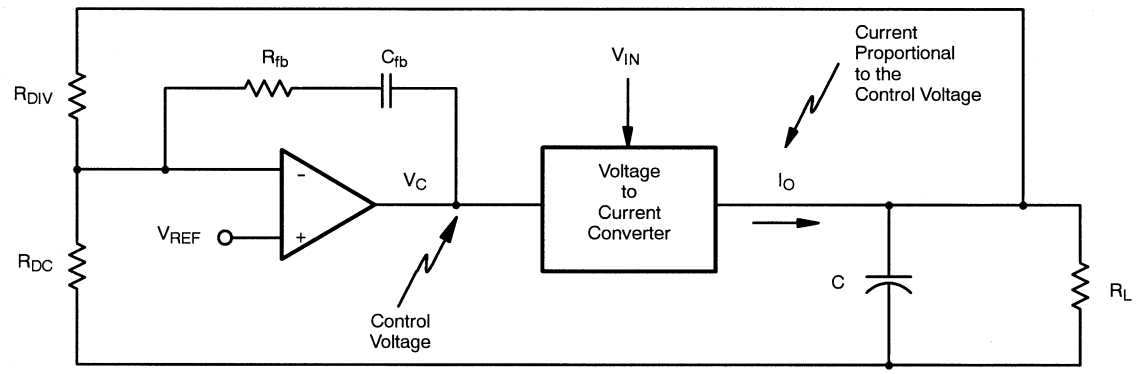


FIGURE 15. Power Converter with Current-mode Control

CONTROL LOOP ANALYSIS

Current-Mode Control

Current-mode control of switching power converters offers several advantages over voltage-mode control. The reliability improvement offered by fast cycle-by-cycle current limiting was discussed above. A second major advantage of current programming is improved dynamic response of the regulator loop while at the same time requiring simpler error amplifier compensation.

The basic objective of current-mode control is to make the power stage behave as a voltage-to-current converter (transconductance amplifier), as shown in Figure 15. To regulate the output voltage, a feedback loop is employed. The control voltage, V_C , is generated by an error amplifier which compares the output voltage to a precision reference, just as in voltage-mode control.

There are several methods for implementing the transconductance power amplifier function-all of them employ an inner current feedback control loop.

The most common method uses a constant frequency clock and peak current sensing, as shown in Figure 16. A clock pulse initiates turn-on of the MOSFET switch, and current ramps up in the output inductor. This current, reflected through the transformer turns ratio, is sensed by the resistor in the MOSFET source to produce a voltage analog of the inductor current. When the voltage ramp reaches the control voltage, V_C, the current-mode comparator sets the latch and turns off the switch. In this way the inner current control loop programs the inductor current in proportion to the control voltage.

To achieve the same loop bandwidth as a current-programmed power converter, a voltage-mode PWM converter requires an error amplifier with compensation as shown in Figure 17.

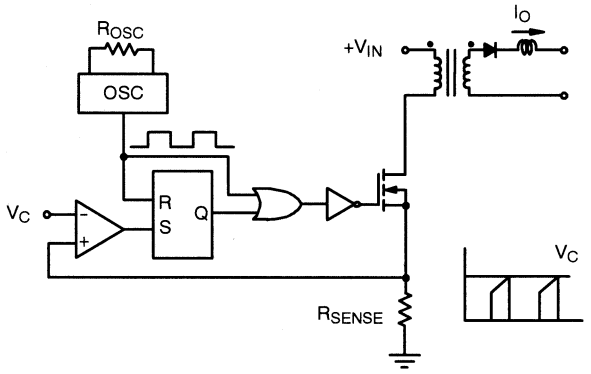


FIGURE 16. Voltage-to-Current Converter

Current-mode control requires fewer compensation components, as shown in Figure 18, and the error amplifier has a simpler transfer function. The simplified compensation is due to the elimination of the double pole of the output LC filter, which must be compensated by the double zero at f_1. If the inner current-programmed loop were perfect, then the inductor would behave as a controlled current source, and the power stage would be a single-pole system. This doesn't happen. What does occur is a splitting of the two poles. One is shifted down in frequency to approximately $f_{p1} = ½\pi R_L C$, which is the dominant low-frequency pole. The second pole in the voltage regulator loop occurs at the unity gain crossover frequency, $\omega_C/2\pi$, of the inner current-control loop. The inner current-control loop has less gain than the voltage loop but has more bandwidth.[1] The wide bandwidth of the current loop enables the power converter to respond more rapidly to step changes in load current, even if the small-signal loop bandwidth is the same. It must be realized that step load changes are large signal perturbations between two different small-signal operating points. With inductor current as a controlled parameter, the wideband current loop changes more rapidly between two operating points of load current. The measured response to a step change in load is given in Figure 19. The switch current and output voltage recover to steady-state within about 50 µs, or five switching cycles. Voltage-mode control generally yields a response which is slower by a factor of 5 to 10.

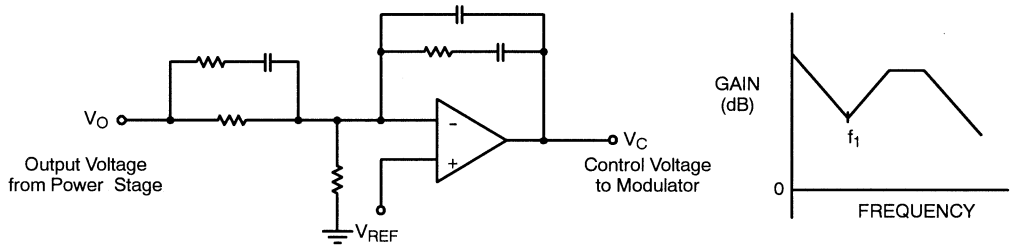


FIGURE 17. Error Amplifier Compensation for Maximum Bandwidth Using Voltage-Mode Control

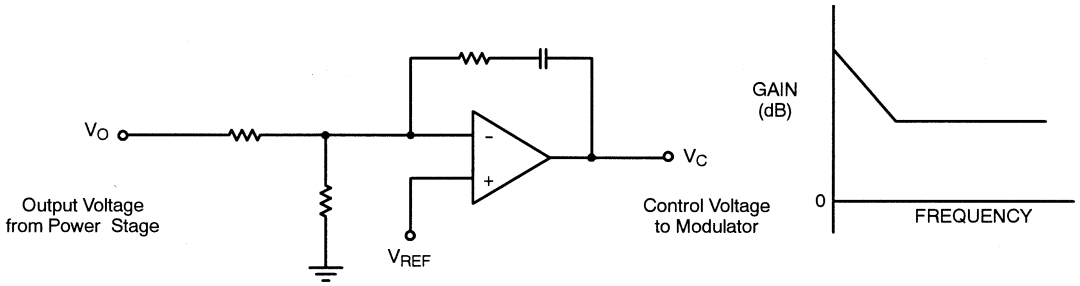


FIGURE 18. Error Amplifier Compensation for Maximum Bandwidth Using Current-Mode Control

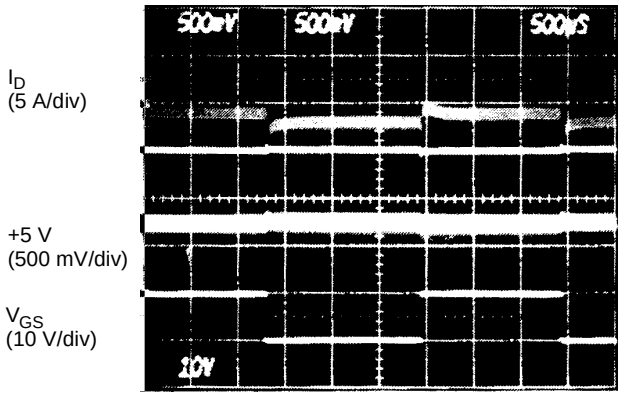


FIGURE 19. Step Load Response

Small-Signal Analysis

A very concise presentation of small-signal analysis of current-mode control loops can be found in Reference 1. In that paper, the Y-parameter model, shown here in Figure 20, is developed for current-programmed power stages since Y-parameters give an output current for a unit of control voltage input. The inner current loop is demonstrated to be stable, as long as slope compensation is employed for D > 0.5, and therefore, the current loop can be absorbed into the new power stage model. This has the advantage of allowing us to analyze the stability of only one (voltage) control loop.

The derivations will not be presented here, but the resulting control-to-output voltage transfer function of the buck regulator is shown in Figure 21. R_{22} is the low frequency value of the inverse of the output admittance, Y_{22}. It is a measure of how effectively current programming makes the power stage behave as a current source and, consequently, depends heavily upon the gain of the inner current loop. More inductance yields higher current loop gain and larger R_{22}. Smaller R_{22} causes the low frequency gain to be diminished, since R_{22} appears in parallel with the load, R_L. R_{22} also decreases the low-frequency pole by the same factor. In this case, R_{2C} is simply the sense resistance value of 0.1 Ω. For buck-derived converters, it is the ratio of voltage at the current-mode comparator input to inductor current, and it accounts for current amplifier gains and current transformer ratios. The second pole at $\omega_C/2\pi$ depends upon the switching frequency, the amount of slope compensation, and the duty ratio at the dc operating point (remember that this is a small-signal analysis of variations around a dc operating point); it does not depend on the load current.

An easy way to work through the calculations is to form a table, as shown in Table 1. The voltage-control loop bandwidth, f_{vc}, and phase margin, ϕ_m, are calculated at full load for three different input voltages. The same symbols are used as in reference 1, with the exceptions that the current ramp slopes m_1, m_2, and m_3 are referenced to the current-mode comparator input. The result is the same as long as the current scale factor, R_f, is taken into account.

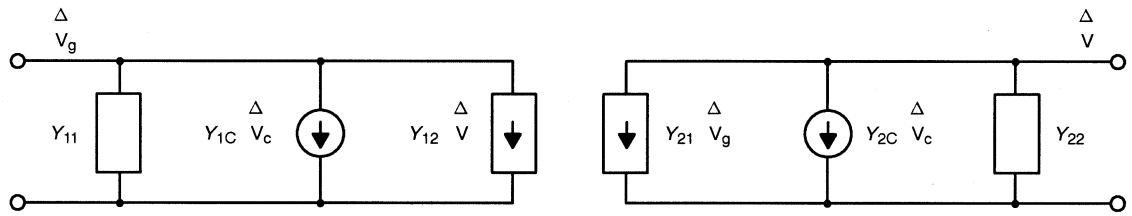


FIGURE 20. Y-parameter Model for Current-mode Regulators

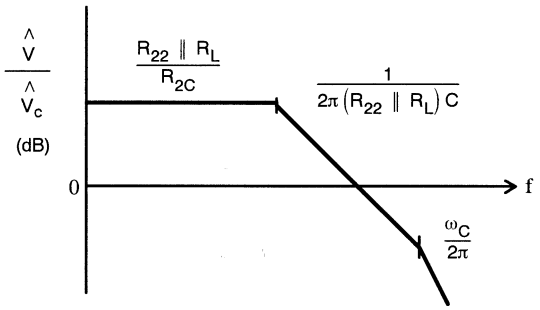


FIGURE 21. Small-signal Control to Output Transfer Function of Current-programmed Buck Regulators

TABLE 1. 15-W Forward-Converter Stability Analysis

V_{IN}	D_i	M_1 (V/µs)	n	R_{2C}	R_{22}	f_p* (Hz)	$A_{cm} = \frac{R_{22} \parallel R_L}{R_{2C}}$	w_C (krad/s)	f_{VC} (kHz)	ϕm (deg)
9	0.59	0.044	1.6	0.1	7.6	144	7.5 (17.5dB)	2 p (33.7)	15.76	52
18	0.78	0.089	1.3	0.1	5.1	147	7.2 (17dB)	2 p (31.4)	15.77	50
32	0.88	0.158	1.16	0.1	4.5	152	7.0 (17dB)	2p (31.2)	15.85	50

$$* f_p = \frac{1}{2\pi(R_{22} \parallel R_L)C}$$

Ramp Slope : $4\, m_C = \frac{V_{CC}/2}{T_S/2} = \frac{R_{fb}}{R_{SLOPE}}$

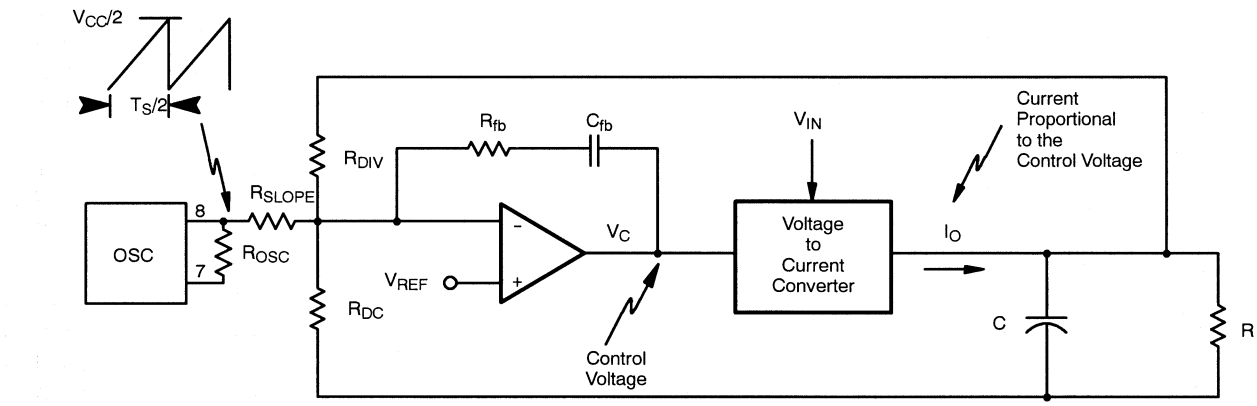


FIGURE 22. Implementation of Slope Compensation Using the Si9110

The forward converter is a transformer-isolated derivative of a buck regulator. Therefore, the Y-parameter model for the buck regulator applies here, but the R, L, and C values used must be reflected through the transformer turns ratios. The resulting circuit parameters are

$$R = \frac{5\ V}{1.5\ A}\left(\frac{9}{13}\right)^2 \Big\| \frac{12\ V}{0.31\ A}\left(\frac{9}{30}\right)^2 \Big\| \frac{12\ V}{0.31\ A}\left(\frac{9}{30}\right)^2 \quad (6)$$

$$= 1.6\ \Omega \| 3.5\ \Omega \| 3.5\ \Omega = 0.83\ \Omega$$

$$L = A_L\left(\frac{N_2}{1000}\right)^2\left(\frac{N_1}{N_2}\right)^2 = 20.3\ \mu H \quad (7)$$

$$C = 220\ \mu F\left(\frac{13}{9}\right)^2 + (47\ \mu F + 47\ \mu F)\left(\frac{30}{9}\right)^2 = 1500\ \mu F \quad (8)$$

Slope compensation is achieved by feeding the oscillator ramp voltage into the inverting input of the error amplifier, as shown in Figure 22.

The amount of slope compensation is given by

$$m_C = \frac{V_{CC}}{T_S} \times \frac{R_{fb}}{R_{SLOPE}} = \frac{8.5\ V}{10\ \mu s} \times \frac{150\ k\Omega}{108\ M\Omega} = 0.071\ V/\mu s \quad (9)$$

This calculation does not take into account the effect of ripple feedback upon slope compensation. For a buck regulator, during the “on” time of the switch, the output ripple voltage is ramping upward due to capacitor ESR. This ramp voltage is amplified and inverted by the error amplifier to provide additional slope compensation. If lower ESR capacitors are used, this effect is diminished. For film or ceramic filter capacitors, the ripple is also phase shifted, since ripple voltage is determined more by C than by ESR.

The slope compensation parameter, n, is given by

$$n = 1 + \frac{2\ m_C}{m_1} \quad (10)$$

where m_1 is the current ramp slope (times the sense resistance) during t_{ON}, which is calculated from

$$m_1 = \frac{V_{IN}}{L} \times R_f = \frac{V_{IN}}{20.3\ \mu H} \times 0.1\ \Omega \quad (11)$$

For a buck converter, R_{2C} is simply equal to R_f, the sense resistance.

The conduction parameter K is a measure of how far into continuous conduction the converter is operating. At full load

$$K = \frac{2L}{RT_S} = \frac{2(20.3\ \mu H)}{(0.83)(10\ \mu s)} = 1.86 \quad (12)$$

This converter operates heavily into the continuous conduction mode and has a fairly high current-loop gain.

The output resistance parameter is

$$R_{22} = \frac{KR}{nD' - D} \quad (13)$$

which varies with both input voltage and load. The frequency, f_P, of the power stage low-frequency pole is

$$f_P = \frac{1}{2\pi(R_{22} \| R_L)C} \quad (14)$$

The low-frequency gain of the power stage is

$$A_{CM} = (R_{22} \| R_L)/R_{2C}$$

and the high-frequency pole is given by $\omega_C = \omega_S/\pi nD'$.

Once the gain of the power stage has been determined and plotted, as shown in Figure 23, the objective is to establish values for the error amplifier compensation to provide good loop bandwidth and phase margin. Some typical “rule-of-thumb” numbers are to use a bandwidth of one sixth to one fifth of the switching frequency and a phase margin of 45° to 60°. A series RC network in the feedback of the error amp gives a pole at the origin and a zero at $f_Z = ½\ \pi\ R_{fb}C_{fb}$.

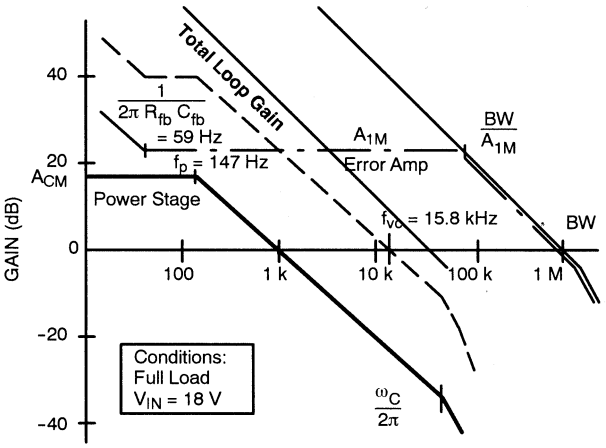


FIGURE 23. Bode Plot of Small-signal Loop Gain

The error amplifier gain remains constant at

$$A_{1M} = \frac{R_{fb}}{R_{div}} = \frac{R_4}{R_7} = \frac{150\ k\Omega}{10\ k\Omega} = 15 (\text{or } 23.5\ dB) \quad (15)$$

between f_Z and the point where the open-loop gain of the error amplifier takes over. This occurs at $A_{OL1} = BW/A_{1M}$, where BW is the error amplifier bandwidth. The gain of the loop is decreased to unity below the poles at $\omega_C/2\pi$, and A_{OL1} , but each can contribute significant phase shift. The voltage loop crossover frequency is calculated from

$$f_{VC} = A_{CM} \times A_{1M} \times f_P \quad (16)$$

The feedback divider resistor, R_7, was first arbitrarily chosen to be 10 kΩ . (This is for the non-isolated configuration. For analysis of the optical-isolator circuit, see Appendix C.) To achieve $f_{VC} \cong f_S /6 = 16$ kHz, A_{1M} was calculated from Equation 15. This requires

$$R_{fb} = A_{1M} \times R_{div} = 15 \times 10\ k\Omega = 150\ k\Omega$$

A standard capacitance value is then chosen such that f_Z falls somewhat below f_P. C_{fb} = 0.018 µF places the zero, f_Z, at about 60 Hz.

The phase margin, ϕ_m, of the ideal current-mode converter is 90°. Phase lags due to poles at $\omega_C/2\pi$ and A_{OL1} diminish the phase margin according to

$$\phi m \cong 90\ \text{deg} - \tan^{-1}\left(\frac{f_{VC}}{\frac{\omega_C}{2\pi}}\right) - \tan^{-1}\left(\frac{f_{VC}}{A_{OL1}}\right) \quad (17)$$

A more accurate analysis should account for the zero of the capacitor ESR. The tantalum capacitors used here (type 550D from Sprague) will cause a zero at approximately 30 to 50 kHz. This will just about cancel the pole at $\omega_C/2\pi$, and increase the phase margin. Higher ESR will cause the extra zero to fall below f_{VC}, and the loop bandwidth will be increased somewhat.

MAGNETICS DESIGN

Transformer Core Selection

The core selection method used here employs the core geometry parameter, K_g, as proposed by McLyman.[3] Pot cores were chosen for both the transformer and the coupled inductor, but another design approach using toroids is recommended for applications requiring either the lower profile or the resilience to thermal shock that toroids provide.

Begin by calculating the output power of the transformer.

$$P_O = \Sigma (V_O + V_D)\ I_O \quad (18)$$

where

V_O ≡ Output Voltage
V_D ≡ Diode Drop
I_O ≡ Output Current

$$P_O = (5\ V + 0.5\ V)(1.5\ A) + 2(12\ V + 0.7\ V)(0.31\ A) = 16.1\ W \quad (19)$$

The apparent power, P_t, for a single-ended forward converter is

$$P_t = P_O\left(\sqrt{\frac{2}{\eta}} + \sqrt{2}\right) \quad (20)$$

where η transformer efficiency

$$P_t = (16.1)\left(\sqrt{\frac{2}{0.99}} + \sqrt{2}\right) = 45.8\ VA \quad (21)$$

The electrical conditions parameter, K_e, is given by

$$K_e = 0.145\ K_e^2 f^2 B_m^2 \times 10^{-4} \quad (22)$$

where

$K_f \equiv$ Waveform Factor ($\sqrt{2}$ for the forward converter)
$f \equiv$ Operating Frequency
$B_m \equiv$ Maximum Flux Density (0.15 tesla was chosen)

$$K_e = 9.145(\sqrt{2})^2(10^5)^2(0.15)^2 \times 10^{-4} = 6525 \quad (23)$$

Finally, the core geometry, K_g, is

$$K_g = \frac{P_t}{2\ K_e \alpha} \quad (24)$$

where $\alpha \equiv$ percent regulation (use 1%)

$$K_g = \frac{45.8}{2(6525)(1)} = 3.5 \times 10^{-3} cm^5 \quad (25)$$

This K_g calculation is based upon an assumed window utilization factor, K_u, of 40% or 0.4. This is difficult to achieve using small pot cores. Assuming a 25% window area, the core geometry is adjusted by

$$K_{g(new)} = (0.4/0.25)\ (3.5 \times 10^{-3}) = 5.6 \times 10^{-3}\ cm^5 \quad (26)$$

The closest pot core is number 1811PL00 from Ferroxcube, for which $K_g = 6.0 \times 10^{-3}$ cm^5.

The toroidal cores which most nearly meet the transformer requirements are numbers T8-16-8 and T10-20-5 from TDK. Their K_g's are 0.007456 cm^5 and 0.007536 cm^5, respectively.

Transformer Winding Design (First Iteration)

Refer to Figure 11 for the nomenclature used here. The number of primary turns is calculated from Faraday's Law, which states that $V = -N(d\phi/dt)$.

$$\frac{V_p}{N_p} = A_C \frac{B_{max}}{t_{ON}} \quad (27)$$

$$N_p = \frac{V_p \times t_{ON}}{B_{max} \times A_C} \quad (28)$$

where

$A_C \equiv$ Cross-sectional Area of Core
$B_{max} \equiv$ Maximum Flux Density
$t_{ON} \equiv$ MOSFET On-time ($t_{ON} = D \times T_S$)

Design for $D_{max} = 0.475$ at $V_{IN} = 9$ V. V_p is calculated from

$$V_p = V_{IN} - I_D \times (r_{DS(on)} + R_{SENSE}) \quad (29)$$

$$I_D \cong \frac{\left(\frac{P_O}{\eta}\right)}{V_{IN} \times D} = \frac{\left(\frac{15\ W}{0.8}\right)}{(9\ V)(0.475)} = 4.4\ A \quad (30)$$

$$V_p = 9 - 4.4(0.08 + 0.10) = 8.2\ V \quad (31)$$

and

$$N_p = \frac{(8.2\ V)(4.75\ \mu s)}{(0.15\ T)(0.433 \times 10^{-4} m^2)} = 6\ turns \quad (32)$$

Calculate the secondary turns as follows:

$$V_O = [(V_p)\ (N_S/N_p) - V_D] \times D \quad (33)$$

If $V_O = V_1 = 5$ V, $D = 0.475$, and $V_p = 8.2$ V, then $N_{S1} = 8.07$. (Assume the diode drop is 0.5 V for Schottky diodes and 0.7 V for fast recovery P-N diodes.)

Eight turns is close enough. Now find the number of turns for the 12-V secondary. During the off-time, the output voltages appear across each coupled inductor winding, which must have the same turns ratios as the transformer secondaries. Therefore,

$$\frac{5\ V + 0.5\ V}{N_{S1}} = \frac{12\ V + 0.7\ V}{N_{S2}} \quad (34)$$

N_{S1} = 8 gives N_{S2} = 18.5 turns; 18 turns give $V_2 \cong 11.65$ V, and 19 turns give $V_2 \cong 12.35$ V. Another option is to set N_{S1} = 16 and N_{S2} = 37. This will more closely achieve the desired turns ratios, but copper losses will be greatly increased. Remember that if the number of turns is doubled, then the copper cross section must be halved. Resistance, and copper losses, increase by a factor of four. If it doesn't matter that the 12-V output is off a bit, then use N_p = 6, N_{S1} = 8, and N_{S2} = 19.

Inductor Core Selection

The power handling capability of the core is independent of the number of windings used. The simplest approach is to refer all outputs to the 5-V winding and assume that

$$I_O = P_O/V_O = 15\ W/5\ V = 3\ A \quad (35)$$

To operate well into continuous conduction choose $K = 2L/RT_S \geq 4$.

Therefore, $L \geq (4/2)(5\ V/3\ A)10^{-5} = 33\ \mu H$.

This is a ball park number; 25 µH is acceptable, and so is 50 µH. However, if L is larger, a larger core is required for the same core losses.

The peak inductor current, at maximum load, is

$$I = I_{O(max)} + \frac{DI}{2} \quad (36)$$

ΔI is approximately given by

$$\frac{V_1 + V_D}{L_{S1}} = \frac{\Delta I}{t_{OFF}} \quad (37)$$

and the maximum ΔI occurs at maximum V_{IN} where $D \cong 0.11$, $t_{OFF} = (1 - D)10\ \mu s = 8.9\ \mu s$.

$$\frac{5\ V + 0.5\ V}{33\ \mu H} = \frac{\Delta I}{8.9\ \mu s} \quad (38)$$

The inductor energy storage requirement is

$$E = ½\ (LI^2) = ½\ (33\ \mu H)(3.75)^2 = 232\ \mu J \quad (40)$$

The electrical conditions are

$$K_e = 0.145\ (P_O)\ (B_m)^2\ 10^{-4} \quad (41)$$
$$= 0.145\ (15)\ (0.3)^2\ 10^{-4} = 19.6 \times 10^{-6}$$

The core geometry requirement is

$$K_g = \frac{(E)^2}{K_e \alpha} = \frac{(232\ \mu J)^2}{(19.6 \times 10^{-6})(1)} = 0.00275\ cm^5 \quad (42)$$

for 1% regulation. Adjust this for a 25% window utilization, and you get

$$K_g = \frac{0.4}{0.25}(0.00275) = 4.4 \times 10^{-3} cm^5 \quad (43)$$

We can use an 1811 pot core with a standard A_L value (160, 250, or 400 mH/10^3). For a toroid, use a number 55206 molypermalloy powder core, for which K_g = 0.007274 cm^5. The pot core was chosen here.

Inductor Winding Design

The transformer design was left with N_{S1} = 8 and N_{S2} = 19, which causes the 12-V output to be about 12.35 V. If A_L = 400 mH/1000 turns is used,

$$L_{S1} = (8/1000)^2\ (0.4) = 25.6\ \mu H \quad (44)$$

This gives

$$K = \frac{2L}{RT_S} = \frac{2(25.6 \mu H)}{(1.67)(10^{-5})} = 3.1 \quad (45)$$

which is still well into continuous conduction ($K_{crit} = D' = 1 - D$ for buck converters).

It could be done this way, but to make the 12-V output come out closer to 12 V, try some other turns ratios. N_{S1} = 13 and N_{S2} = 30 gives:

$$V_2 = (5.5/13)30 - 0.7 = 11.99\ V \quad (46)$$
$$A_L = 250\ mH/1000\ turns\ gives$$
$$L_{S1} = (13/1000)^2\ (0.25) = 42\ \mu H \quad (47)$$

The maximum flux density is found from

$$L = \frac{\lambda}{I} = \frac{N\phi}{I} = \frac{NB_mA_C}{I} \quad (48)$$

$$Bm = \frac{LI}{NA_C} = \frac{(42\ \mu H)(3.75\ A)}{(13)(0.433 \times 10^{-4})} = 0.28\ T \quad (49)$$

Saturation occurs above 0.3 T = 3000 gauss, so this flux level is acceptable. Apportion the window area according to the output power of each winding. Total copper area is 0.25 W_A, where W_A = 0.285 cm^2 is the total window area. The copper cross section for the 5-V winding is

$$A_{CU} = \frac{(0.25)(0.285 cm^2)}{30\ turns} \times \frac{(5\ V)(1.5\ A)}{15\ W} = 2.74 \times 10^{-3} cm^2 \quad (50)$$

Use two strands of AWG26 magnet wire, for which the copper area is

$$A_W = (2)\ (1.28 \times 10^{-3}\ cm^2) = (2.56 \times 10^{-3}\ cm^2) \quad (51)$$

for the 12-V winding,

$$A_{CU} = \frac{(0.25)(0.285 cm^2)}{30\ turns} \times \frac{(12\ V)(0.31\ A)}{15\ W} = 0.59 \times 10^{-3} cm^2 \quad (52)$$

Use one strand of AWG30, for which $A_W = 0.507 \times 10^{-3}\ cm^2$.

Transformer Winding Design (Revisited)

As shown in the above analysis, the transformer and inductor designs are interdependent when coupled inductors are used. Calculations are made based upon some reasonable assumptions, and the results may not give the desired outcome (such as a fractional turn or a saturated core). Then choices must be made which are consistent with the requirements of the end application. The choice made here was to set the output voltages as close as possible to 5 and ±12 V.

The transformer secondary turns are $N_{S1} = 13$ and $N_{S2} = 30$. The primary turns are found from

$$V_S = V_O/D + V_D = V_p\ (N_S/N_p) \quad (53)$$

$$V_s = \frac{5\ V}{0.475} + 0.5 = 11\ V = 8.2\ V\left(\frac{13}{N_p}\right) \quad (54)$$

$$N_p = 9.67\ turns$$

Set $N_p = 9$ turns so that the converter will continue to regulate down to $V_{IN} = 9$ V. Again, apportioning the copper according to power level (and equally split between primary and secondary) gives the following winding configuration.

Winding	Turns	Wire Size
Primary	9	3 Strands AWG26
RESET	9	1 Strand AWG32
+ 5 V	13	1 Strand AWG26
+12 V	30	1 Strand AWG32
-12 V	30	1 Strand AWG32

The primary and RESET windings were wound together (multifilar) over the bobbin, followed by the 5-V output. The ±12-V windings were wound bifilar over the 5-V winding.

Prototyping Hints

A schematic and a parts list do not provide sufficient information to enable a CAD operator to lay out a switching power supply. Parasitic inductances and capacitances, which do not appear on the schematic, can cause major differences in performance. The number of layout iterations can be reduced (down to one with experience) if the following guidelines are followed.

1. Use a ground plane. However, do not assume that the ground plane impedance is zero so that you can ignore the need for good component placement. Every component cannot be placed near every other component. Know which components should be grouped closely together and when close proximity is unnecessary.
2. Keep loop areas small where the current changes rapidly. Loop inductance is proportional to loop area. Inductive voltage spikes are proportional to inductance, i.e, V = Ldi/dt. For example, the loop from C1, through the T1 primary, Q1, R2, and back to the bottom end of C1 carries a current which undergoes a high rate of change. Reducing this loop area reduces noise on the input power lines. Other examples are the loops defined by each secondary winding and the corresponding output rectifiers. Cross regulation of the ±12-V outputs is worsened by the inductance of these loops. Conversely, the inductance of the loop defined by CR3, L2, and C7 is not critical. The parasitic inductance in series with an inductor is of little consequence.
3. Keep noise-sensitive nodes away from noise generators. The drain voltage of Q1 changes rapidly. If the trace between T1 (primary) and Q1 (drain) runs adjacent to the feedback input (pin 14) of U1, then noise is capacitively coupled into the feedback. The noise current is proportional to the parasitic capacitance by i = Cdv/dt. Injected noise currents are worse when the driving point impedance is high. Pins 1, 13, and 14 of the switchmode controller are such high-impedance nodes. Too much noise injection causes a random instability in the control loop.

Following these guidelines reduces headaches as well as costly design time. Using BiC/DMOS PWM controllers reduces component count and failure rates of dc/dc converters in distributed power systems.

References

1. Middlebrook, R.D., “Topics in Multiple-Loop Regulators and Current-Mode Programming,” IEEE Power Electronics Specialists Conference, 985 Record, pp. 716-732 (IEEE Publication 85CH2117-0).
2. Hsu, et al., “Modelling and Analysis of Switching DC-to-DC Converters in Constant-Frequency Current-Programmed Mode,” IEEE Power Electronics Specialist Conference, 1979 Record, pp. 284-301, (IEEE Publication 79CH1461-3 AES).
3. McLyman, Col. W. T., “Magnetic Core Selection for Transformers and Inductors,” Marcel Dekker,1982.

APPENDIX A

Proper operation of the Si9110 requires that a programming resistor, R_{BIAS}, be connected from pin 1 to $-V_{IN}$, which is assumed here to be ground. This resistor programs internal current sources in the analog portion of the control circuitry. The value of the bias current depends upon two parameters, V_{CC} and R_{BIAS}, as shown in the circuit provided in Figure 24. The characteristic curve of the PMOS FET follows the familiar square law (I_D is proportional to V_{GS} squared). However, over the region of interest, between 5 µA and 50 µA, the curve can closely be approximated by a straight line, as shown in Figure 25. This line is defined by its slope (50 kΩ) and its point of intersection with the X-axis (3.5 V). The intersection of this curve with the load line defined by V_{CC} and R_{BIAS} determines the value of I_{BIAS}. The load line in Figure 25 identifies the conditions which are specified in the data sheet. When V_{CC} = 10 V and R_{BIAS} = 390 kΩ , I_{BIAS} = 15 µA.

If the pre-regulator is used continuously, as in the forward converter example above, then V_{CC} has a nominal value of 8.5 V. The 1-MΩ bias resistor gives I_{BIAS} = 5 µA. This is the lowest value recommended. On the high end, not much performance improvement in terms of comparator speed is obtained for I_{BIAS} above 30 µA (see Figure 6).

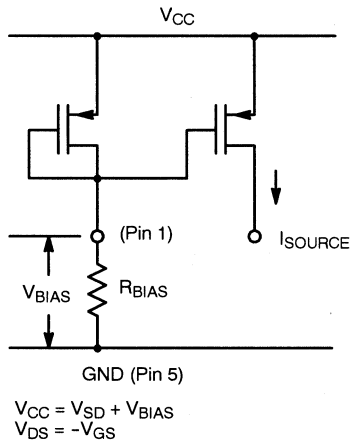


FIGURE 24. Internal Current Source Programming

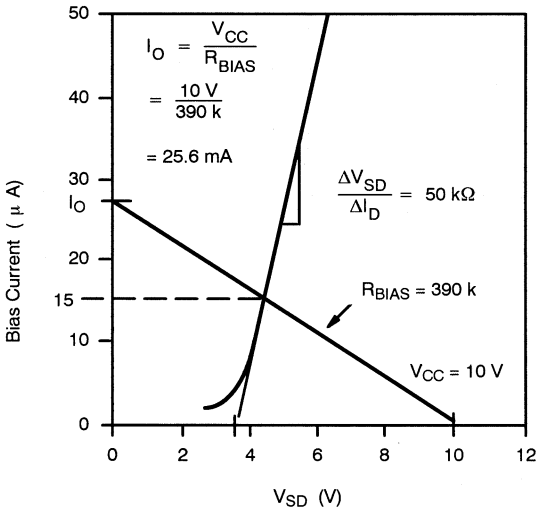


FIGURE 25. Programmable Current Regulator Characteristics

APPENDIX B

The supply current requirements of PWM controller ICs are specified at one operating frequency, with no load being driven. In many cases, it may be useful for the circuit designer to determine the supply current requirements needed to drive a specific MOSFET at a given frequency. The Si9110 has been well characterized in this regard.

Equation 1 provides a quick calculation of the supply current drawn by the Si9110.

$$I_{CC} = 60\ \mu A + \left[1.5\ \mu A \frac{f_S}{1000}\right] + [30 \times I_{BIAS}] + [Q_g \times f_S] \qquad (1)$$

Each of the components has a straightforward explanation.

a. The voltage reference requires a constant current which is neither frequency nor load dependent. It has a typical value of 60 µA.

b. CMOS circuitry only uses power when a change in logic state occurs. Therefore, the quiescent current requirements of the oscillator and logic gates is proportional to the switching frequency. The proportionality constant is typically 1.5 µA per kHz.

c. The analog circuitry (error amplifier and comparators) utilizes constant-current sources which are programmed by the bias resistor connected from pin 1 to ground. Setting R_{BIAS} equal to 390 kΩ and V_{CC} = 10 V programs the bias current at 15 µA. At this current, the internally generated voltage reference levels (for undervoltage lockout, V_{REF}, and V_{CL}) have the best compensation over temperature. This is also the value at which the data sheet parameters are guaranteed.

d. The output drive current is typically the largest component of I_{CC}. The drive stage has been designed to minimize shoot-through current of the output inverter. Thus, the current requirement can be calculated as $I_{gate} = C_L V_{CC} f_S$. A MOSFET gate is a capacitive load, but a non-linear one. Therefore, MOSFET manufacturers specify the total gate charge required to turn a MOSFET on. In this case, $I_{CC} = Q_{g(on)} \times f_S$, where fs is the switching frequency.

For the forward converter example, the supply current should be

Voltage reference = 60 µA

Oscillator and logic = (1.5 µA)/kHz x 100 kHz = 150 µA

Analog circuitry = 30 x 5 µA = 150 µA

Gate drive 15 nC x 100 kHz = 1500 µA

Total supply current = 1860 µA

The measured value was 2.1 mA.

APPENDIX C

The gain of the error amplifier plus the feedback isolation circuit is

$$A_V = \left(\frac{R_9}{R_7}\right)(CTR)\left(\frac{R_{11}}{R_{10}}\right)\left(\frac{R_4}{R_{12}}\right)$$
$$= \left(\frac{5.1\ k\Omega}{1\ k\Omega}\right)(0.07)\left(\frac{47\ k\Omega}{1\ k\Omega}\right)\left(\frac{150\ k\Omega}{180\ k\Omega}\right) = 14$$

which is approximately equal to the gain of the non-isolated feedback circuit analyzed above.

The TL431C has a voltage reference with 2% accuracy equal to 2.5 V. R_7 and R_8 were both chosen to be 1 kΩ to establish a dc current much greater than the input bias current of U2, which is 4 µA. C_{10} causes the amplifier of U2 to behave as an integrator with a high dc gain, thus ensuring the accuracy of the output voltage. R_9 causes the gain of U2 to remain constant at R_9/R_7 above the crossover frequency, $1/(2\pi R_9 C_{10})$.

The minimum current transfer ratio (CTR) of U3 is 0.07. CTR is defined as the ratio of output current to anode current for the optical isolator. The small-signal variation of the LED current is equal to the output voltage of U2 divided by R_{10}. The output voltage of U3 is equal to the output current of U3 times R_{11}. Therefore, the gain from the output of U2 to the output of U3 is given by $CTR(R_{11}/R_{10})$. R_{11} was chosen to establish a dc operating current for U3 given approximately by

$$\frac{V_{REF}}{R_{11}} = \frac{4\ V}{47\ k\Omega} = 85\ \mu A$$

Likewise, R_{10} establishes the dc operating point for the LED at approximately 1 mA. R_9 and R_{12} are chosen last to achieve the desired overall gain.