

## **Design Considerations for a Two Transistor, Current Mode Forward Converter**

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This application note describes the design of a 150 W, 150 kHz, two transistor, current mode forward converter. Topics emphasized are those most often of greatest importance to designers — noise control, feedback circuit analysis, and magnetics design. Improved Schottky rectifiers, power MOSFETs and optocouplers are presented, and their effects on switched mode power supply design are also discussed.

### **INTRODUCTION**

Efforts to improve power supplies currently are focused on increasing efficiency, decreasing size, and improving reliability. Reducing system losses is a way to make progress in all three areas, so it is a good direction to take. Other ways to meet these goals are: improve the overall design, use more efficient components, increase switching frequency to reduce the size of the energy storage elements, use the most reliable components available, or decrease volume by using new packaging techniques such as employing surface mount devices.

The use of components which have been designed specifically for switched mode power supplies (SMPSs) is another tool the designer has to attain the above goals. Device manufacturers can manage device tradeoffs to give the best solution for an application. Since selecting the most appropriate devices is one of the major jobs of a power supply designer, some of these newer devices are discussed here along with the design of a 150 kHz, 150 W, current mode, two transistor forward converter.

The power supply described here operates from an input voltage of 90 to 132 VAC or 180 to 264 VAC (with jumper selection), generates a 5 V output at 30 A, and has a line and load regulation of 0.2%. Hold up time is a minimum of 50 ms, and efficiency is 75 to 81%, depending on operating conditions.

### **ADVANTAGES OF THE TWO TRANSISTOR, CURRENT MODE FORWARD CONVERTER**

More than any other factor, desired output power has a great effect on selecting a topology. The single transistor flyback converter is nearly an uncontested choice for off-line converters delivering less than 150 W. It is inexpensive since

the transformer itself (actually a coupled inductor) serves as part of the output filter for all outputs. Generating auxiliary outputs merely requires the addition of another secondary winding on the power transformer, a diode, and an output filter capacitor. At power levels greater than 150 W, however, the peak currents in the primary switch begin to get out of hand, especially for power transistors that must block the high voltages typically seen in flyback converters.

A major advantage of the two transistor forward converter is that the power transistors need to block only the supply voltage instead of two or more times the supply voltage as they must in a flyback or single transistor forward converter. Easing the voltage requirement from 1000 V to 500 V is an especially significant benefit for a power MOSFET since the MOSFET's on-resistance increases exponentially with breakdown voltage.

The half bridge topology competes directly with the two transistor forward converter since it is commonly used in 150 to 500 W converters. The advantage of the half bridge is that it transfers energy using the transformer core in the first and the third quadrant of its B-H curve, whereas the forward converter uses only the first quadrant to deliver energy. In spite of this advantage, designers sometimes favor the forward converter since it does not require the center tapped secondary and extra output rectifier that the half bridge must have.

Current mode operation is rightfully a popular control method. The two state variables in the control of a converter are the voltage across the output filter capacitor and the current in the output filter inductor. A current mode converter uses both state variables to maintain the output voltage, whereas the voltage mode converter uses only the output voltage. The additional information gives the current mode converter the following performance advantages:

- 1) Cycle by cycle current limiting (which greatly simplifies overload and short circuit protection)
- 2) Inherently good line regulation (pulse width automatically increases with a lower line voltage)
- 3) Improved response time (inner current loop responds rapidly to changes in load)
- 4) Inherently more stable (although the control loop analysis is considerably more complicated)



## FUNDAMENTAL DESIGN EQUATIONS

After settling on a topology and operating mode, the next step is to calculate the lowest DC bus voltage from which the converter must operate. At low line (80% of 220 VAC) the RMS line voltage is 180 V, and the peak DC bus voltage is  $1.41 \times 180$  V, or 254 V. It is common to decrease this figure by 15% for a guardband and subtract another 10 to 20 V for ripple on the DC bus. The final figure is in the 200 V range.

The next task is to determine the shape and magnitude of the power transistor current. From the desired output power, maximum allowable duty cycle of 45%, minimum DC bus voltage, and an anticipated efficiency of 75%, the primary current under full load is calculated as follows:

$$I_P = \frac{P_{out}}{\delta_{max} \eta V_{in}} \quad \text{or}$$

$$I_P = \frac{150 \text{ W}}{(.45)(.75) \times 200 \text{ V}} = 2.22 \text{ A}$$

The figure above represents average current during the transistor's on time. The average current during an entire cycle is equal to 2.22 A times the maximum duty cycle, or 1.0 A. The shape of the current waveform determines its RMS value and the size of the output transistor.

The waveforms of Figure 1 show that when the power transistors are on, their currents are a replica of the output inductor current. The only differences are that the currents are scaled according to the transformer turns ratio, current in the power transistor during its off time is zero, and the power transistors also carry magnetization current, which does not appear at the secondary.

Converters are classified as operating in the "continuous" or "discontinuous" mode, referring to the current in the output

filter inductor. If the converter operates in the discontinuous mode, the output inductor current decays to zero each cycle and the resulting power transistor waveform is triangular. From a peak current of two times the average of 2.22 A ( $a = 4.44$  A), an RMS current of 1.72 A is computed from the formula for a triangular shaped waveform:

$$I_{RMS} = a \sqrt{\frac{\delta_{max}}{3}}$$

From Figure 1 we can see that if the supply operates in the continuous mode, the power transistor's current is trapezoidal, and peak and RMS currents are a function of the output filter inductance. A larger coil gives lower ripple and RMS heating. Lowering inductor ripple current has the added benefit of easing the requirements on the output filter capacitor. This advantage can be oversold easily, however. In the end specifications regarding the supply's response to step changes in load usually determine the number and size of the output capacitors.

The trade off in decreasing ripple current to very small values is that the control circuit in a current mode controller senses the ripple and uses it as part of the control algorithm. A shallow slope makes the circuit susceptible to noise, so a suggested lower limit of ripple is about 20% of the full load current. Because of potential noise sensitivity, the method chosen to sense current becomes important. In this example, using a sense resistor in the MOSFET's source is difficult since inexpensive, low inductance resistors are hard to find. Ways to improve noise immunity at higher power levels include viewing the inductor current with a current sense transformer or a current sense winding on the inductor.

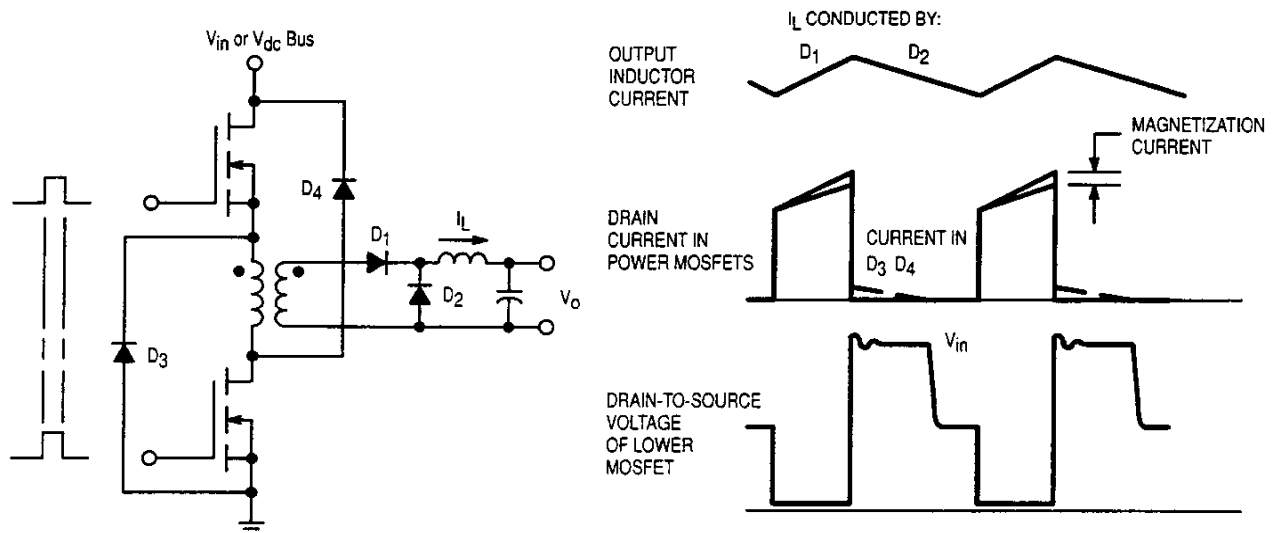


Figure 1. Basic Circuit and Operation of the Two Transistor Forward Converter Operating in the Continuous Conduction Mode

From the formula below for the RMS value of a trapezoidal waveform, we can calculate full load RMS current. With a 2.22 A average current and a .4 A ripple (allotted 6 A inductor ripple current divided by the anticipated 1:15 transformer turns ratio), the  $I_{RMS}$  value can be calculated from:

$$I_{RMS} = \delta_{max} \sqrt{\frac{a^2 + ab + b^2}{3}}$$

where  $a = 2.02$  and  $b = 2.42$  A. The result is only slightly larger than the 1 A average current calculated above.

The previous calculations have ignored the magnetization current, which is calculated from the formula:

$$I_{mag} = \frac{V_{in} t_{on}}{L_p}$$

In this case  $I_{mag}$  is small enough to ignore in sizing the power transistors. Nevertheless, knowing the value of  $I_{mag}$  is helpful since it affects the core's flux density in addition to the primary current. In this supply the magnetizing current is always less than 100 mA due to the power transistor's limited on-time and the large primary inductance (6.67 mH).

From the above calculations we can now size the power transistor and estimate its on-state losses. The MTP4N50E is a good choice. It is a 4 A, 500 V MOSFET with an on resistance of  $1.5 \Omega$  at  $25^\circ\text{C}$ . Typical on-resistance is  $1.8 \Omega$  at  $100^\circ\text{C}$ , so expected on-state losses are about 1.8 W for each of the two transistors.

The MTP4N50E is a good choice for another reason. Its design includes two features to minimize drain-to-gate capacitance, which is the prime determinant of switching

speeds. One feature is specifically targeted at minimizing that component of  $C_{rSS}$  that extends the turn-off delay time. This increases the effectiveness of cycle by cycle current limiting common in current mode applications by decreasing the delay between detecting an overcurrent condition and shutting the transistor off. Turn-off delay of the MTP4N50E is roughly 30% less than that of a standard power MOSFET with similar current and voltage ratings. The second feature decreases overall  $C_{rSS}$  and therefore reduces drain-to-source voltage transition times.

## CONTROL IC

The choice of the control IC is so important that it is worth taking plenty of time to select the one that best matches the system's requirements. The UC3844 (manufactured by Motorola and others) is a good match for a medium range power, off-line, current mode converter. Its features include:

1. Current mode operation to 500 kHz
2. Output deadtime adjustable from 50 to 70%
3. Latching PWM for cycle-by-cycle current limiting
4. Internally trimmed reference with undervoltage lockout
5. Single high current totem pole output
6. Low start-up and operating current
7. 8-pin DIP package

The UC3844 and the UC3845 are identical except that the UC3844's 16 V start up threshold makes it the better choice for off line applications. Figure 2 shows the UC3844's detailed block diagram. Once the topology and operating mode are set, designing the power transformer is the next major step.

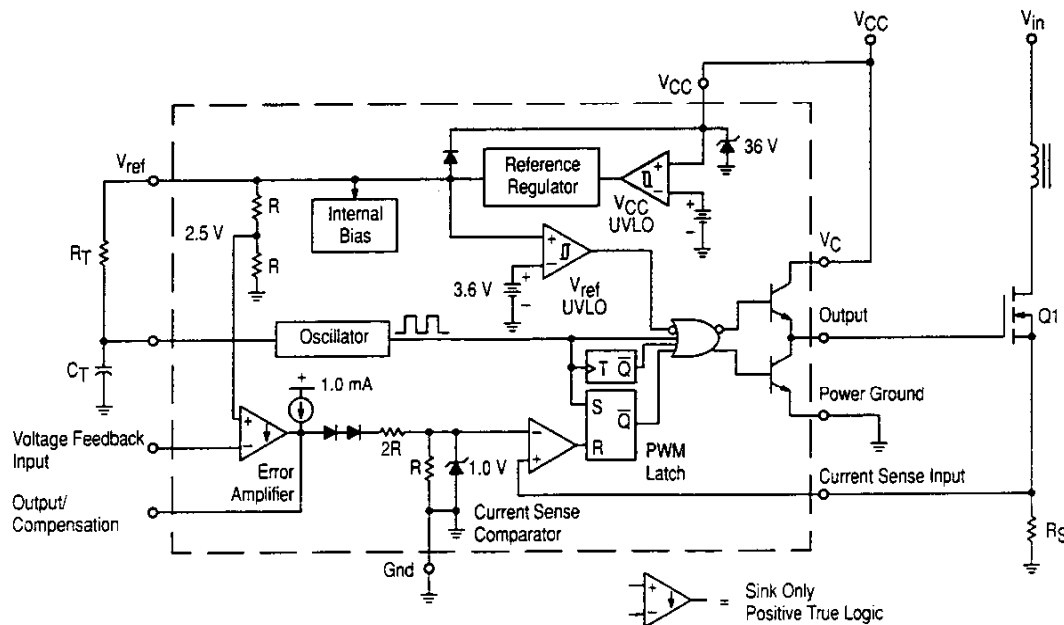


Figure 2. Block Diagram of Motorola's UC3844

## POWER TRANSFORMER DESIGN

Every design engineer seems to have his or her unique way of tackling power transformer design. Factors to consider are core and winding losses, thermal impedance, desired efficiency, core saturation, mechanical dimensions, input/output isolation, core shape and size, the bobbin's winding area and shape, number and location of output pins, the core's ability to contain the magnetic flux, and of course cost. Units of Maxwells, Gauss, Oersteds, and Teslas complicate things further. Another complication is that application information is either lacking or is based on a particular manufacturer's method of specifying their magnetics. A suggested design approach is to select a core and bobbin family that will meet the system's mechanical needs and cost constraints and then use the manufacturer's suggestions for power rating to choose the correct core size. Calculating maximum flux density and core losses is a necessary sanity check on the manufacturer's recommendations.

In a roundabout way, holdup time specifications can affect the choice of power transformer magnetics. Increasing switching frequencies decreases the size of all the energy storage elements but one, the input filter capacitors. A specification requiring long holdup time will necessitate the use of large capacitors, which can very well be the tallest element in the converter. The input capacitors used here are Nichicon's 820  $\mu\text{F}$ , 200 V capacitors and have a height of 30 mm. Finding magnetics with a height of 30 mm or less is relatively easy, so the limiting dimension of the magnetics in this supply becomes its footprint area.

PQ, ETD and EC style cores are potential choices. Although ETD and EC cores are popular, they require more footprint area than the PQ core. The PQ bobbin also has a height-to-width ratio appropriate for the number of turns and layers needed for 150 W. Another advantage of the PQ core is that it is shaped to partially enclose the windings and thus reduce radiated noise; hence the choice is the PQ core.

The function of a transformer in a forward converter is to pass energy directly from input to output, not to store energy and then deliver it as is the case with a flyback core.

Consequently, most of the flux generated when the power transistor turns on is opposed by flux created by the secondary. Therefore, flux swings are lower than those of the flyback core, and the danger of core saturation is lessened. Ensuring good input/output coupling while maintaining isolation and keeping winding and core losses low still deserves attention. Gapping is not necessary since the purpose of a gap is to store energy or reduce the chance of core saturation.

The selected core (TDK PQ 32-30 core made with PC40 material, which is a 100+ kHz material) is slightly oversized per the manufacturer's recommendations but fits the application well. The full height and width of the bobbin are needed for the required number of turns. Using a smaller number of turns increases the magnetization current and flux density.

The primary-to-secondary turns ratio is calculated at lowest DC bus voltage, which is 200 V in this case. Calculating the required secondary voltage takes several simple steps. When the MOSFETs are on, the voltage required at the secondary to maintain the output voltage is:

$$V_{\text{sec}} = V_{\text{diode}} + V_{L(\text{on})} + V_{\text{out}}$$

where  $V_{\text{sec}}$  is the transformer's secondary voltage,  $V_{\text{diode}}$  is the output rectifier's forward voltage drop,  $V_{L(\text{on})}$  is the inductor voltage during the power transistor's on time, and  $V_{\text{out}}$  is the 5 V output voltage. Knowing that the inductor's average voltage is zero, we can find  $V_{L(\text{on})}$  from  $V_{L(\text{off})}$  as follows:

$$V_{L(\text{on})} = \frac{V_{L(\text{off})} \delta_{\text{off}}}{\delta_{\text{on}}}$$

With a maximum duty cycle of 45%, and  $V_{L(\text{off})} = V_{\text{out}} - V_{\text{diode}} = 5.0 - 0.5 = 4.5$  V,  $V_{L(\text{on})}$  is equal to 5.5 V.  $V_{\text{sec}}$  is then  $0.5 + 5.5 + 5.0 = 11.0$  V, and the turns ratio is 200 to 11 or about 18. Shape of the core and the winding area favor a 44 to 3 ratio (14.67 turns ratio), which adds some additional guardband to the design. To reduce the winding's AC and DC resistance, two layers of secondary are wound separately but connected in parallel, interleaved with the two halves of the primary winding. The bobbin's cross-section is shown in Figure 3.

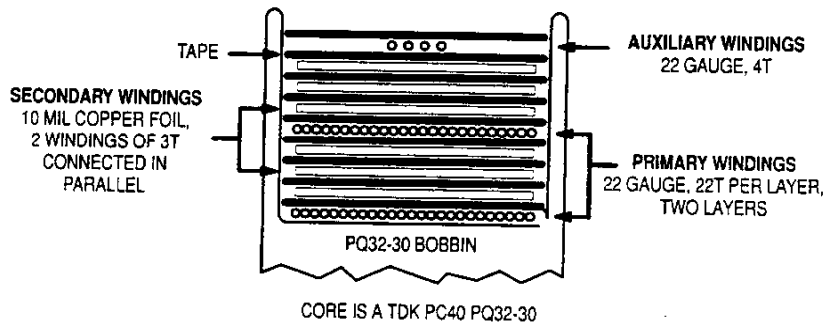


Figure 3. Cross Section of Power Transformer

Most power transformers also have an auxiliary winding to generate the supply voltage for the control IC. How that supply is generated depends on the system's topology. One advantage of a flyback converter is that because the output inductor is essentially part of the transformer, the output at the transformer's secondary is maintained at a regulated voltage and does not vary with input line voltage. All other windings mirror the voltage appearing at the output according to their respective turns ratios. The significance of this is that auxiliary supplies in a flyback system are easy to generate. They need no additional filter inductor and yield voltages independent of the input voltage and proportional to the output. Unfortunately, the forward converter does not share this attribute. Without an LC filter to remove the AC component, auxiliary voltages vary with changes in the input line voltage. Therefore, the designer is either forced to regulate the auxiliary voltage in a fashion similar to that used in this paper or add an additional inductor.

Clamping the peak auxiliary voltage with a capacitor and then regulating that voltage is the method used here to generate the IC's operating voltage. The voltage across the auxiliary winding is lowest at low line, or a bus voltage of 200 V. Four auxiliary turns yields a turns ratio of 44 to 4 and an 18 V output. Considering diode drops and the minimum drop across a series pass transistor (Q5 in Figure 4), 18 V is about right. Q5 and D17 regulate  $V_{CC}$  to about 14 V.

## OUTPUT INDUCTOR

The greatest challenge in the design of the output inductor is its 30 A average current at full load. High winding and core temperatures are concerns, but core saturation is the major worry. As was the case with the power transformer, dimensions of the winding area strongly influence core and bobbin selection. In this case the ability to bring high current leads out of the package is a prime consideration. The bobbin for the EC-35 core has dimensions that fit the application well, and its pins are positioned so that there is room to bring out a wide foil lead on one side.

Desired inductor ripple current and inductor voltage are obvious contributors to setting the size of the output inductor. Maximum off time of the power switch,  $t_{off}$ , is the third controlling element, since that is the longest time the inductor must maintain the desired ripple current. Maximum  $t_{off}$  occurs at high line and is equal to:

$$t_{off} = \frac{1 - \delta_{min}}{f_s} \quad \text{where}$$

$$\delta_{min} = \delta_{max} \frac{V_{in(min)}}{V_{in(max)}} = .45 \frac{2(\sqrt{2} \times 90)}{2(\sqrt{2} \times 132)} \approx .30$$

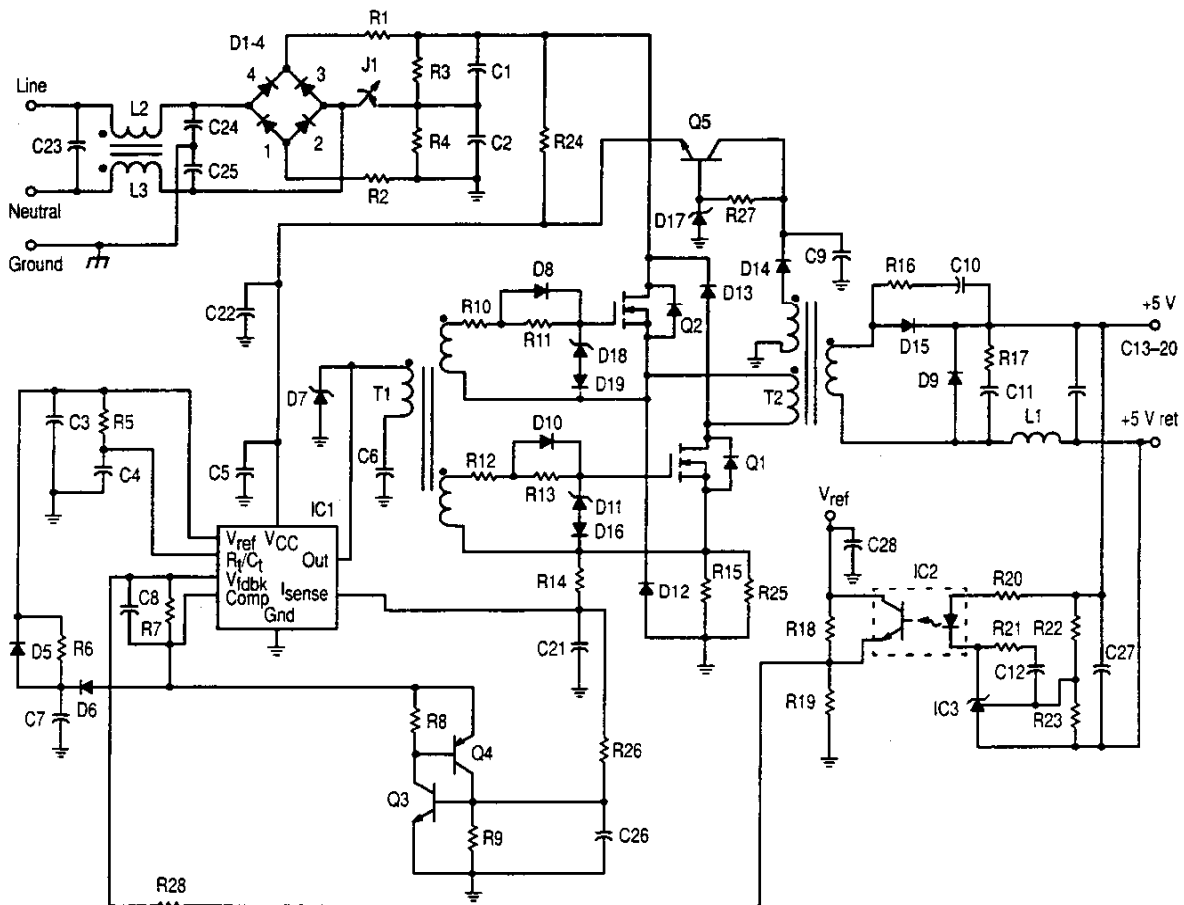


Figure 4. Schematic of a Two Transistor, Current Mode Forward Converter

Substituting for  $\delta_{\min}$  yields  $t_{\text{off}} = 4.67 \mu\text{s}$ . The output filter inductance should be about:

$$L_{\text{out}} = \frac{(V_{\text{out}} + V_{\text{diode}}) t_{\text{off}}}{\Delta I_{\text{o(max)}}} = 4.2 \mu\text{H}$$

Although maximum rated current is only 30 A, the coil could see peaks as high as 40 A during start up into a heavy load or under short circuit conditions. With inductor ripple current being a small fraction of the average current, flux swing will not be large. The core will operate at the upper right corner of the B-H curve where core saturation and not core losses is the greatest worry.

Philips' literature states that the maximum flux density of the 3C81 material (formerly 3C8) is 3300 Gauss at 100°C. The required number of turns can be calculated from:

$$N = \frac{L_{\text{pk}}}{BA_{\text{e}}} \times 10^8$$

where B is in Gauss and  $A_{\text{e}}$  (effective cross sectional core area) is in  $\text{cm}^2$ . Substitution yields:

$$N = \frac{4.3 \mu\text{H} \times 40 \text{ A}}{3300\text{G} \times .843 \text{ cm}^2} \times 10^8 = 5.95 \text{ turns}$$

The above formula shows that for a given inductance the number of turns increases as flux density decreases. Therefore, the core requires a *minimum* of N turns to limit the flux density to  $B_{\text{max}}$ . Several guardbands allow using 6 turns, which produces an inductor that saturates at about 40 A.

If the output inductor does saturate, current in the primary increases rapidly and the converter should limit peak current on a cycle by cycle basis. Viewing only the primary current can give the false impression that the transformer is saturating instead of the inductor, so clearly determine which element is saturating before beginning a redesign of the transformer or inductor.

Data sheet curves for the EC-35 core with 3C81 material recommend a 60 mil gap, which gives a 4.2  $\mu\text{H}$  coil. Two layers of 0.5", 10 mil copper foil handle the high currents well. A foil strip attached at a right angle to the winding forms one external connection. The second is a "flying lead," an extension of the main winding that comes straight from the bobbin with no change in angle.

## GATE DRIVE CIRCUIT AND TRANSFORMER

As is the case with the other magnetic elements, mechanical considerations affect the choice of the gate drive transformer. Theoretically, the control IC can drive the lower transistor directly since they share a common reference. In practice, driving both upper and lower transistors from the transformer provides a better chance of generating matched gate drive signals. Another advantage of driving the lower transistor with a transformer is that the gate signal is not distorted by the presence of inductance in series with the MOSFET's source. Therefore, the core contains three windings, one primary and two secondaries, and the bobbin must have a minimum of six pins. With three windings, isolation

requirements rather than the capability of the core limit the ability to downsize the transformer.

Primary to secondary isolation must be a minimum of 450 V since the bus voltage could reach nearly 380 Vdc. Maintaining creepage distance between layers in a small core prohibits the use of enamelled magnet wire. Teflon insulated wire takes up much more bobbin space than enamelled wire, but it vastly simplifies maintaining isolation, especially as the leads exit the bobbin.

RM-style transformers have a square footprint and use board space efficiently, so they are the choice here. Even the smallest RM cores have the required six pins, but assembly of a core smaller than the RM6 Z-12 is difficult. Of course, flux densities increase with a smaller core.

Unlike gate drive transformers in a half or full bridge, this transformer is to turn on both MOSFETs simultaneously. The UC3844 drives the primary directly, and resistors on the secondaries limit drive currents and switching speeds.

There are a couple of ways to reset the gate drive transformer's core. One is to use an additional ("catch") winding, but that solution adds yet another two pins to the bobbin, limits the choice bobbins, and adds manufacturing complexity. An alternative solution shown in the circuit diagram of Figure 4 is to use capacitor C6 in series with the drive IC to automatically inhibit the presence of DC voltage at the primary. With the average voltage removed, the positive and negative volt-seconds across the primary are equal. Therefore, as the converter approaches a 50% duty cycle, the positive excursion at the primary is only half of that seen at very low duty cycles.

The gate drive transformer has five layers in total; two for the first secondary, one for the primary, and two for the other secondary. The turns ratio (24 : 11-1/2 : 24) is set to make up for the voltage dropped across C6 at high duty cycles. The half turn is caused by having uneven number of pins on each side of the transformer.

As the duty cycle and primary voltage vary, so does the secondary voltage. At high line and light load the converter is at minimum duty cycle, and a zener diode limits the gate voltage to 18 V. Historically gate-to-source voltages of this magnitude have been viewed as being too high. Recent processing improvements now have made such operation more reliable. Typical gate-to-source breakdown voltages of Motorola's high voltage MOSFETs are in the 80 to 90 V range.

Diodes D16 and 19 are needed to ensure that the gate drive transformer sees only a capacitive load. Without them, drive current during the MOSFET's off time would be high, which would increase the IC operating current.

## REDUCING NOISE AND IMPROVING LAYOUT

Forward and reverse recovery of the output rectifiers and switching of the power transistors causes EMI, RFI and heating. Blindly increasing switching speeds to reduce losses is likely to produce severe noise just as certainly as slowing switching speeds will increase heating. Fortunately, some design practices help the designer use high switching speeds without generating excessive noise.

A good layout is fundamental to controlling noise. Major concerns are rapid changes in voltage across parasitic capacitors and abrupt changes in current in parasitic inductors. Large  $dv/dt$ 's are more common on the primary circuit and high  $di/dt$ 's occur more often in the secondary, so the priority is to minimize parasitic capacitance in the primary and parasitic inductance in the secondary.

Layout of the transformer secondary and output rectifiers should take precedence over the layout of all other circuitry. The output capacitors, rectifiers and power transformer secondary should be as tightly packaged as practical. The only element in the secondary that is not greatly affected by parasitic inductance is the inductor itself. All secondary connections should be wide tracks to further reduce inductance and increase current handling ability. Parallel runs help, but runs are so wide on the secondary that placing them in parallel is often difficult. Using multiple ounce copper will increase current handling capability but will not necessarily decrease inductance.

Output rectifiers can also experience very high  $dv/dt$ 's. Some of the newer Schottkys have  $dv/dt$  ratings of 5000 V/ $\mu$ s or higher. These high  $dv/dt$ 's usually inject noise into the heat-sink via the Schottky's parasitic header-to-heat-sink capacitance, but this problem is avoidable. The output filter inductor does not have to lie between the output rectifiers and the +5 V output; it can be placed in the return loop as shown in Figure 4. Circuit operation remains unchanged since the coil is still in series with the parallel combination of the load and the output capacitors. The advantage of this rearrangement is that the cathodes (and headers) of the rectifiers are no longer on a node that has rapid voltage swings and less noise is injected into the heat-sink. The tradeoff in putting the inductor in the return leg is that the secondary of the transformer now moves from a quiet node (the return of the 5 V output) to a noisy one, so it may become a source of radiated noise.

Turning to the primary side, the upper MOSFET does not emit much noise since the voltage on its header has essentially no AC component. The lower power transistor is not as innocent. Its header swings approximately 320 V in 50 to 100 ns. Header to heat-sink capacitance decreases with greater insulator thickness, so a ceramic insulator is an option.

Rules for grounding are all-important and not difficult to master. The underlying principle is "Keep high currents out of logic grounds." Avoid ground loops, as they pick up noise. Use single point, or star, grounding instead. On the primary side there are two sources of high current. Current flowing through the MOSFETs and the power transformer are the first source of high  $di/dt$ 's. Gate drive currents can also be high, so a separate ground return for the gate drive is required. These currents converge on the source pin of the power transistor, making it the best location for a single point ground. A single large groundplane is not recommended, since there is little control of where currents flow and the large surface area can act as an antenna. Double sided circuit boards are usually a must for a good layout.

Once the layout is optimized, options for reducing noise get scarce and difficult to implement. The problem is that fields are set up in parasitic inductors and charge is stored in parasitic capacitors — both of which involve energy storage. This energy must either be radiated, electrically conducted out of the system, recovered via a lossless snubber, or dissipated within the system (most likely in a snubber or added to switching losses). The two least exotic and most practical options are to reduce switching speeds and add snubbers.

Very high switching speeds complicate snubber design since more parasitic elements must be included in the analysis. Rise time of the rectifier's voltage, peak current to be snubbed, and energy to be dissipated are factored into the selection of R16 and R17. In order for the snubber capacitors C10 and C11 to establish voltage rise time, they must be large compared to the MBR2535CTL's junction capacitance. Low inductance carbon composition resistors keep the snubber effective at high  $di/dt$ 's.

There is one other layout issue, but it has nothing to do with noise. Using only a single output capacitor is often impractical since several are required to reduce ripple and minimize ESR, or equivalent series resistance. ESR decreases nearly twofold as the capacitor's temperature rises from 20 to 85°C, so a capacitor with a low ESR or one that is positioned to take on higher than average current will heat up and then take on an even greater share of total current. Using a star connection to ensure a symmetrical layout is a thought, but that introduces excessive inductance and increases output voltage ripple. The best approach is to use fewer but larger capacitors, keep the capacitors tightly clustered, use multiple layer traces with heavy copper to keep parasitic resistance low, and keep the layout symmetrical. In this supply the capacitors' case temperatures are unequal without a small amount of forced air cooling.

## CONTROL LOOP

Designing the feedback loop is the last major challenge in the design of a power supply. Although current mode control has its advantages, it is fundamentally more difficult to understand. That is not to say that it is more difficult to implement. Compensation is actually simpler and the circuit itself is very robust with respect to wiring errors and design mistakes. Fortunately, undertaking a complete analysis from scratch is not necessary since others have suggested compensation schemes for the various converter types. The following steps are a good guideline for closing the feedback loop.

- Step 1: Determine the converter type and find a reference that describes that converter family, lists the sources of the prominent poles and zeros in its control-to-output transfer characteristics, and recommends a compensation network. References 1, 3, 5 and 6 are best bets.
- Step 2: Determine the frequency of all poles and zeros of the control-to-output transfer characteristics.

- Step 3: Determine the DC gain of the control-to-output transfer characteristics.
- Step 4: Draw the bode plot of the open loop control-to-output transfer characteristics
- Step 5: Draw the bode plot of the desired closed loop transfer characteristics
- Step 6: Determine the gain and the location of the compensation network's poles and zeros needed to achieve the desired closed loop response.

For this forward converter operating in the continuous mode there is a pole which is a function of the effective load resistance and the output filter capacitance. Since the pole's location varies with load, it is best to draw the Bode plot at minimum and maximum load. A thorough treatment also entails plots at low and high line. In this case the output capacitance is 8,800  $\mu\text{F}$  and the load ranges from .83 to .166  $\Omega$  (5 to 30 A), which results in corner frequencies of 22 and 108 Hz. The first pole is then:

$$f_{p1} = \frac{1}{2\pi R_L C_O}$$

The zero contributed by the output filter capacitor and its ESR is the second breakpoint on the control-to-output transfer characteristics curve. Illinois Capacitor provides characterization that shows ESR is a strong function of temperature, which makes the location of the zero temperature dependent. For an ESR of .07  $\Omega$  and a capacitance of 2200  $\mu\text{F}$ , the following formula positions the zero at 1447 Hz:

$$f_{z1} = \frac{1}{2\pi \text{RESRC}_O}$$

Another pole occurs at half the output switching frequency, or 75 kHz. The loop gain will be so low at this frequency that this pole is ignored in the remaining analysis.

The next task is to estimate the control-to-output gain. The input variable is the voltage  $V_e$  at the output of the UC3844's error amplifier, and the output variable is the converter's output voltage  $V_o$ . Due to a resistive divider internal to the UC3844, the voltage at the inverting input of the current sense comparator is one-third of  $V_e$ . The current sense resistor gives the voltage to current transformation:

$$\Delta V_e = 3R_S \Delta i_D$$

Power transistor current is approximately equal to the sum of the inductor ripple current and the output current divided by the transformer's turns ratio plus the magnetization current. The approximation in formula form is:

$$i_D = \frac{I_O}{n} + t_{on} \left( \frac{V_L}{n L_O} + \frac{V_{in}}{L_{mag}} \right)$$

where  $I_O$  is the output current,  $n$  is the turns ratio (15 in this case), and  $V_{in}$  is the DC bus voltage.  $L_O$  is equal to 4.2  $\mu\text{H}$ , and at high line  $V_L$  is approximately 19 V, calculated from:

$$V_L = V_S - V_D - V_O = \left( V_{in} \frac{n_s}{n_p} \right) - V_D - V_O$$

$I_O$  is equal to 30 A at full load and

$$i_D = 2 + t_{on} \frac{19}{15 (4.2 \times 10^{-6})} \frac{\text{A}}{\mu\text{s}} + t_{on} \frac{370}{6.67 \times 10^{-3}} \frac{\text{A}}{\mu\text{s}} \text{ or}$$

$$i_D = 2 + t_{on} \left( 300 \frac{\text{mA}}{\mu\text{s}} + 55 \frac{\text{mA}}{\mu\text{s}} \right)$$

From the above we can relate changes in drain current to on time ( $\Delta i/\Delta t = 355 \text{ mA}/\mu\text{s}$ ). Now the job is to relate changes in drain current and on time to a change in output voltage. The output voltage is related to the turns ratio, input voltage and on time as follows:

$$V_o = \frac{V_{in} t_{on}}{nT}$$

Putting all the conversions together gives:

$$\text{Gain} = \frac{V_o}{V_e} = \frac{V_{in}}{3R_S nT} \frac{di_D}{dt_{on}}$$

Substituting values gives a control-to-output DC gain of 11.2 or 21 dB.

The next step is to set the DC gain of the feedback circuit. At very low frequencies C12 acts like an open circuit and the gain is limited by the TL431's open loop gain, which is given as 54 dB (500) on the data sheet. This figure is a voltage gain for a specific cathode resistance, 230  $\Omega$ . For determining performance with other resistances, the TL431 is best viewed as a transconductance amplifier. Its voltage gain is converted to a transconductance as follows:

$$G_{TL431} = 500 = \frac{\Delta V_{cat}}{\Delta V_{ref}} = \frac{\Delta i_{cat} \times 230 \Omega}{\Delta V_{ref}} \text{ or}$$

$$\frac{\Delta i_{cat}}{\Delta V_{ref}} = \frac{500}{230} = 2.17 \text{ mhos}$$

The only other variables affecting DC gain are the ratio of R22 and R23, the current transfer ratio (CTR) of the MOC8102, and the resistance of R19. From  $V_O$  to the R18/R19 resistive divider the gain is:

$$G = \frac{R_{23}}{R_{22} + R_{23}} (2.17 \text{ mhos}) (\text{CTR}) R_{19}$$

Using a CTR of .9, a one to one ratio between R22 and R23, and 1 k $\Omega$  for R19 gives a gain of 60 dB. Total closed loop gain comes to 81 dB, which gives the converter its good load regulation.



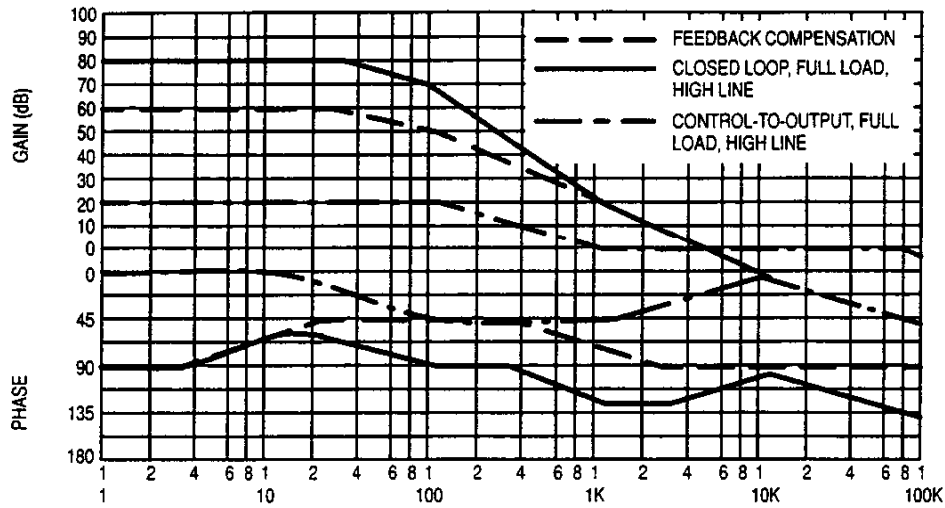


Figure 5. Bode Plot for Small Signal Loop Gain

In the preceding analysis it is assumed that the TL431 acts as a transconductance amplifier at high as well as low frequencies. This may not be true of some manufacturer's devices. Another pointer is that if the feedback loop is broken to inject a signal for measuring the loop gain, break it so that currents in R20 and R22 are both included in the loop.

The two pole, single zero compensation network used in this supply is split between the TL431 and the UC3844's error amplifier. Assigning one pole to the UC3844 helps filter any noise that is induced between the TL431 and the IC. The control to output transfer characteristics and the estimate of the converter's closed loop response is shown in Figure 5.

The astute reader has probably noticed there were numerous estimates and assumptions made in the above analysis. Capacitor ESL, noise, low pass filtering of the current sense signal, delay and phase shift induced by the turn off delay time of the power transistors, temperature effects on the output capacitor's ESR, load characteristics including excessive capacitive and inductive loading, frequency response of the MOC8102 and TL431, and device tolerances were not included. Most of these effects are minor or occur at high frequencies. Nevertheless, the above listing of assumptions shows that Bode plots are only a best guess of system performance.

Two other problems that have pestered designers are wide variations in the optocoupler's Current Transfer Ratio (CTR) and gradual degradation of the opto's LED output. Both problems increase CTR variation and thereby complicate the design. The MOC8101 through MOC8104 form a new series of optocouplers designed and specified for use in power supplies. One of their strengths is their tight CTR distribution. The comparison of ratings shown in Table 1 indicates that the MOC8102 gives much better control of the converter's loop gain than the popular 4N25.

Table 1. Comparison of Popular Optocouplers

	MOC8102	4N25
Minimum CTR	.73	0.20
Typical CTR	.90	0.70
Maximum CTR	1.17	no limit
Base Pin of Output Transistor	Not Pinned Out	Pinned Out

The MOC8100 series devices incorporate another improvement, low degradation LEDs. Until just recently, industry wide tests showed that LED degradation was typically 15 to 20% after 1000 hours, with some parts degrading by as much as 50%. After gaining a better understanding of the degradation mechanism, Motorola designers produced a very stable LED, and they are now using the improved LED for all optocouplers. Typical degradation of devices like the MOC8102 is approximately 1% at 7500 hours for an LED input current of 50 mA, which accelerates the test. One final modification in the design of the MOC8102 is that the base pin of its output transistor is left unconnected, which reduces noise pickup.

### SYSTEM PERFORMANCE

This supply runs at efficiencies typical of 5 V supplies. It varies from a peak of 81% at an output current of 15 A to a low of 73% at 5 A, the lowest specified operating current. Besides the obvious benefit of power savings, higher efficiencies help reduce power supply volume by decreasing heatsink size. Lower junction temperatures also improve reliability.

One way to boost efficiency is to use larger power semiconductors. For example, the power MOSFET can be replaced by an MTP8N50E. This cuts the MOSFET's on-state losses in half and saves 2 W total for the two MOSFETs. Switching

losses increase for an unchanged gate drive, but there is plenty of latitude in speeding the gate drive to maintain the speed and low switching losses of the existing MTP4N50E's.

Supplies that deliver low output voltages have a difficult time achieving high efficiencies since the drop across the output rectifier is 6 to 20% of the output voltage. For a supply with a 5 V output, every 100 mV drop across the output rectifier equates to a 2% decrease in efficiency. For its size, the MBR2535CTL is hard to beat, so improvements currently require larger packages or multiple devices. Using two MBR2535CTLs in place of each existing one cuts the  $V_f$  from .42 to .33 V, which saves nearly another 3 W. Keeping their headers (and dice) at similar temperatures by placing them side by side on the same heatsink is a way to help maintain current sharing in paralleled Schottkys.

With respect to load and line variation,  $V_o$  varies by 10 mV with maximum variation in load and input line voltage. Output ripple is 50 mV peak to peak with additional high frequency spikes of 150 mV peak to peak, which is typical of a supply with a single stage output filter. High frequency spikes are believed to be caused by parasitic interwinding capacitance of the output filter inductor. Overcurrent shutdown is triggered by Q3 and Q4 and occurs between output currents of 36 and 39 A, depending on input voltage.

Response to a step change in output current gives a good overall view of the stability of the system and its high frequency output impedance, which is primarily set by the ESR of the output filter capacitors. Figure 6 shows the supply's transient response to a step change in output current from 15 to 20 A. The 40 mV dip in  $V_o$  suggests that the capacitor ESR is 8 m $\Omega$ . The supply recovers within about 400  $\mu$ s.

Hold up time is a measure of how long the converter is able to maintain the output voltage after the AC power has been interrupted. At nominal input voltage and full load hold up time is about 55 ms, as shown in Figure 7. The following equation gives the relationship between the relevant variables:

$$t_{\text{hold up}} \times \frac{P_{\text{out}}}{\eta} = \frac{1}{2} C (V_{\text{initial}}^2 - V_{\text{drop out}}^2)$$

Their high energy storage density and low profile (35 mm in diameter and 30 mm tall) make a pair of 200 V, 820  $\mu$ F electrolytics (Nichicon part #LLK2D821MHSC) good input filter capacitors. A 250 V version is available at the expense of an additional 5 mm of height.

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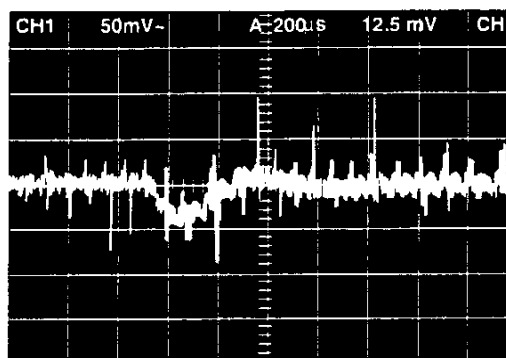


Figure 6. Step Change in  $V_{\text{out}}$  (50 mV/div) to a 5 A Change in Output Current

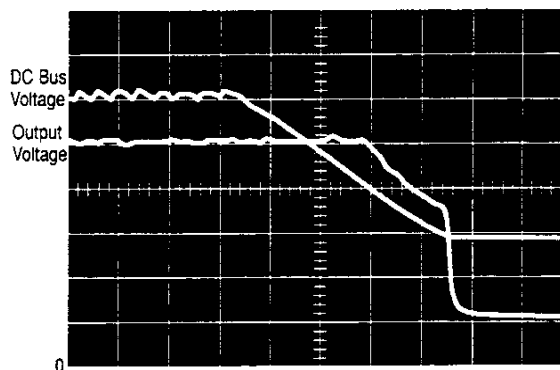



Figure 7. Output Voltage (1 V/div) and DC Bus Voltage (50 V/div) after Interruption of AC Power

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**Parts List for 150 W Forward Converter**

Designator	Qty	Description	Rating	Tol.	Manufact.	Part Number	Type
C1, 2	2	820 $\mu$ F, Elect. Cap.	200 V	10%	Nichicon	LLK2D821MHSC	Al. Elec.
C3, 8, 27, 28	4	0.01 $\mu$ F, Capacitor	50 V	10%			ceramic
C4	1	500 pF, Capacitor	50 V	5%			mica
C5, 6, 12	3	1 $\mu$ F, Capacitor	50 V	10%			ceramic
C7, 22	2	10 $\mu$ F, Elect. Cap.	50 V	10%			Al. Elec.
C9	1	5 $\mu$ F, Elect. Cap.	50 V	10%			Al. Elec.
C10, 11	2	0.022 $\mu$ F, Capacitor	63 V	10%	Wima	MKS 2-i series	met. polyester
C13-16	4	2200 $\mu$ F, Capacitor	16 V	10%	Ill. Cap.	228RZS016M	Al. Elec.
C17-20	4	1 $\mu$ F, Capacitor	63 V	10%	Wima	MKS 3 series	met. polyester
C21	1	390 pF, Capacitor	50 V	5%			mica
C23	1	0.1 $\mu$ F, Capacitor	275 V	20%	Rifa	PME285MB6100M	met. paper
C24, 25	2	4700 pF, Capacitor	275 V	20%	Rifa	PME289MA4470M	met. paper
C26	1	100 pF, Capacitor	50 V	5%			mica
C29	1	0.068 $\mu$ F, Capacitor	400 V	10%	Wima	MKP 10 series	met. polypro.
D1, 2, 3, 4	4	600 V Diode	3.0 A		Motorola	MR506	std. recovery
D5, 6, 8, 10, 16, 19	6	Diode				1N914	
D7	1	40 V Diode	0.5 A		Motorola	MBR040	Schottky
D9, 15	2	35 V Dual Diode	25 A		Motorola	MBR2535CTL	Schottky
D11, 18	1	18 V Zener	1.5 W	5%	Motorola	1N5931B	
D12, 13	2	600 V Diode	1 A		Motorola	MUR160	Ultrafast
D14	1	50 V Diode	1 A		Motorola	1N4001	Standard Recovery
D17	1	15 V Zener	1.5 W	5%	Motorola	1N5929B	
Q1, 2	2	N-ch MOSFET, 1.5 $\Omega$	500 V		Motorola	MTP4N50E	
Q3	1	NPN, 0.2 A	40 V		Motorola	2N3904	
Q4	1	PNP, 0.2 A	40 V		Motorola	2N3906	
Q5	1	NPN, 1 A	40 V		Motorola	MPSW01	
R1, 2	2	Thermistor	2.8 A		Keystone	CL-160	
R3, 4	2	82K Resistor	1 W	5%			
R5, 8, 9,	3	10K Resistor	1/4 W	5%			
R6	1	1M Resistor	1/4 W	5%			
R7, 28	2	51K Resistor	1/4 W	5%			
R10, 12	2	51 $\Omega$ Resistor	1/4 W	5%			
R11, 13	2	82 $\Omega$ Resistor	1/4 W	5%			
R14	1	620 $\Omega$ Resistor	1/4 W	5%			
R15, 25	2	0.62 $\Omega$ Resistor	1/2 W	5%			Low induct.
R16, 17	2	3.3 $\Omega$ Resistor	2 W	5%			Low induct.
R18	1	3.9K Resistor	1/4 W	5%			
R19	1	1K Resistor	1/4 W	5%			
R20	1	100 $\Omega$ Resistor	1/4 W	5%			
R21	1	5.1K Resistor	1/4 W	5%			
R22, 23	2	1K Resistor	1/4 W	1%			
R24	1	160K Resistor	1 W	5%			
R26	1	4.3K Resistor	1/4 W	5%			
R27	1	2K Resistor	1/4 W	5%			
T1	1	Gate Drive Transformer			TDK	PC40RM06Z-12	(see text)
T2	1	Power Transformer			TDK	PC40PQ32/30Z-12	(see text)
IC1	1	Current Mode Contr. IC			Motorola	UC3844AN	
IC2	1	Optocoupler			Motorola	MOC8102	
IC3	1	Program. Volt. Ref.			Motorola	TL431CLP	
J1	1	Jumper 110 (closed)/220 selection					
L1	1	Output Filter Inductor	4.2 $\mu$ H		Philips	EC35 Core, 3C81	(see text)
L2, 3	1	Line Filter			Pulse Eng.	1/2 of #96171	

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